# 2-Channel, 12-Bit ADC with I²C-Compatible Interface in 10-Lead MSOP

# AD7992

## FEATURES

- 12-bit ADC with fast conversion time: 2 µs typ
- 2 single-ended analog input channels
- Specified for $V_{DD}$ of 2.7 V to 5.5 V
- Low power consumption
- Fast throughput rate: up to 188 kSPS
- Sequencer operation
- Temperature range: −40 °C to 125 °C
- Automatic cycle mode
- I²C®-compatible serial interface supports standard, fast, and high speed modes
- Out-of-range indicator/alert function
- Pin-selectable addressing via AS
- 2 versions allow 5 I²C addresses
- Shutdown mode: 1 µA max
- 10-lead MSOP package

## GENERAL DESCRIPTION

The AD7992 is a 12-bit, low power, successive approximation ADC with an I²C-compatible interface. The part operates from a single 2.7 V to 5.5 V power supply and features a 2 µs conversion time. The part contains a 2-channel multiplexer and track-and-hold amplifier that can handle input frequencies up to 11 MHz.

The AD7992 provides a 2-wire serial interface compatible with I²C interfaces. The part comes in two versions, the AD7992-0 and the AD7992-1, and each version allows for at least two different I²C addresses. The AD7992-0 supports standard and fast I²C interface modes, and the AD7992-1 supports standard, fast, and high speed I²C interface modes.

The AD7992 normally remains in a shutdown state while not converting, and powers up only for conversions. The conversion process can be controlled using the $\overline{\text{CONVST}}$ pin, by a command mode where conversions occur across I²C write operations, or an automatic conversion interval mode selected through software control.

The AD7992 requires an external reference in the range of 1.2 V to $V_{DD}$. This allows the widest dynamic input range to the ADC. On-chip limit registers can be programmed with high and low limits for the conversion result, and an open-drain, out-of-range indicator output (ALERT) becomes active when the conversion result violates the programmed high or low limits. This output can be used as an interrupt.

## FUNCTIONAL BLOCK DIAGRAM

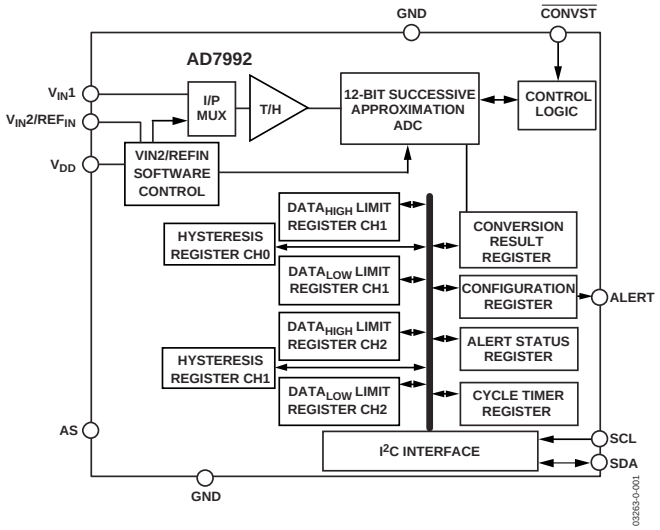


*Figure 1.*

## PRODUCT HIGHLIGHTS

1. 2 µs conversion time and low power consumption.
2. I²C-compatible serial interface with pin-selectable addresses. Two AD7992 versions allow five AD7992 devices to be connected to the same serial bus.
3. The part features automatic shutdown while not converting to maximize power efficiency. Current consumption is 1 µA max when in shutdown mode at 3 V.
4. Reference can be driven up to the power supply.
5. Out-of-range indicator that can be software disabled or enabled.
6. One-shot and automatic conversion rates.
7. Registers store minimum and maximum conversion results.

**Table 1. Related Products**

| Part Number | No. of Bits | No. of Channels | Package |
|---|---|---|---|
| AD7998 | 12 | 8 | 20-TSSOP |
| AD7994 | 12 | 4 | 16-TSSOP |
| AD7997 | 10 | 8 | 20-TSSOP |
| AD7993 | 10 | 4 | 16-TSSOP |

**Rev. 0**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.326.8703** 

# TABLE OF CONTENTS



## REVISION HISTORY

**1/05—Revision 0: Initial Version**

# SPECIFICATIONS

Temperature range for B version is −40°C to +125°C. Unless otherwise noted, $V_{DD}$ = 2.7 V to 5.5 V; $REF_{IN}$ = 2.5 V to $V_{DD}$. For the AD7992-0, all specifications apply for $f_{SCL}$ up to 400 kHz; for the AD7992-1 all specifications apply for $f_{SCL}$ up to 3.4 MHz. All specifications are for both single-channel mode and dual-channel mode, Unless otherwise noted; $T_A = T_{MIN}$ to $T_{MAX}$.

**Table 2.**

| Parameter | B Version | Unit | Test Conditions/Comments |
|---|---|---|---|
| DYNAMIC PERFORMANCE[1] | | | $F_{IN}$ = 10 kHz sine wave for $f_{SCL}$ from 1.7 MHz to 3.4 MHz |
| | | | $F_{IN}$ = 1 kHz sine wave for $f_{SCL}$ up to 400 kHz |
| Signal-to-Noise + Distortion (SINAD)[2] | 70.5 | dB min | |
| Signal-to-Noise Ratio (SNR)[2] | 71 | dB min | |
| Total Harmonic Distortion (THD)[2] | −78 | dB max | |
| Peak Harmonic or Spurious Noise (SFDR)[2] | −79 | dB max | |
| Intermodulation Distortion (IMD)[2] | | | fa = 10.1 kHz, fb = 9.9 kHz for $f_{SCL}$ from 1.7 MHz to 3.4 MHz |
| | | | fa = 1.1 kHz, fb = 0.9 kHz for $f_{SCL}$ up to 400 kHz |
| Second-Order Terms | −90 | dB typ | |
| Third-Order Terms | −90 | dB typ | |
| Aperture Delay[2] | 10 | ns max | |
| Aperture Jitter[2] | 50 | ps typ | |
| Channel-to-Channel Isolation[2] | −90 | dB typ | $F_{IN}$ = 108 Hz; see the Terminology section |
| Full Power Bandwidth[2] | 11 | MHz typ | @ 3 dB |
| | 2 | MHz typ | @ 0.1 dB |
| DC ACCURACY | | | |
| Resolution | 12 | Bits | |
| Integral Nonlinearity[1, 2] | ±1 | LSB max | |
| | ±0.2 | LSB typ | |
| Differential Nonlinearity[1, 2] | +1/−0.9 | LSB max | Guaranteed no missed codes to 12 bits |
| | ±0.2 | LSB typ | |
| Offset Error[2] | ±4 | LSB max | Mode 1 ($\overline{CONVST}$ mode) |
| | ±6 | LSB max | Mode 2 (command mode) |
| Offset Error Match[2] | ±1 | LSB max | Dual-channel mode |
| Gain Error[2] | ±2 | LSB max | |
| Gain Error Match[2] | ±1 | LSB max | Dual-channel mode |
| ANALOG INPUT | | | |
| Input Voltage Range | 0 to $REF_{IN}$ | V | |
| DC Leakage Current | ±1 | µA max | |
| Input Capacitance | 30 | pF typ | |
| REFERENCE INPUT | | | |
| $REF_{IN}$ Input Voltage Range | 1.2 to $V_{DD}$ | V min/V max | |
| DC Leakage Current | ±1 | µA max | |
| Input Impedance | 69 | kΩ typ | |
| LOGIC INPUTS (SDA, SCL) | | | |
| Input High Voltage, $V_{INH}$ | 0.7 ($V_{DD}$) | V min | |
| Input Low Voltage, $V_{INL}$ | 0.3 ($V_{DD}$) | V max | |
| Input Leakage Current, $I_{IN}$ | ±1 | µA max | $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[3] | 10 | pF max | |
| Input Hysteresis, $V_{HYST}$ | 0.1 ($V_{DD}$) | V min | |

| Parameter | B Version | Unit | Test Conditions/Comments |
|---|---|---|---|
| LOGIC INPUTS ($\overline{CONVST}$) | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | V min | $V_{DD}$ = 5 V |
| | 2.0 | V min | $V_{DD}$ = 3 V |
| Input Low Voltage, $V_{INL}$ | 0.8 | V max | $V_{DD}$ = 5 V |
| | 0.4 | V max | $V_{DD}$ = 3 V |
| Input Leakage Current, $I_{IN}$ | ±1 | μA max | $V_{IN}$ = 0 V or $V_{DD}$ |
| Input Capacitance, $C_{IN}$[3] | 10 | pF max | |
| LOGIC OUTPUTS (OPEN DRAIN) | | | |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 3 mA |
| | 0.6 | V max | $I_{SINK}$ = 6 mA |
| Floating-State Leakage Current | ±1 | μA max | |
| Floating-State Output Capacitance[3] | 10 | pF max | |
| Output Coding | Straight (Natural) Binary | | |
| CONVERSION RATE | | | See the Serial Interface section |
| Conversion Time | 2 | μs typ | |
| Throughput Rate | | | |
| Mode 1 (Reading after the Conversion) | 5 | kSPS typ | $f_{SCL}$ = 100 kHz |
| | 21 | kSPS typ | $f_{SCL}$ = 400 kHz |
| | 121 | kSPS typ | $f_{SCL}$ = 3.4 MHz |
| Mode 2 | 5.5 | kSPS typ | $f_{SCL}$ = 100 kHz |
| | 22 | kSPS typ | $f_{SCL}$ = 400 kHz |
| | 147 | kSPS typ | $f_{SCL}$ = 3.4 MHz , 188 kSPS typ @ 5 V |
| POWER REQUIREMENTS | | | |
| $V_{DD}$ | 2.7/5.5 | V min/max | |
| $I_{DD}$ | | | Digital inputs = 0 V or $V_{DD}$ |
| Power-Down Mode, Interface Inactive | 1/2 | μA max | $V_{DD}$ = 3.3 V/5.5 V |
| Power-Down Mode, Interface Active | 0.07/0.3 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 400 kHz $f_{SCL}$ |
| | 0.3/0.6 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ |
| Operating, Interface Inactive | 0.06/0.1 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 400 kHz $f_{SCL}$ |
| | 0.3/0.6 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ |
| Operating, Interface Active | 0.15/0.4 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 400 kHz $f_{SCL}$ |
| | 0.6/1.1 | mA max | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ Mode1 |
| | 0.7/1.4 | mA typ | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ Mode 2 |
| Mode 3 ($I^2C$ Inactive, $T_{CONVERT} \times 32$) | 0.7/1.5 | mA max | $V_{DD}$ = 3.3 V/5.5 V |
| POWER DISSIPATION | | | |
| Fully Operational | | | |
| Operating, Interface Active | 0.495/2.2 | mW max | $V_{DD}$ = 3.3 V/5.5 V, 400 kHz $f_{SCL}$ |
| | 1.98/6.05 | mW max | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ Mode 1 |
| | 2.31/7.7 | mW typ | $V_{DD}$ = 3.3 V/5.5 V, 3.4 MHz $f_{SCL}$ Mode 2 |
| Power Down, Interface Inactive | 3.3/11 | μW max | $V_{DD}$ = 3.3 V/5.5 V |

[1] Maximum/minimum ac dynamic performance, INL and DNL specifications are typical specifications when operating in Mode 2 with $I^2C$ high speed mode SCL frequencies. Specifications outlined for Mode 2 apply to Mode 3 also. Sample delay and bit trial delay enabled.
[2] See the Terminology section.
[3] Guaranteed by initial characterization.

# I²C TIMING SPECIFICATIONS

Guaranteed by initial characterization. All values measured with the input filtering enabled. $C_B$ refers to the capacitive load on the bus line. $t_r$ and $t_f$ measured between 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

High speed mode timing specifications apply to the AD7992-1 only. Standard and fast mode timing specifications apply to both the AD7992-0 and the AD7992-1. See Figure 2. Unless otherwise noted, $V_{DD}$ = 2.7 V to 5.5 V; $REF_{IN}$ = 2.5 V to $V_{DD}$; $T_A$ = $T_{MIN}$ to $T_{MAX}$.

**Table 3.**

| | | Limit at $T_{MIN}$, $T_{MAX}$ | | | |
|---|---|---|---|---|---|
| **Parameter** | **Conditions** | **Min** | **Max** | **Unit** | **Description** |
| $f_{SCL}$ | Standard mode | | 100 | kHz | Serial clock frequency |
| | Fast mode | | 400 | kHz | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | | 3.4 | MHz | |
| | $C_B$ = 400 pF max | | 1.7 | MHz | |
| $t_1$ | Standard mode | 4 | | µs | $t_{HIGH}$, SCL high time |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 60 | | ns | |
| | $C_B$ = 400 pF max | 120 | | ns | |
| $t_2$ | Standard mode | 4.7 | | µs | $t_{LOW}$, SCL low time |
| | Fast mode | 1.3 | | µs | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 160 | | ns | |
| | $C_B$ = 400 pF max | 320 | | ns | |
| $t_3$ | Standard mode | 250 | | ns | $t_{SU;DAT}$, data setup time |
| | Fast mode | 100 | | ns | |
| | High speed mode | 10 | | ns | |
| $t_4$[1] | Standard mode | 0 | 3.45 | µs | $t_{HD;DAT}$, data hold time |
| | Fast mode | 0 | 0.9 | µs | |
| | High Speed mode | | | | |
| | $C_B$ = 100 pF max | 0 | 70[2] | ns | |
| | $C_B$ = 400 pF max | 0 | 150 | ns | |
| $t_5$ | Standard mode | 4.7 | | µs | $t_{SU;STA}$, setup time for a repeated START condition |
| | Fast mode | 0.6 | | µs | |
| | High Speed mode | 160 | | ns | |
| $t_6$ | Standard mode | 4 | | µs | $t_{HD;STA}$, hold time for a repeated START condition |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | 160 | | ns | |
| $t_7$ | Standard mode | 4.7 | | µs | $t_{BUF}$, bus free time between a STOP and a START condition |
| | Fast mode | 1.3 | | µs | |
| $t_8$ | Standard mode | 4 | | µs | $t_{SU;STO}$, setup time for STOP condition |
| | Fast mode | 0.6 | | µs | |
| | High speed mode | 160 | | ns | |
| $t_9$ | Standard mode | | 1000 | ns | $t_{RDA}$, rise time of SDA signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |

| Parameter | Conditions | Limit at $T_{MIN}$, $T_{MAX}$ | | | Description |
|---|---|---|---|---|---|
| | | Min | Max | Unit | |
| $t_{10}$ | Standard mode | | 300 | ns | $t_{FDA}$, fall time of SDA signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |
| $t_{11}$ | Standard mode | | 1000 | ns | $t_{RCL}$, rise time of SCL signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 40 | ns | |
| | $C_B$ = 400 pF max | 20 | 80 | ns | |
| $t_{11A}$ | Standard mode | | 1000 | ns | $t_{RCL1}$, rise time of SCL signal after a repeated START condition and after an acknowledge bit |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 80 | ns | |
| | $C_B$ = 400 pF max | 20 | 160 | ns | |
| $t_{12}$ | Standard mode | | 300 | ns | $t_{FCL}$, fall time of SCL signal |
| | Fast mode | 20 + 0.1 $C_B$ | 300 | ns | |
| | High speed mode | | | | |
| | $C_B$ = 100 pF max | 10 | 40 | ns | |
| | $C_B$ = 400 pF max | 20 | 80 | ns | |
| $t_{SP}$ | Fast mode | 0 | 50 | ns | Pulse width of suppressed spike |
| | High speed mode | 0 | 10 | ns | |
| $t_{POWER-UP}$ | | 1 | | µs typ | Power-up time |

[1] A device must provide a data hold time for SDA in order to bridge the undefined region of the SCL falling edge.
[2] For 3 V supplies, the maximum hold time with $C_B$ = 100 pF max is 100 ns max.

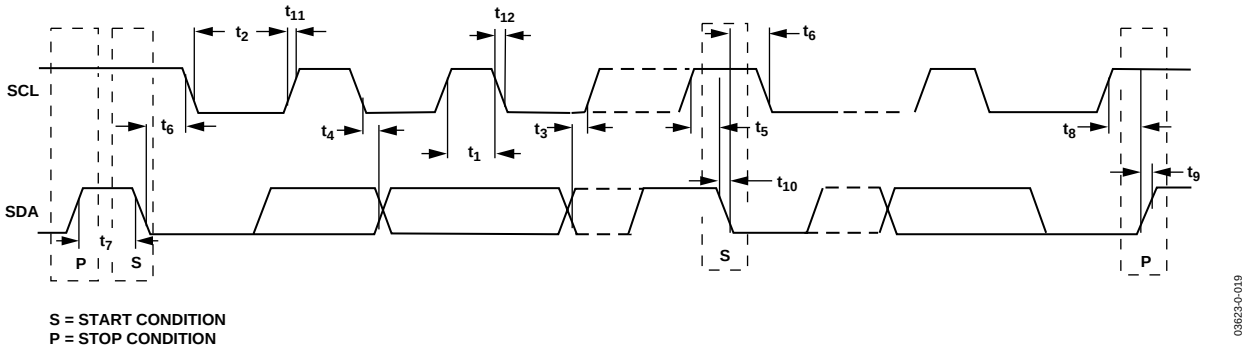


*Figure 2. Two-Wire Serial Interface Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to 7 V |
| Analog Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Reference Input Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to +7 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | |
| Commercial (B Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150° |
| Junction Temperature | 150°C |
| 10-Lead MSOP Package | |
| $\theta_{JA}$ Thermal Impedance | 200°C/W (MSOP) |
| $\theta_{JC}$ Thermal Impedance | 44°C/W (MSOP) |
| Pb/SN Temperature, Soldering Reflow (10 sec to 30 sec) | 240 (+0/−5)°C |
| Pb-Free Temperature, Soldering Reflow | 260 (+0)°C |
| ESD | 1.5 kV |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

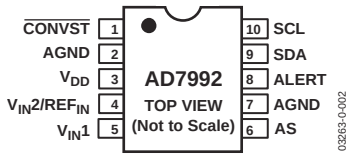


*Figure 3. AD7992 Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Function |
|---|---|---|
| 2, 7 | AGND | Analog Ground. Ground reference point for all circuitry on the AD7992. All analog input signals should be referred to this GND voltage. |
| 3 | $V_{DD}$ | Power Supply Input. The $V_{DD}$ range for the AD7992 is from 2.7 V to 5.5 V. |
| 4 | $V_{IN}2/REF_{IN}$ | Analog Input 2/Voltage Reference Input. In single-channel mode, this pin becomes the reference voltage input; an external reference should be applied at this pin. The external reference input range is 1.2 V to $V_{DD}$. A 0.1 µF and 1µF capacitor should be tied between this pin and AGND. If Bit D6 is set to 1 in the configuration register, the AD7992 operates in single-channel mode. In dual-channel mode, D6 in the configuration register is 0; in this case, this pin provides the second analog input channel. The reference voltage for the AD7992 is taken from the power supply voltage in dual-channel mode. See the Configuration Register section and Table 10. |
| 5 | $V_{IN}1$ | Analog Input 1. Single-ended analog input channel. The input range is 0 V to $REF_{IN}$. |
| 6 | AS | Logic Input. Address select input that selects one of three I²C addresses for the AD7992, as shown in Table 6. |
| 1 | $\overline{CONVST}$ | Logic Input Signal. Convert start signal. This is an edge-triggered logic input. The rising edge of this signal powers up the part. The power up time for the part is 1 µs. The falling edge of $\overline{CONVST}$ places the track-and-hold into hold mode and initiates a conversion. A power-up time of at least 1 µs must be allowed for the $\overline{CONVST}$ high pulse; otherwise, the conversion result is invalid (see the Modes of Operation section). |
| 8 | ALERT/BUSY | Digital Output. Selectable as an ALERT or BUSY output function. When configured as an ALERT, this pin acts as an out-of-range indicator and, if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Limit Registers section. When configured as a BUSY output, this pin becomes active when a conversion is in progress. Open-drain output. An external pull-up resistor is required. |
| 9 | SDA | Digital I/O. Serial bus bidirectional data. Open-drain output. An external pull-up resistor is required. |
| 10 | SCL | Digital Input. Serial bus clock. Open-drain output. An external pull-up resistor is required. |

**Table 6. I²C Address Selection**

| Part Number | AS Pin | I²C Address |
|---|---|---|
| AD7992-0 | GND | 010 0001 |
| AD7992-0 | $V_{DD}$ | 010 0010 |
| AD7992-1 | GND | 010 0011 |
| AD7992-1 | $V_{DD}$ | 010 0100 |
| AD7992-x[1] | Float | 010 0000 |

[1] If the AS pin is left floating on any of the AD7992 parts, the device address is 010 0000. This gives each AD7992 device three different address options.

# TERMINOLOGY

**Signal-to-Noise and Distortion Ratio (SINAD)**
The measured ratio of signal-to-noise and distortion at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, the SINAD is 74 dB for a 12-bit converter.

**Total Harmonic Distortion (THD)**
The ratio of the rms sum of harmonics to the fundamental. For the AD7992, it is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental, and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through sixth harmonics.

**Peak Harmonic or Spurious Noise**
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Intermodulation Distortion**
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n equal zero. For example, second-order terms include (fa + fb) and (fa − fb), while third-order terms include (2fa + fb), (2fa − fb),(fa + 2fb), and (fa − 2fb).

The AD7992 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of intermodulation distortion is, like the THD specification, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

**Channel-to-Channel Isolation**
A measure of the level of crosstalk between channels, taken by applying a full-scale sine wave signal to the unselected input channels, and determining how much the 108 Hz signal is attenuated in the selected channel. The sine wave signal applied to the unselected channels is then varied from 1 kHz up to 2 MHz, each time determining how much the 108 Hz signal in the selected channel is attenuated. This figure represents the worst-case level across all channels.

**Aperture Delay**
The measured interval between the sampling clock's leading edge and the point at which the ADC takes the sample.

**Aperture Jitter**
The sample-to-sample variation in the effective point in time when the sample is taken.

**Full-Power Bandwidth**
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

**Power Supply Rejection Ratio (PSRR)**
The ratio of the power in the ADC output at the full-scale frequency, *f*, to the power of a 200 mV p-p sine wave applied to the ADC $V_{DD}$ supply of frequency $f_S$:

$$PSRR\ (\text{dB}) = 10 \log (Pf/Pf_S)$$

where *Pf* is the power at frequency *f* in the ADC output; $Pf_S$ is the power at frequency $f_S$ coupled onto the ADC $V_{DD}$ supply.

**Integral Nonlinearity**
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

**Differential Nonlinearity**
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, AGND + 1 LSB.

**Offset Error Match**
The difference in offset error between any two channels.

**Gain Error**
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, $REF_{IN}$ − 1 LSB) after the offset error has been adjusted out.

**Gain Error Match**
The difference in gain error between any two channels.

# TYPICAL PERFORMANCE CHARACTERISTICS

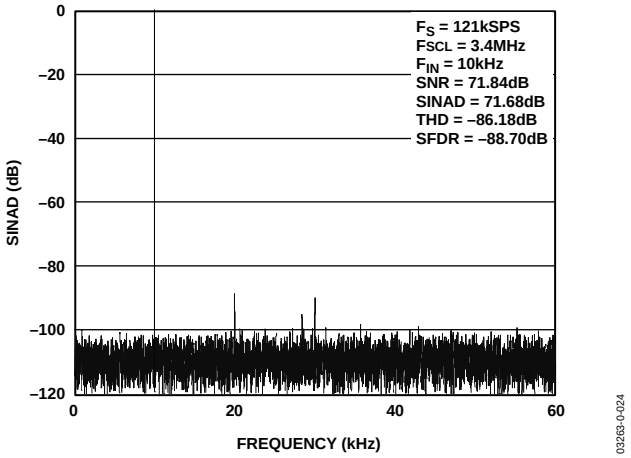


*Figure 4. Dynamic Performance with 5 V Supply and 2.5 V Reference, 121 kSPS, Mode 1, Single-Channel Mode*

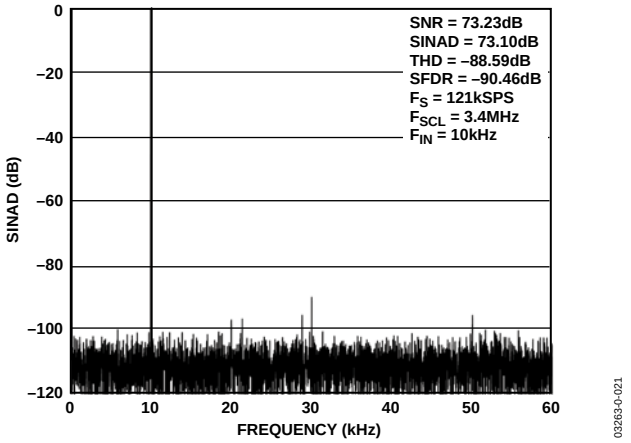


*Figure 5. Dynamic Performance with 5.5 V Supply and 5.5 V Reference, 121 KSPS, Mode 1, Dual-Channel Mode*

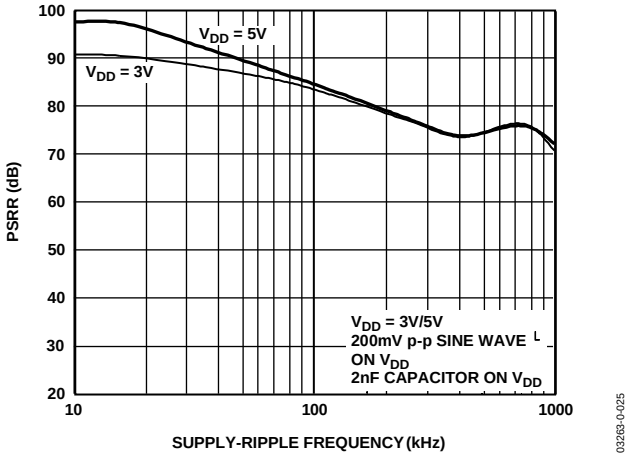


*Figure 6. PSRR vs. Supply-Ripple Frequency, Single-Channel Mode Only*

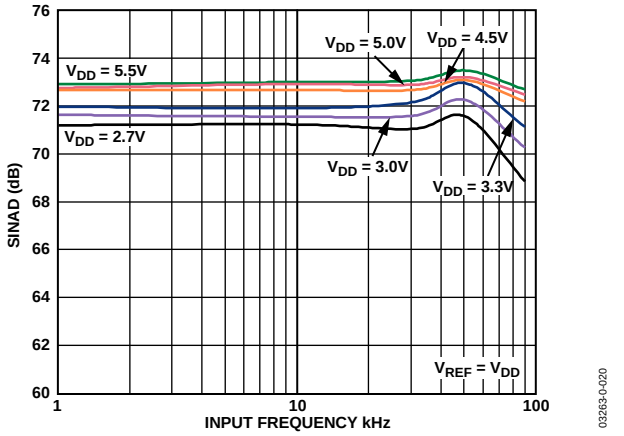


*Figure 7. SINAD vs. Analog Input Frequency for Various Supply Voltages at 136 kSPS with 3.4 MHz $f_{SCL}$*

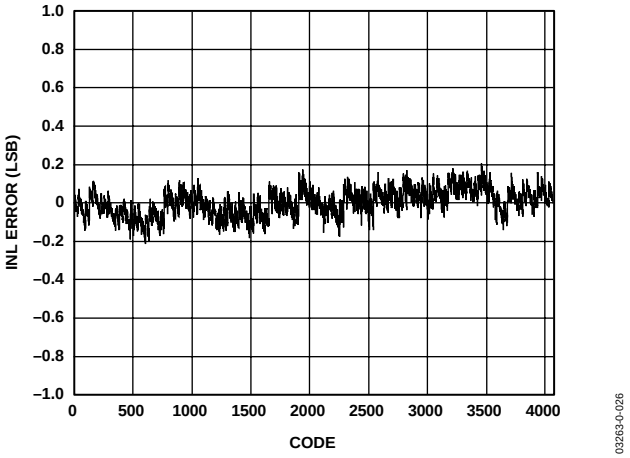


*Figure 8. Typical INL, $V_{DD}$ = 5.5 V, Reference = 2.5 V, Mode 1, 3.4 MHz $f_{SCL}$, 121 kSPS*

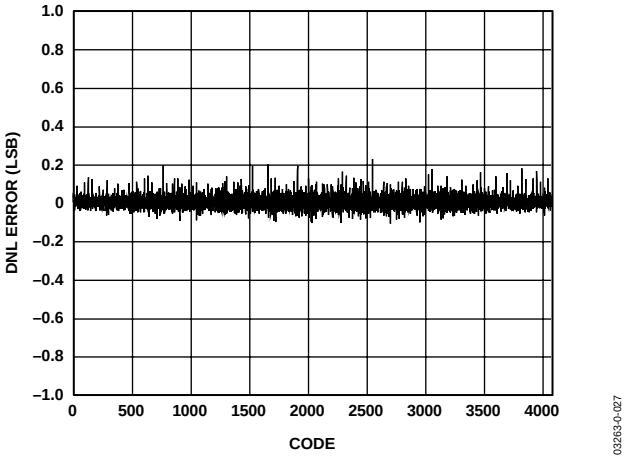


*Figure 9. Typical DNL, $V_{DD}$ = 5.5 V, Reference = 2.5 V Mode 1, 3.4 MHz $f_{SCL}$, 121 kSPS*

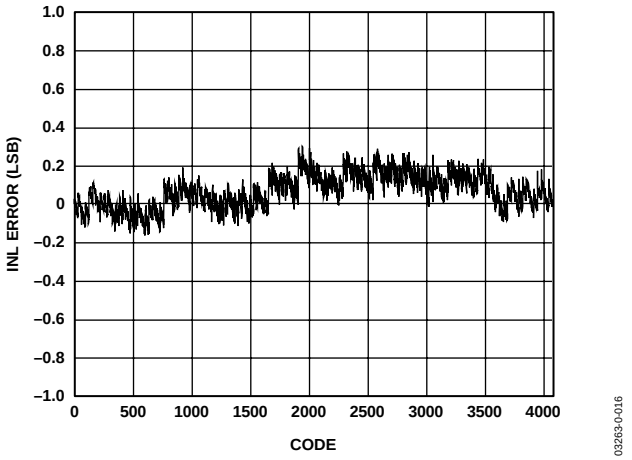


Figure 10. Typical INL, $V_{DD}$ = 2.7 V, Reference = 2.5 V, Mode1, 3.4 MHz $f_{SCL}$, 121 kSPS

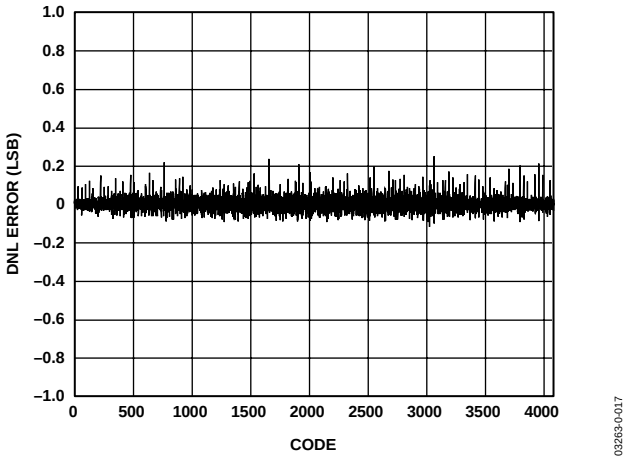


Figure 11. Typical DNL, $V_{DD}$ = 2.7 V, Reference = 2.5 V, Mode 1, 3.4 MHz $f_{SCL}$, 121 kSPS

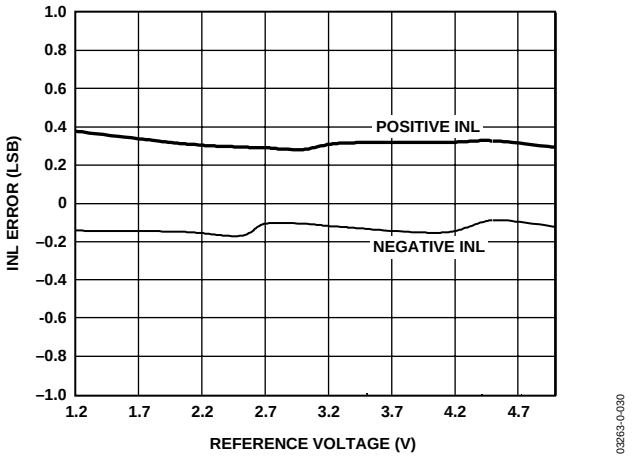


Figure 12. Change in INL vs. Reference Voltage, $V_{DD}$ = 5 V, Mode 1, 121 kSPS

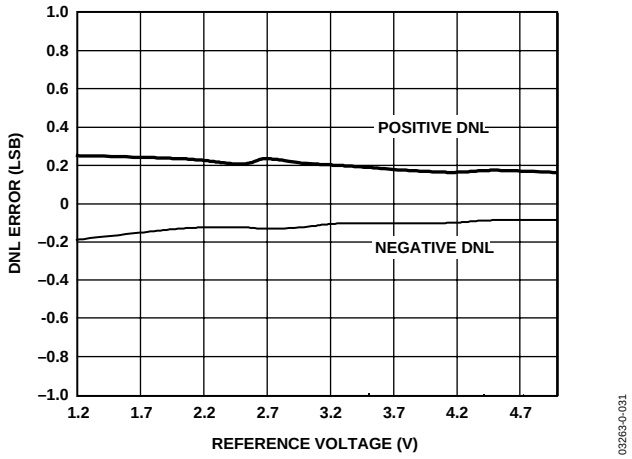


Figure 13. Change in DNL vs. Reference Voltage, $V_{DD}$ = 5 V, Mode 1, 121 kSPS

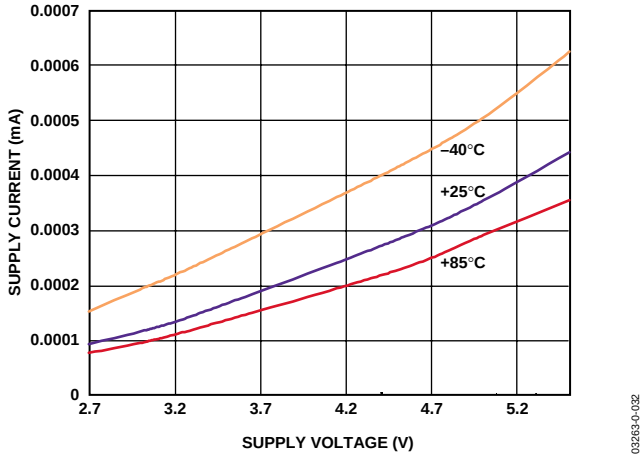


Figure 14. Shutdown Current vs. Supply Voltage, –40°C, +25°C, and +85°C

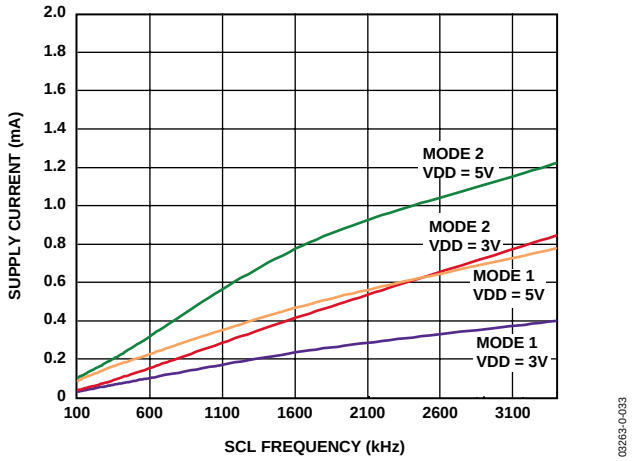


Figure 15. Average Supply Current vs. $I^2C$ Bus Rate for $V_{DD}$ = 3 V and 5 V

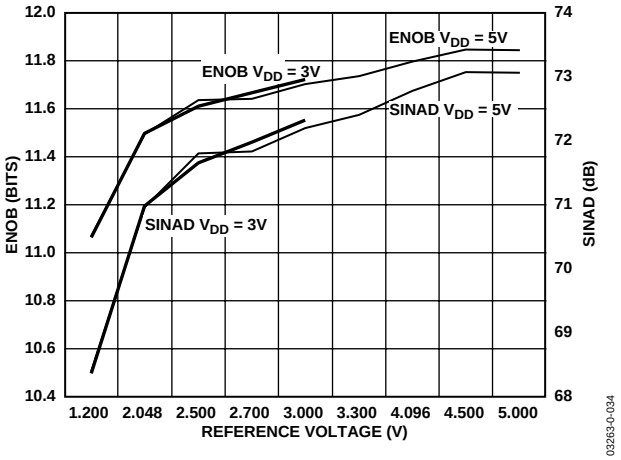


*Figure 16. ENOB/SINAD vs. Reference Voltage, Mode 1, 121 kSPS*

# CIRCUIT INFORMATION

The AD7992 is a low power, 12-bit, single-supply, 2-channel analog-to-digital converter (ADC). The part can be operated from a 2.7 V to 5.5 V supply.

The AD7992 provides the user with a 2-channel multiplexer, an on-chip track-and-hold, an ADC, an on-chip oscillator, internal data registers, and an I²C-compatible serial interface, all housed in a 10-lead MSOP package that offers the user considerable space-saving advantages over alternative solutions. The AD7992 requires an external reference in the range of 1.2 V to $V_{DD}$.

The AD7992 normally remains in a power-down state while not converting. When supplies are first applied, the part comes up in a power-down state. Power-up is initiated prior to a conversion, and the device returns to power-down upon completion of the conversion. Conversions can be initiated on the AD7992 by pulsing the $\overline{\text{CONVST}}$ signal, using an automatic cycle interval mode or a command mode where wake-up and a conversion occur during a write address function (see the Modes of Operation section). On completion of a conversion, the AD7992 again enters power-down mode. This automatic power-down feature allows power saving between conversions. This means any read or write operations across the I²C interface can occur while the device is in power-down.

## CONVERTER OPERATION

The AD7992 is a successive approximation, analog-to-digital converter based around a capacitive DAC. Figure 17 and Figure 18 show simplified schematics of the ADC during its acquisition and conversion phases, respectively. Figure 17 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on $V_{IN}$.

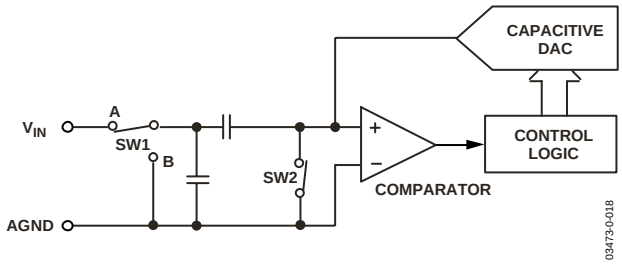


*Figure 17. ADC Acquisition Phase*

When the ADC starts a conversion, as shown in Figure 18, SW2 opens and SW1 moves to position B, causing the comparator to become unbalanced. The input is disconnected once the conversion begins. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 19 shows the ADC transfer function.

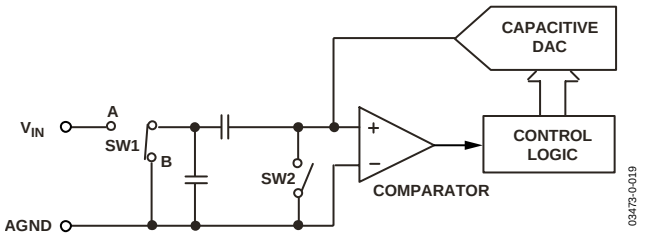


*Figure 18. ADC Conversion Phase*

### *ADC Transfer Function*

The output coding of the AD7992 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size for the AD7992 is $REF_{IN}/4096$. Figure 19 shows the ideal transfer characteristic for the AD7992.

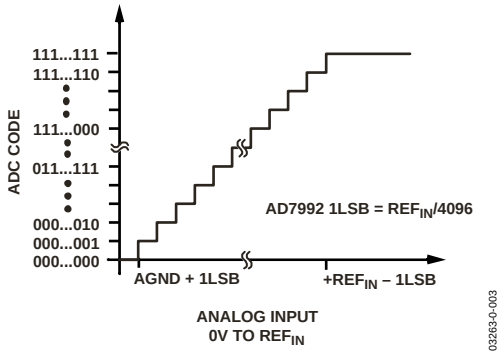


*Figure 19. AD7992 Transfer Characteristic*

## TYPICAL CONNECTION DIAGRAM

Figure 21 shows the typical connection diagram for the AD7992. In Figure 21, the address select pin (AS) is tied to $V_{DD}$; however AS can also be tied to AGND or left floating, allowing the user to select up to five AD7992 devices on the same serial bus. An external reference must be applied to the AD7992. This reference can be in the range of 1.2 V to $V_{DD}$. A precision reference like the REF 19x family, ADR03, or ADR381 can be used to supply the reference voltage to the ADC. The AD7992 can be configured to be a single-channel device with the reference voltage applied to the $V_{IN}2/REF_{IN}$ pin. The AD7992 can also be configured as a dual-channel device where the reference voltage is taken from the supply voltage $V_{DD}$, and the $V_{IN}2/REF_{IN}$ takes on its analog input function,$V_{IN}2$.

SDA and SCL form the 2-wire $I^2C$/SMBus-compatible interface. External pull-up resisters are required for both SDA and SCL lines.

The AD7992-0 supports standard and fast $I^2C$ interface modes. The AD7992-1 supports standard, fast, and high speed $I^2C$ interface modes. Therefore, if operating the AD7992 in either standard or fast mode, up to five AD7992 devices can be connected to the bus (3 × AD7992-0 and 2 × AD7992-1 or 3 × AD7992-1 and 2 × AD7992-0). In high speed mode, up to three AD7992-1 devices can be connected to the bus.

Wake up from power-down prior to a conversion is approximately 1 µs, and conversion time is approximately 2 µs. The AD7992 enters shutdown mode again after each conversion, which is useful in applications where power consumption is a concern.

## ANALOG INPUT

Figure 20 shows an equivalent circuit of the AD7992 analog input structure. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 300 mV. This causes these diodes to become forward-biased and start conducting current into the substrate. These diodes can conduct a maximum current of 10 mA without causing irreversible damage to the part.

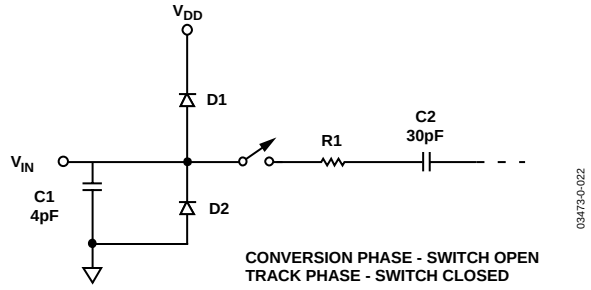


*Figure 20. Equivalent Analog Input Circuit*

Capacitor C1 in Figure 20 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance ($R_{ON}$) of a track-and-hold switch, and also the $R_{ON}$ of the input multiplexer. The total resistor is typically about 400 Ω. C2, the ADC sampling capacitor, has a typical capacitance of 30 pF.

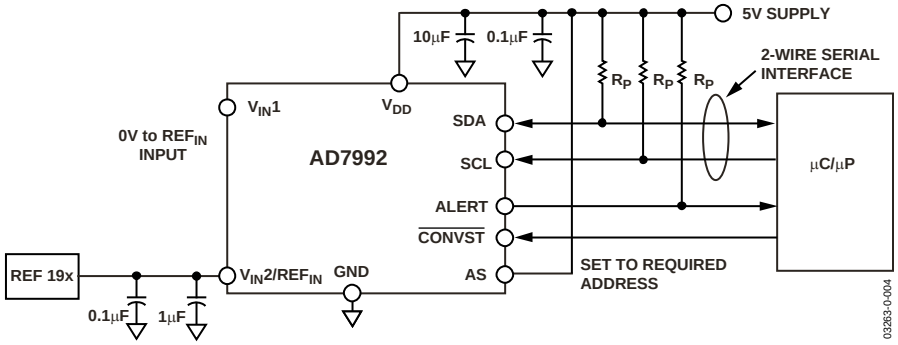


*Figure 21. AD7992 Typical Connection Diagram, Single-Channel Mode, Mode 1*

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. THD increases as the source impedance increases, and performance degrades. Figure 22 shows the THD vs. the analog input signal frequency when using supply voltages of 3 V ± 10% and 5 V ± 10%. Figure 23 shows the THD vs. the analog input signal frequency for different source impedances.

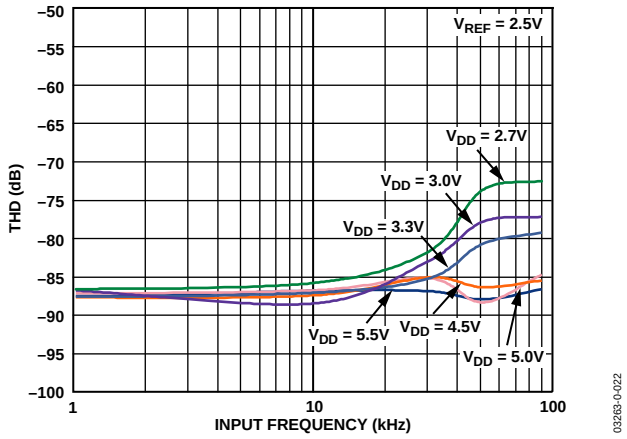


*Figure 22. THD vs. Analog Input Frequency for Various Supply Voltages, $F_S$ = 136 kSPS, Mode 1*

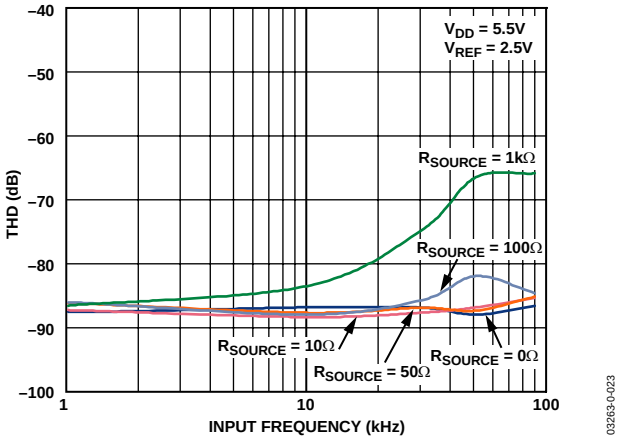


*Figure 23. THD vs. Analog Input Frequency for Various Source Impedances for $V_{DD}$ = 5.5 V, 136 kSPS, Mode 1*

# INTERNAL REGISTER STRUCTURE

The AD7992 contains 11 internal registers (see Figure 24) that are used to store conversion results, high and low conversion limits, and information to configure and control the device. There are ten data registers and one address pointer register.

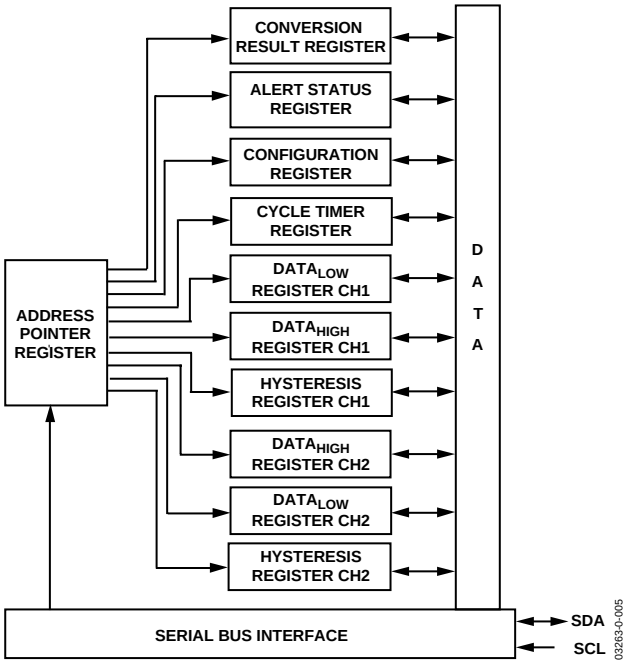


*Figure 24. AD7992 Register Structure*

Each data register has an address that the address pointer register points to when communicating with it. The conversion result register is the only data register that is read-only.

## ADDRESS POINTER REGISTER

Because it is the register to which the first data byte of every write operation is written automatically, the address pointer register does not have and does not require an address. The address pointer register is an 8-bit register in which the 4 LSBs are used as pointer bits to store an address that points to one of the AD7992's data registers. The 4 MSBs are used as command bits when operating in Mode 2 (see the Modes of Operation section). The first byte following each write address is the address of one of the data registers, which is stored in the address pointer register and selects the data register to which subsequent data bytes are written. Only the 4 LSBs of this register are used to select a data register. On power-up, the address pointer register contains all 0s, pointing to the conversion result register.

**Table 7. Address Pointer Register**

| C4 | C3 | C2 | C1 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Register select | | | |

**Table 8. AD7992 Register Addresses**

| P3 | P2 | P1 | P0 | Registers |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Conversion result register (read) |
| 0 | 0 | 0 | 1 | Alert status register (read/write) |
| 0 | 0 | 1 | 0 | Configuration register (read/write) |
| 0 | 0 | 1 | 1 | Cycle Timer register (read/write) |
| 0 | 1 | 0 | 0 | $DATA_{LOW}$ register CH1 (read/write) |
| 0 | 1 | 0 | 1 | $DATA_{HIGH}$ register CH1 (read/write) |
| 0 | 1 | 1 | 0 | Hysteresis register CH1 (read/write) |
| 0 | 1 | 1 | 1 | $DATA_{LOW}$ register CH2 (read/write) |
| 1 | 0 | 0 | 0 | $DATA_{HIGH}$ register CH2 (read/write) |
| 1 | 0 | 0 | 1 | Hysteresis register CH2 (read/write) |

## CONFIGURATION REGISTER

The configuration register is a 8-bit, read/write register that is used to set the operating modes of the AD7992. The MSB of the register is unused and is a don't care bit. The bit functions of the configuration register are outlined in Table 9. A single-byte write is necessary when writing to the configuration register.

**Table 9. Configuration Register Bit Function Descriptions and Default Settings at Power-Up**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| DONTC | Single/Dual | CH2 | CH1 | FLTR | ALERT EN | BUSY/ALERT | ALERT/BUSY POLARITY |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bit | Mnemonic | Comment |
|---|---|---|
| D7 | DONTC | Don't care bit. |
| D6 | Single/Dual | The value written to this bit determines the functionality of the $V_{IN}2/REF_{IN}$ pin and the reference source for the conversions. When this bit is 1, the pin takes on its reference input function, $REF_{IN}$, making the AD7992 a single-channel part with the reference being taken from the $REF_{IN}$ pin. However, when only Channel 1 is selected for a conversion, the reference can also be taken from the supply voltage by setting D6 to 0. When this bit is a 0, the $V_{IN}2/REF_{IN}$ pin becomes a second analog input pin, $V_{IN}2$, making the AD7992 a dual-channel part with the reference being taken from the supply voltage. See Table 10. |
| D5, D4 | CH2, CH1 | These two channel address bits select which analog input channel is to be converted. A 1 in any of Bits D5 or D4 selects a channel for conversion. If more than one channel bit is set (with D6 = 0), the alternating channel sequence is used. Table 10 shows how these two channel address bits are decoded. If D5 is selected, the part operates in dual-channel mode, with the reference for the ADC being taken from the supply voltage (D6 set to 0 for dual-channel mode). |
| D3 | FLTR | The value written to this bit of the control register determines whether the filtering on SDA and SCL is enabled or is bypassed. If this bit is a 1, the the filtering is enabled; if it is a 0, the filtering is bypassed. |
| D2 | ALERT EN | The hardware ALERT function is enabled if this bit is set to 1 and disabled if this bit is set to 0. This bit is used in conjunction with the BUSY/ALERT bit to determine if the ALERT/BUSY pin acts as an ALERT or a BUSY output (see Table 11). |
| D1 | BUSY/ALERT | This bit is used in conjunction with the ALERT EN bit to determine if the ALERT/BUSY pin acts as an ALERT or BUSY output (see Table 11), and if configured as an ALERT output pin, if it is to be reset. |
| D0 | BUSY/ALERT POLARITY | This bit determines the active polarity of the ALERT/BUSY pin regardless of whether it is configured as an ALERT or BUSY output. It is active low if this bit is set to 0 and active high if set to 1. |

**Table 10. Channel and Reference Selection**

| D6 Single/Dual | D5 CH2 | D4 CH1 | Analog Input Channel |
|---|---|---|---|
| 0 | 0 | 0 | No conversion |
| 0 | 0 | 1 | Convert on $V_{IN}1$ (reference from $V_{DD}$) |
| 1 | 0 | 1 | Convert on $V_{IN}1$ (reference from $REF_{IN}$) |
| 0 | 1 | 0 | Convert on $V_{IN}2$ (reference from $V_{DD}$) |
| 0 | 1 | 1 | Sequence between Channel 1 and Channel 2, beginning with Channel 1 (reference from $V_{DD}$) |

**Table 11. ALERT/BUSY Function**

| D2 | D1 | ALERT/BUSY Pin Configuration |
|---|---|---|
| 0 | 0 | Pin does not provide any interrupt signal. |
| 0 | 1 | Pin configured as a BUSY output. |
| 1 | 0 | Pin configured as an ALERT output. |
| 1 | 1 | Resets the ALERT output pin, the Alert_Flag bit in the conversion result register, and the entire alert status register (if any is active). If 1/1 is written to Bits D2/D1 in the configuration register to reset the ALERT pin, the Alert_Flag bit, and the alert status register, the contents of the configuration register read 1/0 for D2/D1, respectively, if read back. |

## CONVERSION RESULT REGISTER

The conversion result register is a 16-bit, read-only register that stores the conversion result from the ADC in straight binary format. A 2-byte read is needed to read data from this register.

Table 12 shows the contents of the first byte to be read from the AD7992, and Table 13 shows the contents of the second byte.

**Table 12. Conversion Value Register (First Read)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| Alert_Flag | Zero | Zero | $CH_{ID0}$ | MSB | B10 | B9 | B8 |

**Table 13. Conversion Value Register (Second Read)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

The AD7992 conversion result consists of an Alert_Flag bit, two leading zeros, a channel identifier bit, and the 12-bit data result. The Alert_Flag bit indicates whether the conversion result being read or any other channel result has violated the limit registers associated with it. If an ALERT occurs, the master may wish to read the ALERT status register to obtain more information on where the ALERT occurred if the Alert_Flag bit is set.

The Alert_Flag bit is followed by two leading zeros and a channel identifier bit that indicate to which channel the conversion result corresponds. When this bit is 0, the conversion result corresponds to $V_{IN}1$, and when it is 1, the conversion result corresponds to $V_{IN}2$. These, in turn, are followed by the 12-bit conversion result, MSB first.

## LIMIT REGISTERS

The AD7992 has two pairs of limit registers. Each pair stores high and low conversion limits for both analog input channels. Each pair of limit registers has one associated hysteresis register. All 6 registers are 16 bits wide; only the 12 LSBs of the registers are used. On power-up, the contents of the $DATA_{HIGH}$ register for each channel are full scale, while the contents of the $DATA_{LOW}$ registers are zero scale by default.

The limit registers can be used to monitor the conversion results on one or both channels. The AD7992 signals an ALERT (in either hardware or software or both, depending on the configuration) if the result moves outside the upper or lower limit set by the user.

### *$DATA_{HIGH}$ Register CH1/CH2*

The $DATA_{HIGH}$ register for a channel is a 16-bit, read/write register; only the 12 LSBs of each register are used. This register stores the upper limit that activates the ALERT output and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is greater than the value in the $DATA_{HIGH}$ register, an ALERT occurs. When the conversion result returns to a value at least N LSB below the $DATA_{HIGH}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N is taken from the 12-bit hysteresis register associated with that channel. The ALERT pin can also be reset by writing to Bits D2 and D1 in the configuration register.

**Table 14. AD7992 $DATA_{HIGH}$ Register (First Read/Write)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | B11 | B10 | B9 | B8 |

**Table 15. AD7992 $DATA_{HIGH}$ Register (Second Read/Write)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

### *$DATA_{LOW}$ Register CH1/CH2*

The $DATA_{LOW}$ register for each channel is a 16-bit read/write register; only the 12 LSB of each register are used. The register stores the lower limit that activates the ALERT output and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is less than the value in the $DATA_{LOW}$ register, an ALERT occurs. When the conversion result returns to a value at least N LSB above the $DATA_{LOW}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N is taken from the hysteresis register associated with that channel. The ALERT output pin can also be reset by writing to Bits D2 and D1 in the configuration register.

**Table 16. $DATA_{LOW}$ Register (First Read/Write)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | B11 | B10 | B9 | B8 |

**Table 17. $DATA_{LOW}$ Register (Second Read/Write)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

### *Hysteresis Register (CH1/CH2)*

Each hysteresis register is a 16-bit read/write register; only the 12 LSBs of the register are used. The hysteresis register stores the hysteresis value, N, when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin/Alert_Flag if a violation of the limits has occurred. For example, if a hysteresis value of 8 LSB is required on the upper and lower limits of Channel 1, the 16 bit word, 0000 0000 0000 1000, should be written to the hysteresis register of CH1 (see Table 8 for the address of this register). On power-up, the hysteresis registers contain a value of 8 LSB. If a different hysteresis value is required, that value must be written to the hysteresis register for the channel in question.

**Table 18. Hysteresis Register (First Read/Write)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | B11 | B10 | B9 | B8 |

**Table 19. Hysteresis Register (Second Read/Write)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

### *Using the Limit Registers to Store Min/Max Conversion Results*

If full scale—that is, all 1s—is written to the hysteresis register for a particular channel, the $DATA_{HIGH}$ and $DATA_{LOW}$ registers for that channel no longer act as limit registers as previously described, but instead act as storage registers for the maximum and minimum conversion results returned from conversions on a channel over any given period of time. This function is useful in applications where the widest span of actual conversion results is required rather than using the ALERT to signal that an intervention is necessary—for example, when monitoring temperature extremes during refrigerated goods transportation. Note that on power-up, the contents of the $DATA_{HIGH}$ register for each channel are full scale, while the contents of the $DATA_{LOW}$ registers are zero scale by default. Therefore, minimum and maximum conversion values being stored in this way are lost if power is removed or cycled.

## ALERT STATUS REGISTER

The alert status register is an 8-bit read/write register that provides information on an alert event. If a conversion results in activating the ALERT pin or Alert_Flag bit in the conversion result register (see the Limit Registers section) the alert status register may be read to gain further information. It contains two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits. The bit with a status of 1 shows where the violation occurred—that is, on which channel—and whether the violation occurred on the upper or lower limit. If a second alert event occurs on the other channel between receiving the first alert and interrogating the alert status register, the corresponding bit for that alert event is also set.

The entire contents of the alert status register can be cleared by writing 1,1 to Bits D2 and D1 in the configuration register, as shown in Table 11. This can also be achieved by writing all 1s to the alert status register itself. Thus, if the alert status register is addressed for a write operation, which is all 1s, the contents of the alert status register are cleared or reset to all 0s.

**Table 20. Alert Status Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $CH2_{HI}$ | $CH2_{LO}$ | $CH1_{HI}$ | $CH1_{LO}$ |

**Table 21. Alert Status Register Bit Function Descriptions**

| Bit | Mnemonic | Comment |
|---|---|---|
| D0 | CH1LO | Violation of $DATA_{LOW}$ limit on Channel 1 if bit is set to 1, no violation if bit is set to 0. |
| D1 | CH1HI | Violation of $DATA_{HIGH}$ limit on Channel 1 if bit is set to 1, no violation if bit is set to 0. |
| D2 | CH2LO | Violation of $DATA_{LOW}$ limit on Channel 2 if bit is set to 1, no violation if bit is set to 0. |
| D3 | CH2HI | Violation of $DATA_{HIGH}$ limit on Channel 2 if bit is set to 1, no violation if bit is set to 0. |

## CYCLE TIMER REGISTER

The cycle timer register is an 8-bit read/write register that stores the conversion interval value for the automatic cycle mode of the AD7992 (see the Modes of Operation section). The 5 MSBs of the cycle timer register are unused and should contain 0s at all times (see the Sample Delay and Bit Trial Delay section). On power-up, the cycle timer register contains all 0s, thus disabling automatic cycle operation of the AD7992. To enable automatic cycle mode, the user must write to the cycle timer register, selecting the required conversion interval. Table 22 shows the structure of the cycle timer register, while Table 23 shows how the bits in this register are decoded to provide various automatic sampling intervals.

**Table 22. Cycle Timer Register and Defaults at Power-Up**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Sample Delay | Bit Trial Delay | 0 | 0 | 0 | Cyc Bit 2 | Cyc Bit 1 | Cyc Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 23. Cycle Timer Intervals**

| CYC Reg Value | | | Conversion Interval |
|---|---|---|---|
| D2 | D1 | D0 | ($T_{CONVERT}$ =conversion time of ADC) |
| 0 | 0 | 0 | Mode not selected |
| 0 | 0 | 1 | $T_{CONVERT} \times 32$ |
| 0 | 1 | 0 | $T_{CONVERT} \times 64$ |
| 0 | 1 | 1 | $T_{CONVERT} \times 128$ |
| 1 | 0 | 0 | $T_{CONVERT} \times 256$ |
| 1 | 0 | 1 | $T_{CONVERT} \times 512$ |
| 1 | 1 | 0 | $T_{CONVERT} \times 1024$ |
| 1 | 1 | 1 | $T_{CONVERT} \times 2048$ |

## SAMPLE DELAY AND BIT TRIAL DELAY

It is recommended that no $I^2C$ bus activity occurs when a conversion is taking place. However, this may not be possible, for example, when operating in Mode 2 or the automatic cycle mode. In order to maintain the performance of the ADC in such cases, Bits D7 and D6 in the cycle timer register are used to delay critical sample intervals and bit trials from occurring while there is activity on the $I^2C$ bus. This may have the effect of increasing the conversion time. When Bits D7 and D6 are both 0, the bit trial and sample interval delaying mechanism are implemented. The default setting of D7 and D6 is 0. If bit trial delays extend longer than 1 μs, the conversion terminates. When D7 is 0, the sampling instant delay is implemented. When D6 is 0, the bit trial delay is implemented. To turn off both the sample delay and bit trial delay, set D7 and D6 to 1.

# SERIAL INTERFACE

Control of the AD7992 is carried out via the I²C-compatible serial bus. The AD7992 is connected to this bus as a slave device under the control of a master device, such as the processor.

## SERIAL BUS ADDRESS

Like all I²C-compatible devices, the AD7992 has a 7-bit serial address. The 3 MSBs of this address for the AD7992 are set to 010. The device comes in two versions, the AD7992-0 and the AD7992-1. The two versions have three different I²C addresses available, which are selected by either tying the address select pin, AS, to AGND or $V_{DD}$, or by letting the pin float (refer to Table 6). By giving different addresses for the two versions, up to five AD7992 devices can be connected to a single serial bus, or the addresses can be set to avoid conflicts with other devices on the bus.

The serial bus protocol operates as follows.

The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA, while the serial clock line, SCL, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer—that is, whether data is written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the receiver of data. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a STOP signal.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a STOP condition. In read mode, the master device pulls the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

# WRITING TO THE AD7992

Depending on the register being written to, there are three different writes for the AD7992.

## WRITING TO THE ADDRESS POINTER REGISTER FOR A SUBSEQUENT READ

In order to read from a particular register, the address pointer register must first contain the address of that register. If it does not, the correct address must be written to the address pointer register by performing a single-byte write operation, as shown in Figure 25. The write operation consists of the serial bus address followed by the address pointer byte. No data is written to any of the data registers. A read operation can be subsequently performed to read the register of interest.

## WRITING A SINGLE BYTE OF DATA TO THE ALERT STATUS REGISTER, CYCLE REGISTER, OR CONFIGURATION REGISTER

The alert status register, cycle register, and configuration register are all 8-bit registers, so only one byte of data can be written to each. Writing a single byte of data to one of these registers consists of the serial bus write address, the chosen data register address written to the address pointer register, followed by the data byte written to the selected data register. See Figure 26.

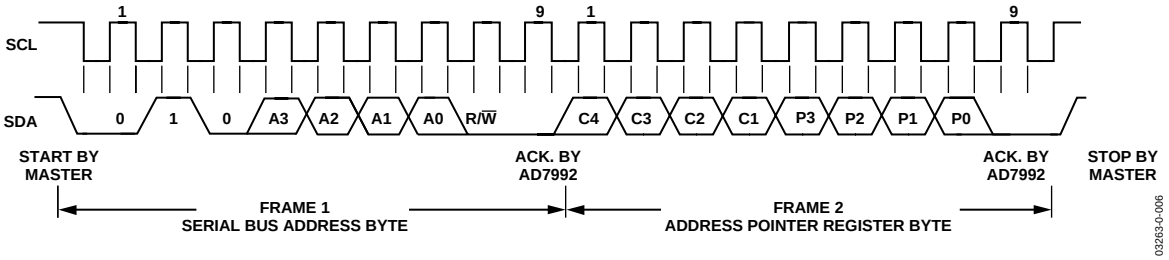


*Figure 25. Writing to the Address Pointer Register to Select a Register for a Subsequent Read Operation*

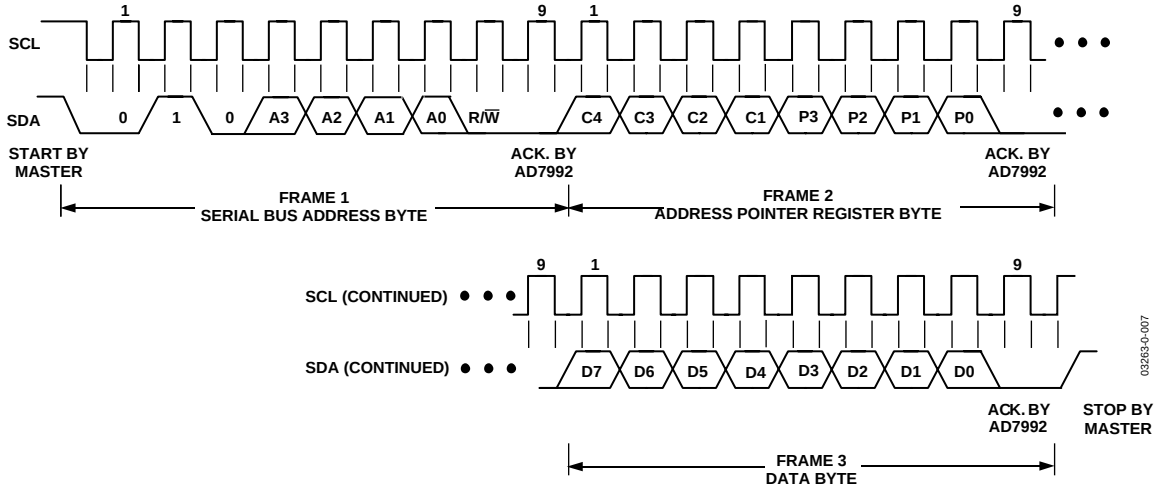


*Figure 26. Single-Byte Write Sequence*

## WRITING TWO BYTES OF DATA TO A LIMIT REGISTER OR HYSTERESIS REGISTER

Each of the limit registers and hysteresis registers are 12-bit registers, so two bytes of data are required to write a value to any one of them. Writing two bytes of data to one of these registers consists of the serial bus write address, the chosen limit register address written to the address pointer register, followed by two data bytes written to the selected data register. See Figure 27.

If the master is write-addressing the AD7992, it can write to more than one register with out re-addressing the ADC. After the first write operation has completed for the first data register, during the next byte, the master writes to the address pointer byte to select the next data register for a write operation. This eliminates the need to re-address the device in order to write to another data register.

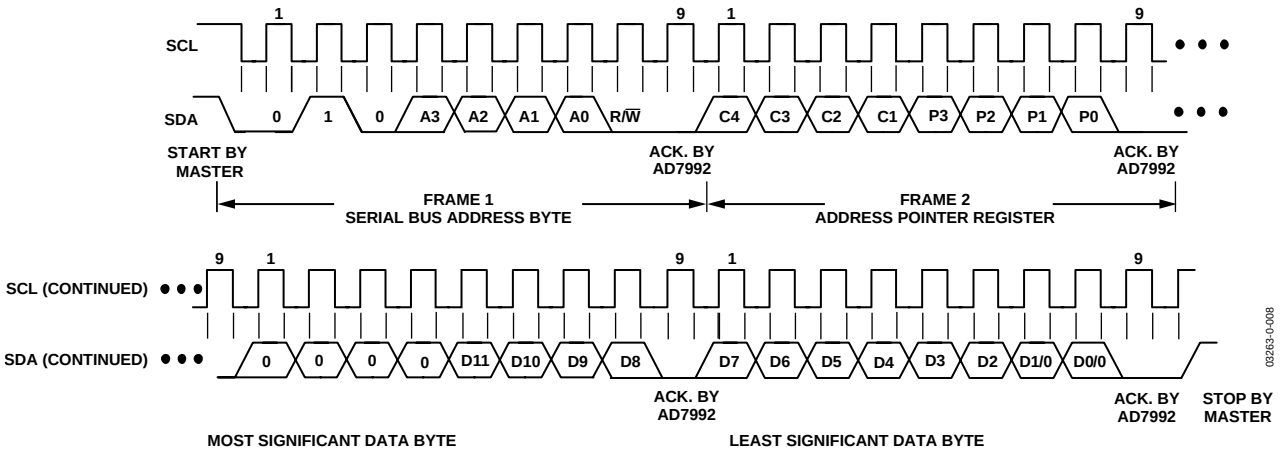


*Figure 27. Two-Byte Write Sequence*

# READING DATA FROM THE AD7992

Reading data from the AD7992 is a 1- or 2-byte operation. Reading back the contents of the alert status register, the configuration register, or the cycle timer register is a single-byte read operation, as shown in Figure 28. This assumes the particular register address has previously been set up by a single-byte write operation to the address pointer register (see Figure 25). Once the register address has been set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. If a read from a different register is required, the relevant register address has to be written to the address pointer register, and again any number of reads from this register may then be performed.

Reading data from the conversion result register, $DATA_{HIGH}$ registers, $DATA_{LOW}$ registers, or hysteresis registers is a 2-byte operation, as shown in Figure 29. The same rules apply for a 2-byte read as a 1-byte read.

When reading data back from a register, such as the conversion result register, if more than two read bytes are supplied, the same or new data is read from the AD7992 without the need to re-address the device. This allows the master to continuously read from a data register without having to re-address the AD7992.

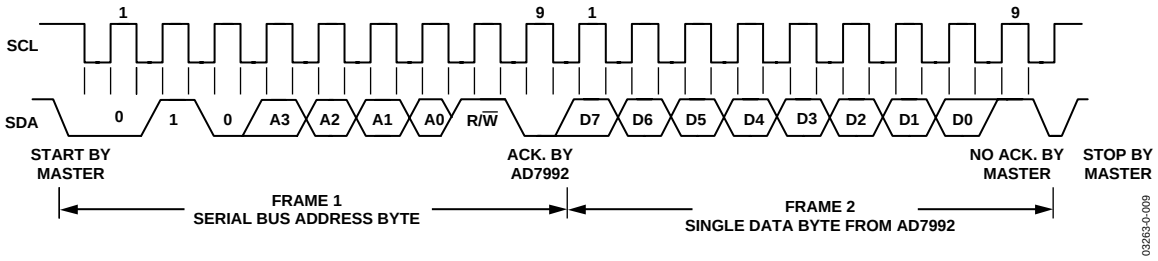


*Figure 28. Reading a Single Byte of Data from a Selected Register*

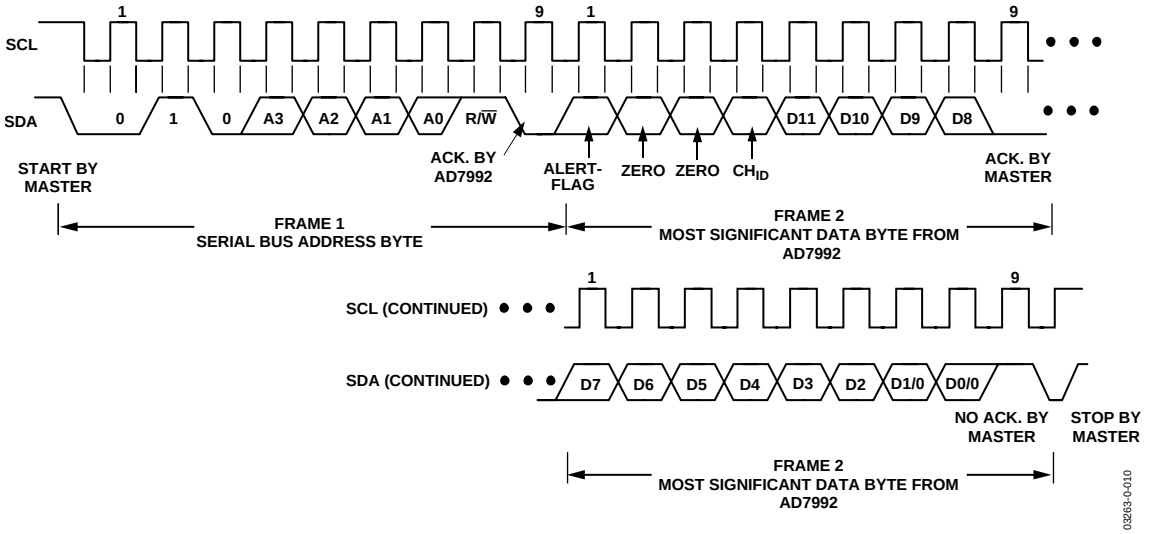


*Figure 29. Reading Two Bytes of Data from the Conversion Result Register*

# ALERT/BUSY PIN

The ALERT/BUSY pin may be configured as an ALERT output or BUSY output, as shown in Table 11.

## SMBus ALERT

The AD7992 ALERT output is an SMBus interrupt line for devices that want to trade their ability to master for an extra pin. The AD7992 is a slave-only device and uses the SMBus ALERT to signal the host device that it wants to talk. The SMBus ALERT on the AD7992 is used as an out-of-conversion-range indicator (a limit violation indicator).

The ALERT pin has an open-drain configuration that allows the ALERT outputs of several AD7992s to be wire-AND'ed together when the ALERT pin is active low. D0 of the configuration register is used to set the active polarity of the ALERT output. The power-up default is active low. The ALERT function can be disabled or enabled by setting D2 of the configuration register to 0 or 1, respectively.

The host device can process the ALERT interrupt and simultaneously access all SMBus ALERT devices through the alert response address. Only the device that pulled the ALERT low acknowledges the ARA (alert response address). If more than one device pulls the ALERT pin low, the highest priority (lowest address) device wins communication rights via standard $I^2C$ arbitration during the slave address transfer.

The ALERT output becomes active when the value in the conversion result register exceeds the value in the $DATA_{HIGH}$ register or falls below the value in the $DATA_{LOW}$ register for a selected channel. It is reset when a write operation to the configuration register sets D1 to a 1, or when the conversion result returns N LSBs below or above the value stored in the $DATA_{HIGH}$ register or $DATA_{LOW}$ register, respectively. N is the value in the hysteresis register (see the Limit Registers section).

The ALERT output requires an external pull-up resistor that can be connected to a voltage different from $V_{DD}$ provided the maximum voltage rating of the ALERT output pin is not exceeded. The value of the pull-up resistor depends on the application, but should be as large as possible to avoid excessive sink currents at the ALERT output.

## PLACING THE AD7992-1 INTO HIGH SPEED MODE

High speed mode communication commences after the master addresses all devices connected to the bus with the master code, 00001XXX, to indicate that a high speed mode transfer is to begin. No device connected to the bus is allowed to acknowledge the high speed master code; therefore, the code is followed by a not acknowledge (see Figure 30). The master must then issue a repeated start followed by the device address with a R/$\overline{W}$ bit. The selected device then acknowledges its address.

All devices continue to operate in high speed mode until the master issues a STOP condition. When the STOP condition is issued, the devices all return to fast mode.

## THE ADDRESS SELECT (AS) PIN

The address select pin on the AD7992 is used to set the $I^2C$ address for the AD7992 device. The AS pin can be tied to $V_{DD}$, to AGND, or left floating. The selection should be made as close as possible to the AS pin; avoid having long tracks introducing extra capacitance onto the pin. This is important for the float selection, because the AS pin has to charge to a midpoint after the start bit during the first address byte. Extra capacitance on the AS pin increases the time taken to charge to the midpoint and may cause an incorrect decision on the device address. When the AS pin is left floating, the AD7992 can work with a capacitive load up to 40 pF.

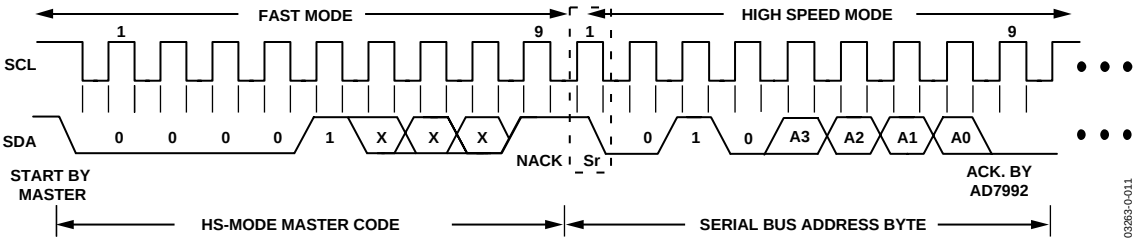


*Figure 30. Placing the Part into High Speed Mode*

# MODES OF OPERATION

When supplies are first applied to the AD7992, the ADC powers up in sleep mode and normally remains in this shutdown state while not converting. There are three different methods of initiating a conversion on the AD7992.

## MODE 1—USING THE $\overline{\text{CONVST}}$ PIN

A conversion can be initiated on the AD7992 by pulsing the $\overline{\text{CONVST}}$ signal. The conversion clock for the part is internally generated so no external clock is required, except when reading from or writing to the I²C serial port. On the rising edge of $\overline{\text{CONVST}}$, the AD7992 begins to power up (see point A in Figure 31). The power-up time from shutdown mode for the AD7992 is approximately 1 µs; the $\overline{\text{CONVST}}$ signal must remain high for 1 µs for the part to power up fully. $\overline{\text{CONVST}}$ can be brought low after this time. The falling edge of the $\overline{\text{CONVST}}$ signal places the track-and-hold into hold mode; a conversion is also initiated at this point (point B in Figure 31). When the conversion is complete, approximately 2 µs later, the part returns to shutdown (point C in Figure 31) and remains there until the next rising edge of $\overline{\text{CONVST}}$. The master can then read the ADC to obtain the conversion result. The address pointer register must be pointing to the conversion result register in order to read back the conversion result.

If the $\overline{\text{CONVST}}$ pulse does not remain high for more than 1 µs, the falling edge of $\overline{\text{CONVST}}$ still initiates a conversion, but the result is invalid because the AD7992 is not fully powered up when the conversion takes place. To maintain the performance of the AD7992 in this mode, it is recommended that the I²C bus is quiet when a conversion is taking place.

The cycle timer register and Command Bits C4 to C1 in the address pointer register should contain all 0s when operating the AD7992 in this Mode 1. The $\overline{\text{CONVST}}$ pin should be tied low for all other modes of operation. Prior to initiating a conversion in this mode, a write to the configuration register is needed to select the channel for conversion. To select both input channels for conversion, set D5 and D4 in the configuration register to 1. The ADC services each channel in the sequence with each $\overline{\text{CONVST}}$ pulse.

Once the conversion is complete, the master can address the AD7992 to read the conversion result. If further conversions are required, the SCL line can be taken high while the $\overline{\text{CONVST}}$ signal is pulsed; then an additional 18 SCL pulses are required to read the next conversion result.

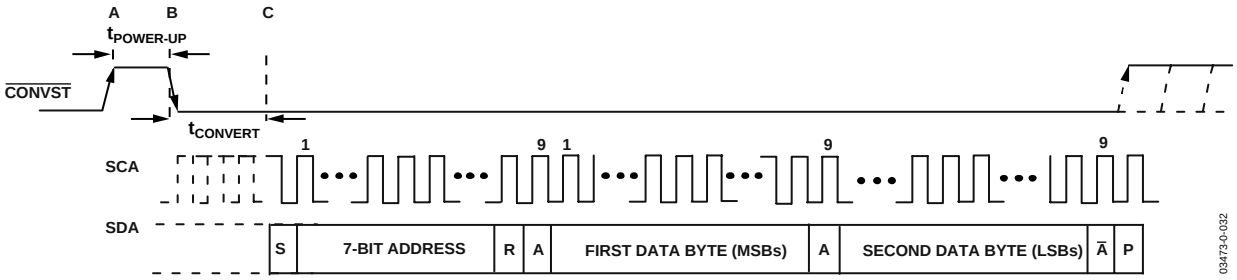


*Figure 31. Mode 1 Operation*

## MODE 2 – COMMAND MODE

Mode 2 allows a conversion to be automatically initiated any time a write operation occurs. In order to use this mode, Command Bits C2 to C1 in the address pointer byte, shown in Table 7, must be programmed. Command Bits C4 and C3 are not used and should contain zeros at all times.

To select a channel for conversion in Mode 2, set the corresponding channel command bit in the address pointer byte (see Table 24). To select both analog input channels for conversion, set both C1 and C2 to 1. When all four command bits are 0, this mode is not used.

Figure 28 illustrates a 2-byte read operation from the conversion result register. Prior to the read operation, ensure that the address pointer is pointing to the conversion result register. When the contents of the address pointer register are being loaded, if Command Bits C2 or C1 are set, the AD7992 begins to power up and convert upon the selected channel(s). Power-up begins on the fifth SCL falling edge of the address point byte (see point A in Figure 32). Table 24 shows the channel selection in this mode via Command Bits C1 and C2 in the address pointer register. The wake-up and conversion time together should take approximately 3 µs, and the conversion begins when the last Command Bit, C1, has been clocked in midway through the write to the address pointer register. Following this, the AD7992 must be addressed again to tell it that a read operation is required. The read then takes place from the conversion result register. This read accesses the result from the conversion selected via the command bits. If Command Bits C2, C1 are set to 1,1, a 4-byte read is necessary. The first read accesses the data from the conversion on $V_{IN}1$. While this read takes place, a conversion occurs on $V_{IN}2$. The second read accesses this data from $V_{IN}2$. Figure 33 shows how this mode operates.

After the conversion result has been read, and if further read bytes are issued, the ADC continuously converts on the selected input channel(s). This has the effect of increasing the overall throughput rate of the ADC.

When operating the AD7992-1 in Mode 2 with high speed mode, 3.4 MHz SCL, the conversion may not be complete before the master tries to read the conversion result. In this case, the AD7992-1 holds the SCL line low during the ACK clock after the read address until the conversion is complete. When the conversion is complete, the AD7992-1 releases the SCL line and the master can then read the conversion result.

After a conversion is initiated in this mode by setting the command bits in the address pointer byte, if the AD7992 receives a STOP or NACK from the master, the AD7992 stops converting.

**Table 24. Address Pointer Byte—Command Bits**

| C2 | C1 | Analog Input Channel |
|---|---|---|
| 0 | 0 | No conversion |
| 0 | 1 | Conversion on $V_{IN}1$ |
| 1 | 0 | Conversion on $V_{IN}2$ |
| 1 | 1 | Conversion on $V_{IN}1$ followed by conversion on $V_{IN}2$ |

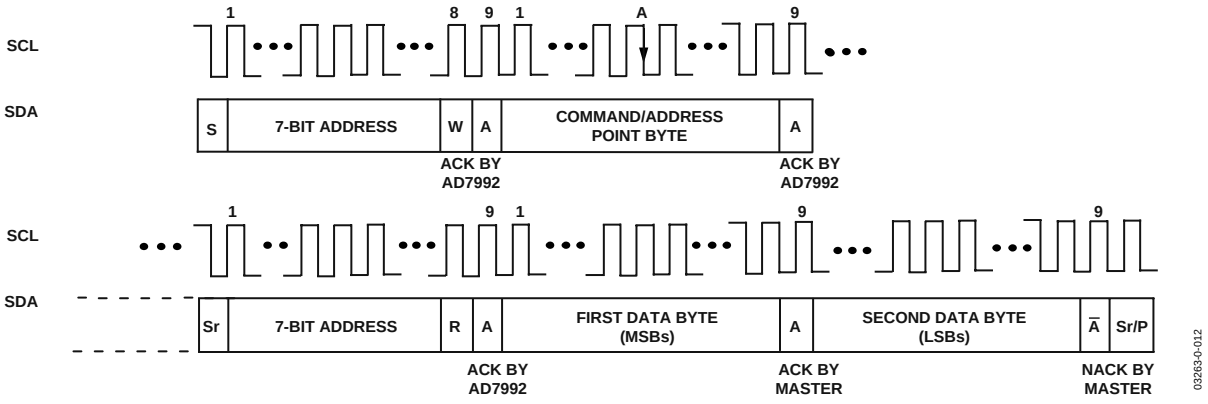


*Figure 32. Mode 2 Operation*

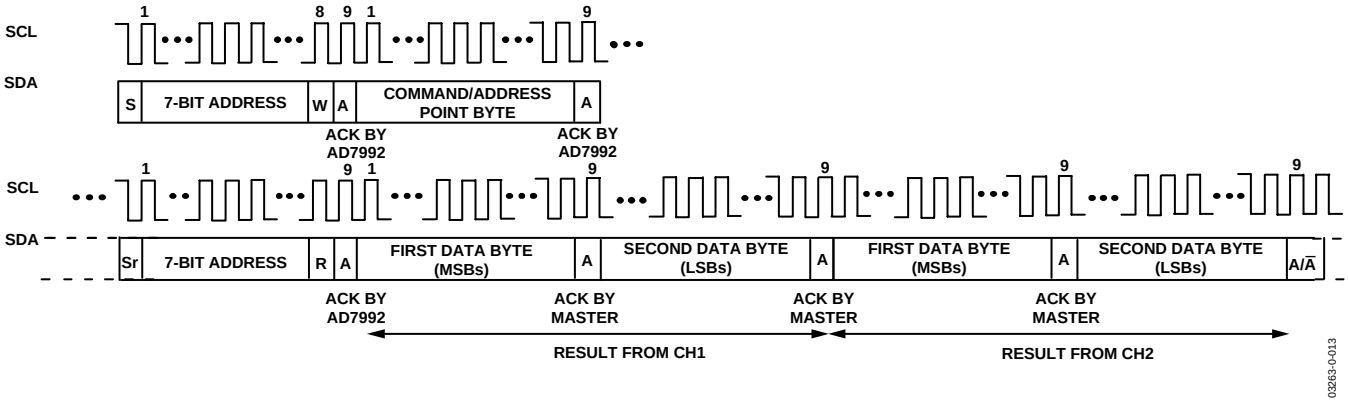


*Figure 33. Mode 2 Sequence Operation*

## MODE 3—AUTOMATIC CYCLE MODE

An automatic conversion cycle can be selected and enabled by writing a value to the cycle timer register. A conversion cycle interval can be set up on the AD7992 by programming the relevant bits in the 8-bit cycle timer register, as decoded in Table 23. Only the 3 LSBs are used; the 5 MSBs should contain 0s (see the Sample Delay and Bit Trial Delay section). When the 3 LSBs of the register are programmed with any configuration other than all 0s, a conversion takes place every X ms; the cycle interval, X, depends on the configuration of these three bits in the cycle timer register. There are seven different cycle time intervals to choose from, as shown in Table 23. Once the conversion has taken place, the part powers down again until the next conversion occurs. To exit this mode of operation, the user must program the 3 LSBs of the cycle timer register to contain all 0s. For cycle interval options, see Table 23.

To select a channel(s) for operation in cycle mode, set the corresponding channel bit(s), D5 to D4, of the configuration register. If more than one channel bit is set in the configuration register, the ADC automatically cycles through the channel sequence, starting with the lowest channel. Once the sequence is complete, the ADC starts converting on the lowest channel again, continuing to loop through the sequence until the cycle timer register contents are set to all 0s. This mode is useful for monitoring signals, such as battery voltage and temperature, alerting only when the limits are violated.