HMC694LP4 / 694LP4E

v02.1108

GaAs MMIC ANALOG VARIABLE GAIN AMPLIFIER, 6 - 17 GHz

Typical Applications

The HMC694LP4(E) is ideal for:

- Point-to-Point Radio
- Point-to-Multi-Point Radio
- EW & ECM
- X-Band Radar
- Test Equipment

Features

Wide Gain Control Range: 23 dB

Single Control Voltage

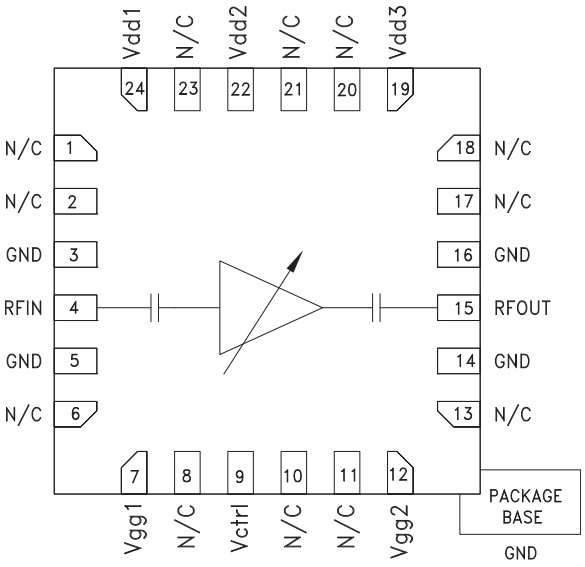
Output IP3 @ Max Gain: +30 dBm

Output P1dB: +22 dBm

No External Matching

24 Lead 4x4 mm SMT Package: 16 mm^2

Functional Diagram



General Description

The HMC694LP4(E) is a GaAs MMIC PHEMT analog variable gain amplifier which operates between 6 and 17 GHz. Ideal for microwave radio applications, the amplifier provides up to 22 dB of gain, output P1 dB of up to +22 dBm, and up to +30 dBm of output IP3 at maximum gain, while requiring only 175 mA from a +5V supply. A gate bias pin (Vctrl) is provided to allow variable gain control up to 23 dB. Gain flatness is excellent making the HMC694LP4E ideal for EW, ECM and radar applications. The HMC694LP4E is housed in a RoHS compliant 4x4 mm QFN leadless package and is compatible with high volume surface mount manufacturing.

Electrical Specifications, T_A = +25°C, Vdd1, 2, 3= 5V, Vctrl= -2V, Idd= 170 mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		6 - 10			10 - 17		GHz
Gain	19	22		14	18		dB
Gain Flatness		±1			±1.5		dB
Gain Variation Over Temperature		0.015			0.015		dB/ °C
Gain Control Range		23			20		dB
Noise Figure		6	7.5		6	6.5	dB
Input Return Loss		15			8		dB
Output Return Loss		10			8		dB
Output Power for 1 dB Compression (P1dB)	19	21		21	22		dBm
Saturated Output Power (Psat)		22			23		dBm
Output Third Order Intercept (IP3)		30			30		dBm
Total Supply Current (Idd)		175			175		mA

*Set Vctrl = -2V and then adjust Vgg1, 2 between -2V to 0V (typ. -0.8V) to achieve Idd = 170mA typical.

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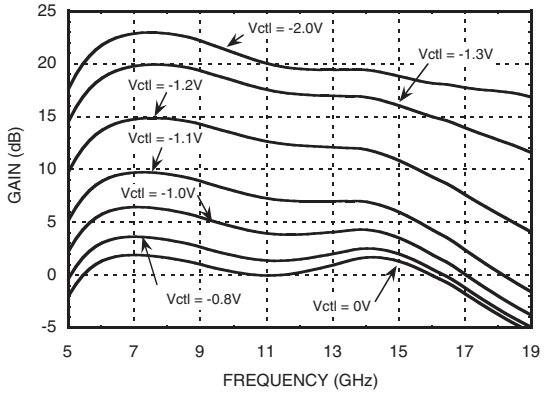
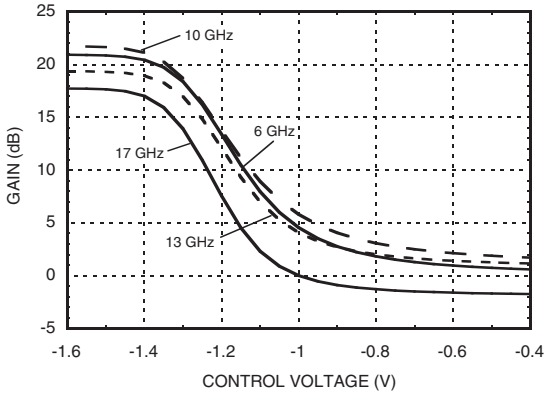
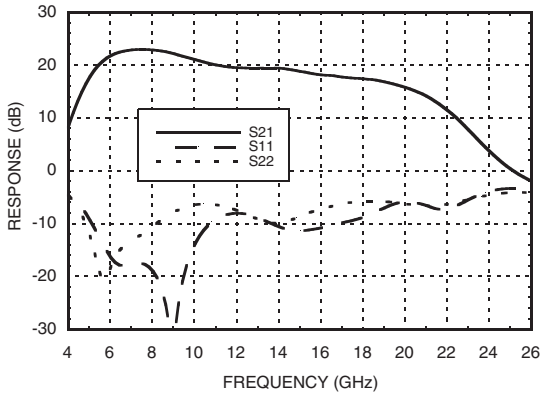
Control Voltage Range vs. Gain



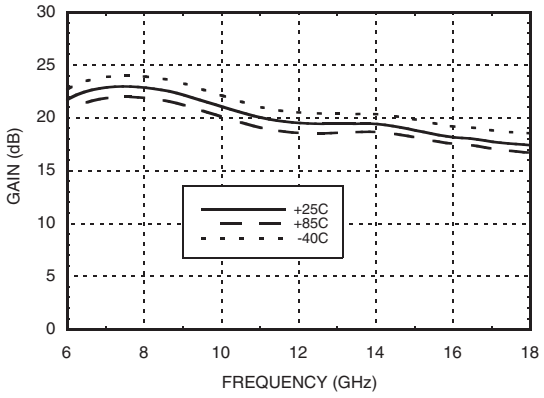
Gain vs. Control Voltage



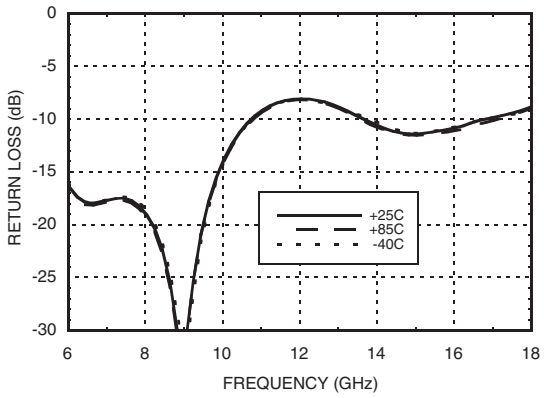
Broadband Gain & Return Loss



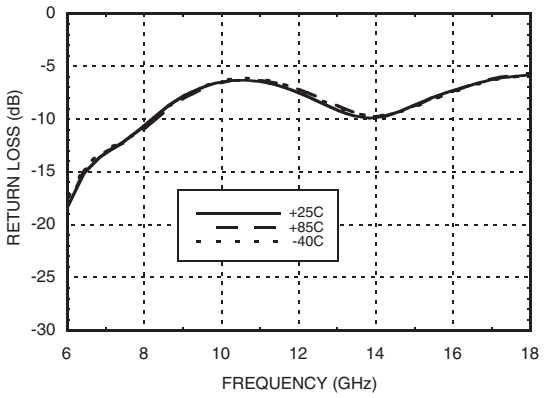
Gain vs. Temperature



Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



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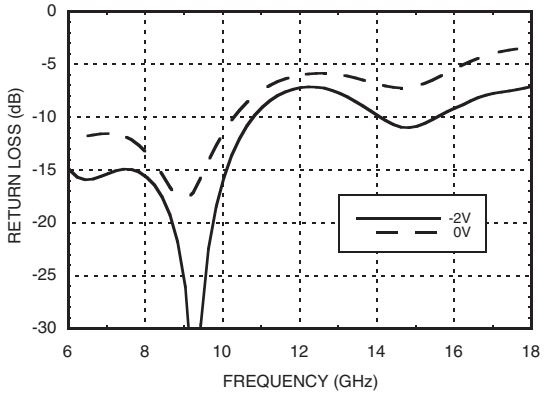
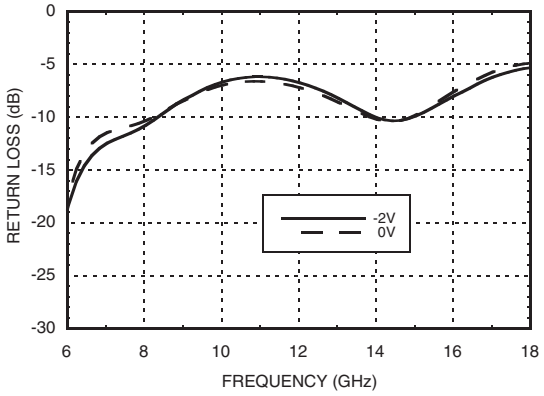
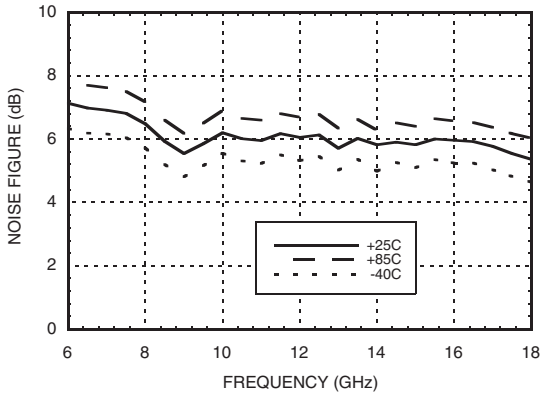
Return Loss @ Voltage Extreme



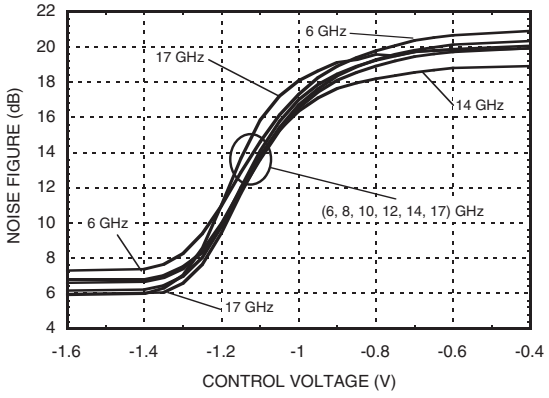
Output Return Loss @ Voltage Extreme



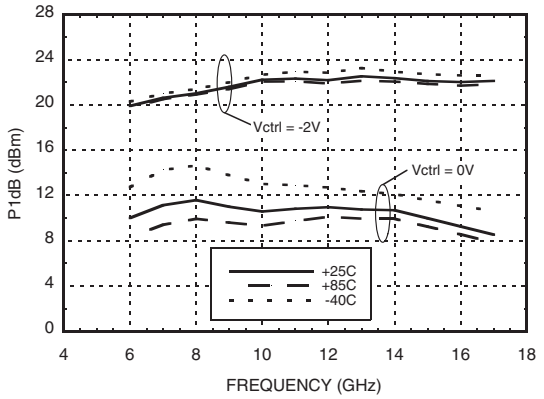
Noise Figure vs. Temperature



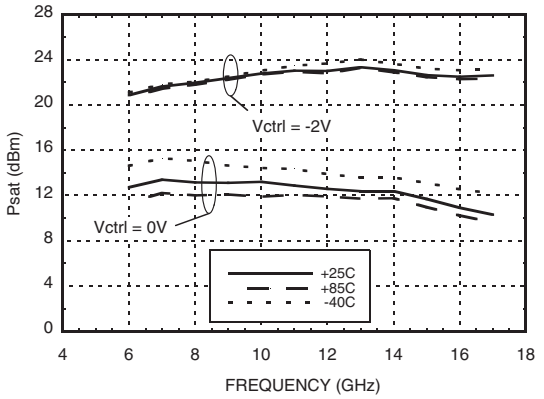
Noise Figure vs. CTRL



P1dB vs. Temperature



Psat vs. Temperature



[1] Tested with broadband bias tee on RF ports and C1 = 10,000pF
[2] C1, C6 and C8 = 100pF, L1 = 24nF

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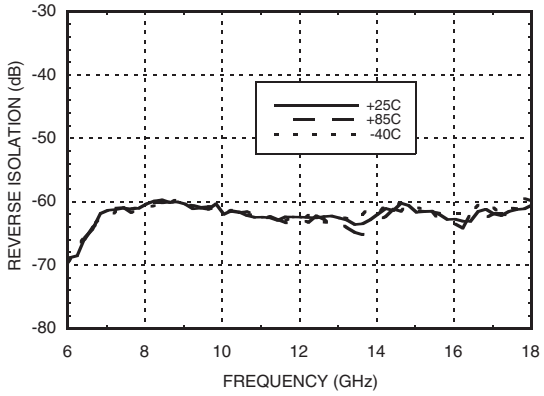
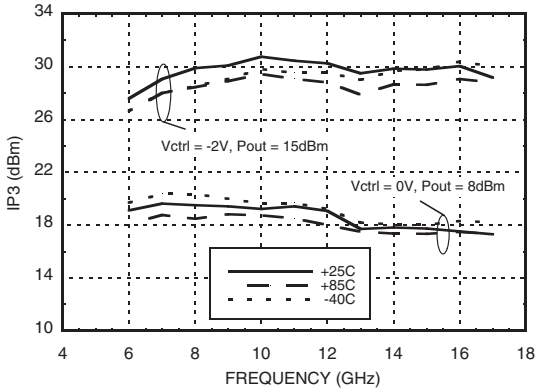
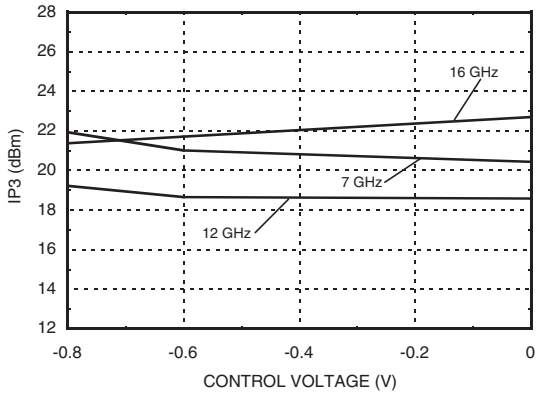
Reverse Isolation vs. Temperature



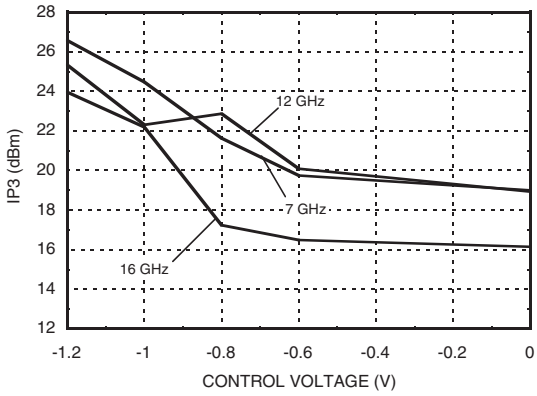
Output IP3 vs. Temperature



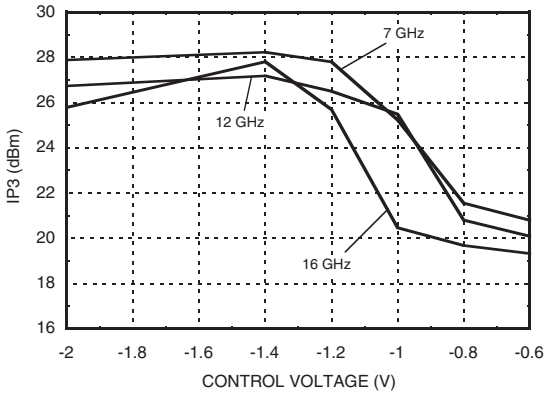
Output IP3 @ 0 dBm



Output IP3 @ 5 dBm



Output IP3 @ 10 dBm



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Absolute Maximum Ratings

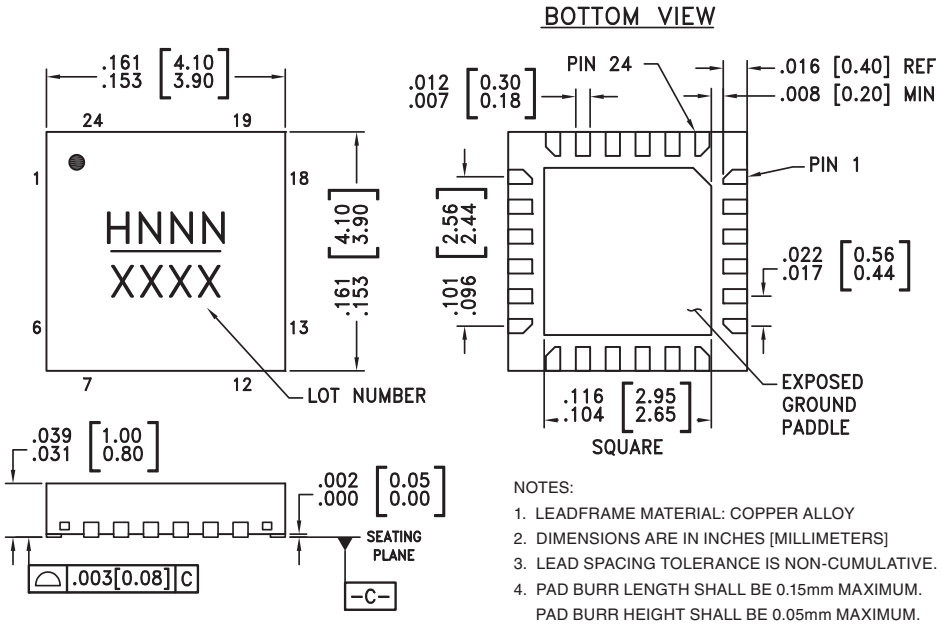
Drain Bias Voltage (Vdd1, 2, 3)	+5.5V
Gate Bias Voltage (Vgg1, 2)	-3 to 0V
Gain Control Voltage (Vctrl)	-3 to 0V
RF Power Input	+5 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 10.2 mW/°C above 85 °C) [1]	0.92 W
Thermal Resistance (Channel to ground paddle)	97.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Bias Voltage

Vdd1,2,3 (V)	Idd Total (mA)
+5.0	170
Vgg1,2 (V)	Igg Total (mA)
0V to -2V	<3 µA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC694LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H694 XXXX
HMC694LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H694 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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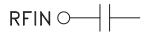
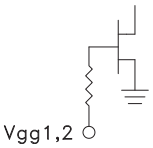
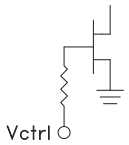
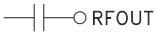
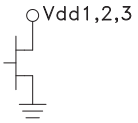
Pin Descriptions

Pad Number	Function	Description	Interface Schematic
1, 2, 6, 8, 10, 11, 13, 17, 18, 20, 21, 23	N/C	No Connection	
3, 5, 14, 16	GND	Die bottom must be connected to RF/DC ground.	
4	RFIN	This pad is AC coupled and matched to 50 Ohm.	
7, 12	Vgg1, 2	Gate control for amplifier. Adjust voltage to achieve typical Idd. Please follow “MMIC Amplifier Biasing Procedure” application note.	
9	Vctrl	Gain control Voltage for the amplifier. See assembly diagram for required external components.	
15	RFOUT	This pad is AC coupled and matched to 50 Ohm.	
19, 22, 24	Vdd1, 2, 3	Drain Bias Voltage for the amplifier. See assembly diagram for required external components	

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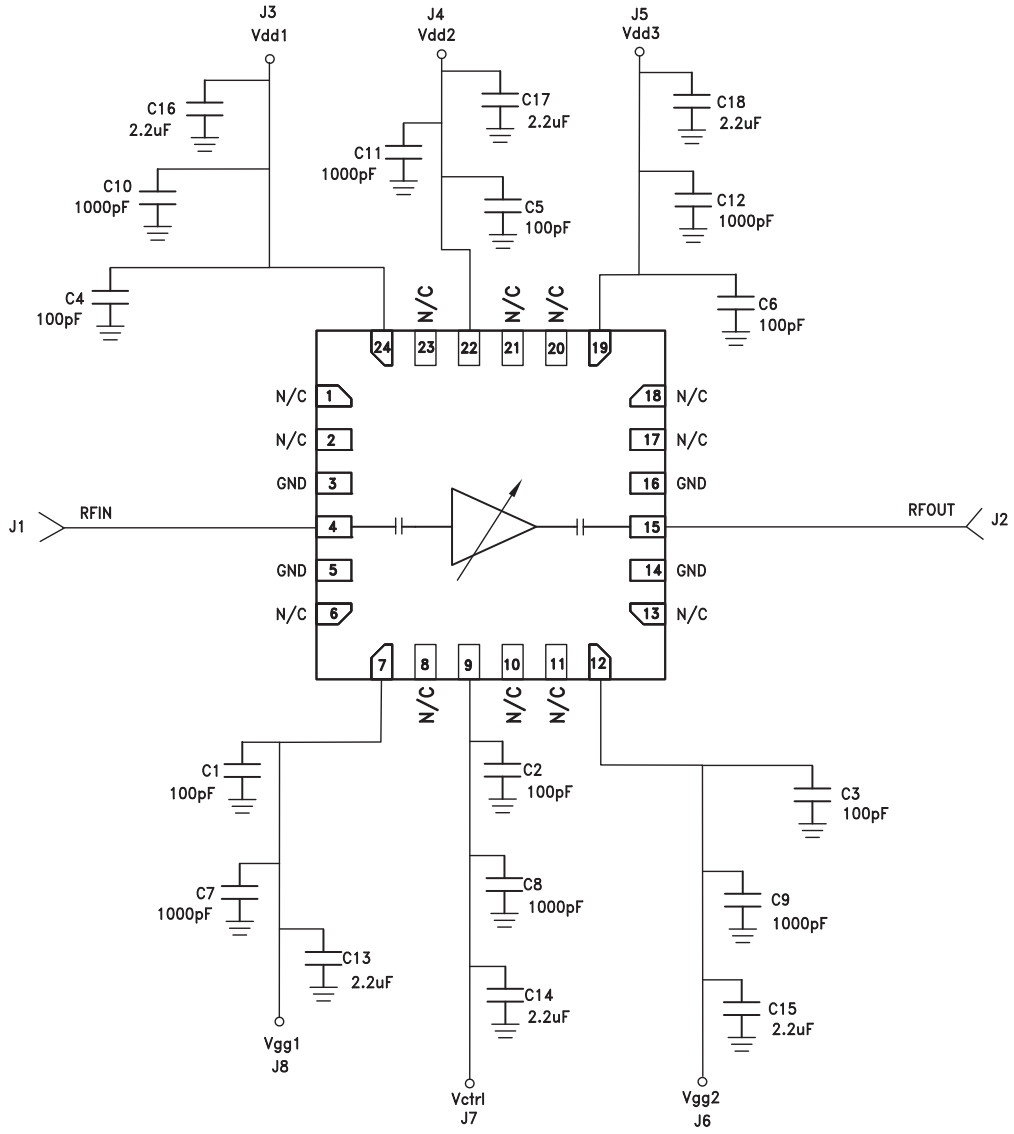
Application Circuit



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