

### FEATURES

- Equivalent input bandwidth: 9.3 GHz typical**
- Propagation delay: 85 ps typical**
- Overdrive and slew rate dispersion: 10 ps typical**
- Input signal minimum pulse width: 60 ps typical**
- Resistor programmable hysteresis**
- Differential latch control**
- Power dissipation: 140 mW typical**
- 16-terminal, 3 mm × 3 mm, ceramic leadless chip carrier (LCC)**
- 16-lead lead frame chip scale package (LFCSP)**

### APPLICATIONS

- Automatic test equipment (ATE) applications**
- High speed instrumentation**
- Digital receiver systems**
- Pulse spectroscopy**
- High speed trigger circuits**
- Clock and data restoration**

### GENERAL DESCRIPTION

The [HMC674LC3C/HMC674LP3E](#) are silicon germanium (SiGe), monolithic, ultrafast comparators that feature reduced swing positive emitter-coupled logic (RSPECL) output drivers and latch inputs. These comparators support 10 Gbps operation and provide 85 ps propagation delay and an input signal minimum pulse width of 60 ps with 0.2 ps rms of random jitter (RJ). Overdrive and slew rate dispersion is typically 10 ps, making the [HMC674LC3C/HMC674LP3E](#) ideal for a wide range of

applications from ATE to broadband communications. The RSPECL output stages directly drive 400 mV into a 50 Ω resistor terminated to  $V_{TT} = (V_{CC0} - 2.0 \text{ V})$ , where  $V_{TT}$  is the PECL termination voltage (see Figure 16). The [HMC674LC3C/HMC674LP3E](#) feature a high speed latch and programmable hysteresis. These devices can operate in either latch mode or as a tracking comparator.

### FUNCTIONAL BLOCK DIAGRAM

HMC674LC3C/HMC674LP3E

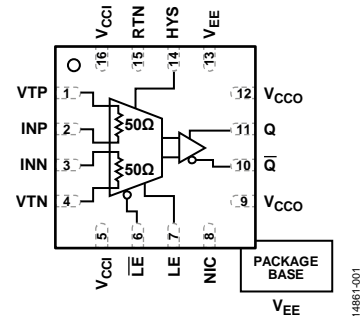


Figure 1. HMC674LC3C/HMC674LP3E Functional Block Diagram

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## REVISION HISTORY

Two Hittite Microwave product data sheets have been reformatted to the styles and standards of Analog Devices, Inc., and combined into one data sheet.

### 12/2016—v12.0616 (HMC674LC3C and HMC674LP3E) to Rev. K

Updated Format.....	Universal
Changes to Title, Features Section, and General Description Section.....	1
Changes to Table 7.....	6
Changes to Table 8.....	7
Changes to Figure 10.....	9
Changed Operational Description Section to Theory of Operation Section.....	10
Changes to Figure 15 and Table 9.....	12
Updated Outline Dimensions .....	13
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## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $V_{CCI} = 3.3\text{ V}$ ,  $V_{CCO} = 2.0\text{ V}$ ,  $V_{EE} = -3\text{ V}$ ,  $V_{TT} = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
INPUT				
Voltage Range	-2		+2	V
Differential Voltage	-1.75		+1.75	V
Offset Voltage ( $V_{OS}$ )		$\pm 5$		mV
Temperature Coefficient		15		$\mu\text{V}/^\circ\text{C}$
Bias Current		15		$\mu\text{A}$
Temperature Coefficient		50		$\text{nA}/^\circ\text{C}$
Offset Current		4		$\mu\text{A}$
Impedance		50		$\Omega$
Common-Mode		350		$\text{k}\Omega$
Differential		15		$\text{k}\Omega$
Active Gain		48		dB
Common-Mode Rejection Ratio (CMRR)		80		dB
Hysteresis, $R_{HYS} = \text{Infinity}$		$\pm 1$		mV

## LATCH ENABLE ( $\overline{\text{LE}}/\overline{\text{LE}}$ ) SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LATCH ENABLE ( $\overline{\text{LE}}/\overline{\text{LE}}$ )						
Input Impedance			8		$\text{k}\Omega$	Each pin
To Output Delay	$t_{PLOL}, t_{PLOH}$		85		ps	Input overdrive voltage ( $V_{OD}$ ) = 200 mV
Minimum Pulse Width	$t_{PL}$		20		ps	$V_{OD} = 200\text{ mV}$
Input Range		1.6		2.4	V	$V_{OD} = 200\text{ mV}$
LATCH ENABLE ( $\overline{\text{LE}}/\overline{\text{LE}}$ ) TIME						
Setup	$t_S$		45		ps	$V_{OD} = 200\text{ mV}$
Hold	$t_H$		-42		ps	

## DC OUTPUT SPECIFICATIONS

$V_{CCO} = 2.00\text{ V}$ ,  $V_{TT} = 0\text{ V}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
OUTPUT VOLTAGE					
High Level	$V_{OH}$	1.03	1.09	1.14	V
Low Level	$V_{OL}$	0.65	0.71	0.81	V
Differential Swing		440	760	980	mV p-p

## AC SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION DELAY ( $t_{PDL}$ , $t_{PD}$ , $t_{PDH}$ )	80	85	110	ps	$V_{OD} = 500$ mV
Temperature Coefficient		0.45		ps/°C	
Skew (Rising to Falling Transition)		10		ps	$V_{OD} = 500$ mV
$V_{OD}$ <sup>1</sup> DISPERSION		10		ps	$50$ mV < $V_{OD}$ < $1$ V
PROPAGATION DELAY ( $t_{PD}$ ) vs. INPUT COMMON-MODE VOLTAGE ( $V_{CM}$ ) DISPERSION		8		ps	$V_{OD} = 500$ mV, $-1.75$ V < $V_{CM}$ < $+1.75$ V
NOISE (RETURN TO INPUT, RTI)		5.9		nV/ $\sqrt{\text{Hz}}$	
EQUIVALENT INPUT BANDWIDTH ( $BW_{EQ}$ ) <sup>2</sup>	8.6	9.3	12	GHz	
JITTER					10 Gbps with $\pm 100$ mV overdrive
Deterministic		2		ps p-p	
Random		0.2		ps rms	
INPUT SIGNAL MINIMUM PULSE WIDTH		60		ps	$V_{CM} = 0$ V, $\pm 100$ mV overdrive
Q/Q TIME					From 20% to 80%
Rise		24		ps	
Fall		15		ps	

<sup>1</sup>  $V_{OD}$  is the input overdrive voltage, for example, ( $V_{INP} - V_{INN} - V_{OS}$ ), where  $V_{OS}$  is the input offset voltage.

<sup>2</sup> Equivalent input bandwidth is calculated by

$$BW_{EQ} = 0.22 / \sqrt{(TRCOMP^2 - TRIN^2)}$$

where:

$TRIN$  is the 20%/80% transition time of a quasi Gaussian signal applied to the comparator input.

$TRCOMP$  is the effective transition time digitized by the comparator.

## POWER SUPPLY SPECIFICATIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
VOLTAGE					
Power Supply Voltage Input Stage	$V_{CCI}$	3.135	3.3	3.465	V
Power Supply Voltage Output Stage	$V_{CCO}$	1.8	3.3	3.465	V
Negative Power Supply ( $-3$ V)	$V_{EE}$	$-3.15$	$-3.0$	$-2.85$	V
CURRENT					
Supply Input	$I_{CCI}$		9		mA
Supply Output	$I_{CCO}$		45		mA
$V_{EE}$	$I_{EE}$		19		mA
POWER DISSIPATION	$P_D$		140		mW
POWER SUPPLY REJECTION RATIO	PSRR				
$V_{CCI}$			38		dB
$V_{EE}$			38		dB

**TIMING DESCRIPTIONS**

Table 6.

Parameter	Symbol	Description
Input to Output High Delay	$t_{PDH}$	The propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the 50% point of an output low to high transition.
Input to Output Low Delay	$t_{PDL}$	The propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the 50% point of an output high to low transition.
Latch Enable ( $LE/\overline{LE}$ ) to Output High Delay	$t_{PLOH}$	The propagation delay measured from the 50% point of the latch enable ( $LE/\overline{LE}$ ) signal high to low transition to the 50% point of an output low to high transition.
Latch Enable ( $LE/\overline{LE}$ ) to Output Low Delay	$t_{PLOL}$	The propagation delay measured from the 50% point of the latch enable ( $LE/\overline{LE}$ ) signal high to low transition to the 50% point of an output high to low transition.
Minimum Hold Time	$t_H$	The minimum time after the positive transition of the latch enable ( $LE/\overline{LE}$ ) signal that the input signal must remain unchanged to be acquired and held at the outputs.
Minimum Latch Enable ( $LE/\overline{LE}$ ) Pulse Width	$t_{PL}$	The minimum time that the latch enable ( $LE/\overline{LE}$ ) signal must be low to acquire an input signal change.
Minimum Setup Time	$t_S$	The minimum time before the positive transition of the latch enable ( $LE/\overline{LE}$ ) signal that an input signal change must be present to be acquired and held at the outputs.
Output Rise Time	$t_R$	The amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
Output Fall Time	$t_F$	The amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
Input Overdrive Voltage	$V_{OD}$	The difference between the input voltages ( $V_{INP}$ and $V_{INN}$ ).

**Timing Diagram**

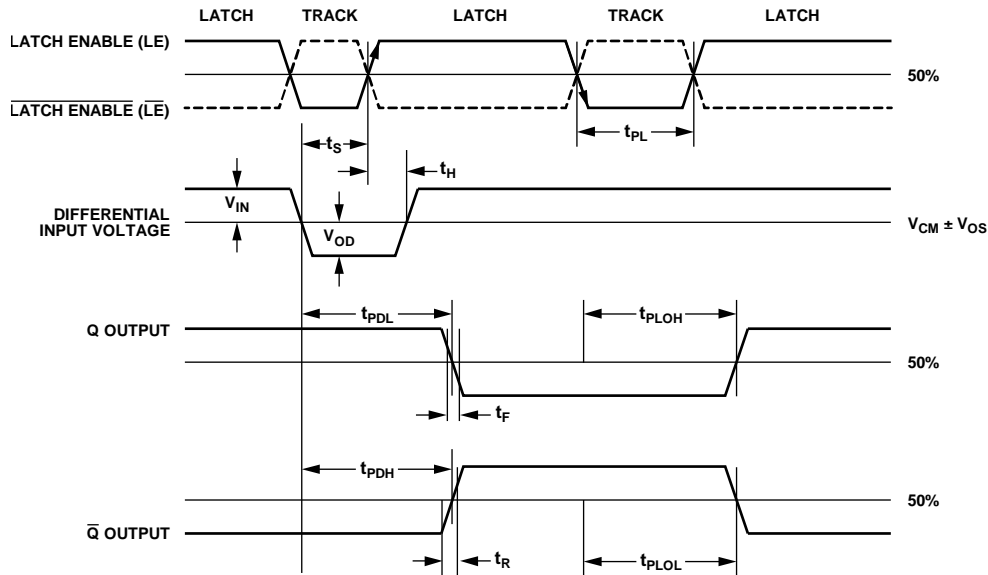


Figure 2. Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	
Input ( $V_{CCI}$ to GND)	–0.5 V to +4 V
Output ( $V_{CCO}$ to GND)	–0.5 V to +4 V
Positive Differential ( $V_{CCI}$ to $V_{CCO}$ )	–0.5 V to +3.3 V
$V_{EE}$ Supply to GND	–3.3 V to +0.5 V
Input Voltage	–2 V to +2 V
Differential	–2 V to +2 V
Latch Enable ( $LE/\overline{LE}$ )	–0.5 V to $V_{CCI} + 0.5$ V
Applied Voltage (HYS)	$V_{EE}$ to GND
Current	
Maximum Input	±20 mA
Output	40 mA
Continuous Power Dissipation ( $P_{DISS}$ , $T_A = 85^\circ\text{C}$ )	
Derate 43.5 mW/ $^\circ\text{C}$ Above $85^\circ\text{C}$ (HMC674LP3E)	1.74 W
Derate 20.4 mW/ $^\circ\text{C}$ Above $85^\circ\text{C}$ (HMC674LC3C)	0.816 W
Junction Temperature	$125^\circ\text{C}$
Maximum Peak Reflow Temperature <sup>1</sup>	
MSL1 and MSL3	$260^\circ\text{C}$
Thermal Resistance ( $\theta_{JC}$ )	
HMC674LP3E	$23^\circ\text{C/W}$
HMC674LC3C	$49^\circ\text{C/W}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
ESD Sensitivity, Human Body Model (HBM)	Class 1A

<sup>1</sup> See the Ordering Guide section.

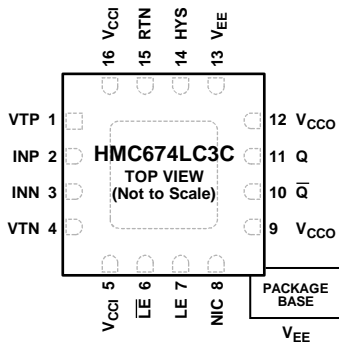
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

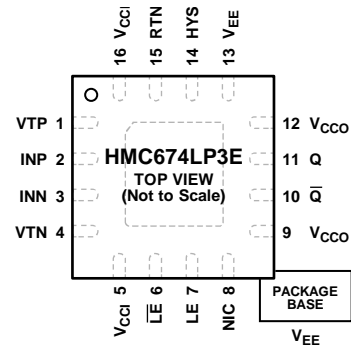
### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
 1. NIC = NOT INTERNALLY CONNECTED. CONNECT THIS PIN TO GROUND FOR IMPROVED NOISE.  
 2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO V<sub>EE</sub>.

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Figure 3. HMC674LC3C Pin Configuration



NOTES  
 1. NIC = NOT INTERNALLY CONNECTED. CONNECT THIS PIN TO GROUND FOR IMPROVED NOISE.  
 2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO V<sub>EE</sub>.

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Figure 4. HMC674LP3E Pin Configuration

Table 8. HMC674LC3C/HMC674LP3E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VTP	Termination Resistor Return Pin for V <sub>P</sub> Input. See Figure 5 for the interface schematic.
2	INP	Noninverting Analog Input. See Figure 5 for the interface schematic.
3	INN	Inverting Analog Input. See Figure 5 for the interface schematic.
4	VTN	Termination Resistor Return Pin for V <sub>N</sub> Input. See Figure 5 for the interface schematic.
5, 16	V <sub>CCI</sub>	Positive Supply Voltage Input Stage. See Figure 6 for the interface schematic.
6	$\overline{LE}$	Latch Enable Input Pin, Inverting Side. See the Theory of Operation section for additional information. See Figure 6 for the interface schematic.
7	LE	Latch Enable Input Pin, Noninverting Side. See the Theory of Operation section for additional information. See Figure 6 for the interface schematic.
8	NIC	Not Internally Connected. Connect this pin to ground for improved noise.
9, 12	V <sub>CCO</sub>	Positive Supply Voltage for the Output Stage. See Figure 7 for the interface schematic.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in track mode. See the Theory of Operation section for additional information. See Figure 7 for the interface schematic.
11	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in track mode. See the Theory of Operation section for additional information. See Figure 7 for the interface schematic.
13	V <sub>EE</sub>	Negative Power Supply, -3 V. See Figure 6 for the interface schematic.
14	HYS	Hysteresis Control Pin. Leave this pin disconnected for zero hysteresis. Connect this pin to V <sub>EE</sub> with a resistor to add the desired amount of hysteresis. See Figure 12 to determine the correct size of the R <sub>HYS</sub> hysteresis control resistor. See Figure 8 for the interface schematic.
15	RTN	Return for ESD Protection.
	EPAD	Exposed Pad. The exposed pad must be connected to V <sub>EE</sub> .

INTERFACE SCHEMATICS

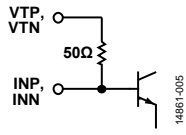


Figure 5. VTP, VTN and INP, INN Interface Schematic

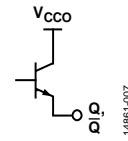


Figure 7. Q,  $\bar{Q}$  Interface Schematic

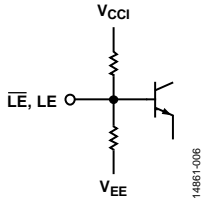


Figure 6.  $\bar{LE}$ , LE Interface Schematic

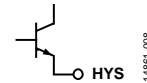


Figure 8. HYS Interface Schematic



### TYPICAL PERFORMANCE CHARACTERISTICS

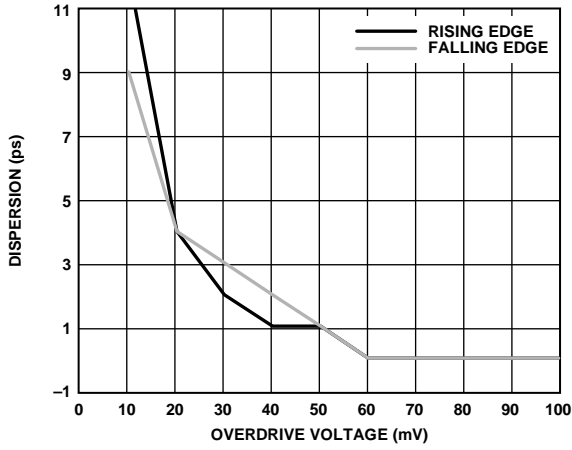


Figure 9. Dispersion vs. Overdrive Voltage

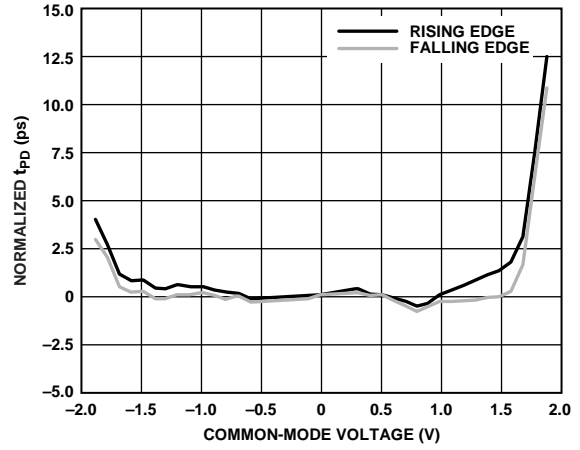


Figure 11. Normalized Propagation Delay ( $t_{PD}$ ) vs. Common-Mode Voltage

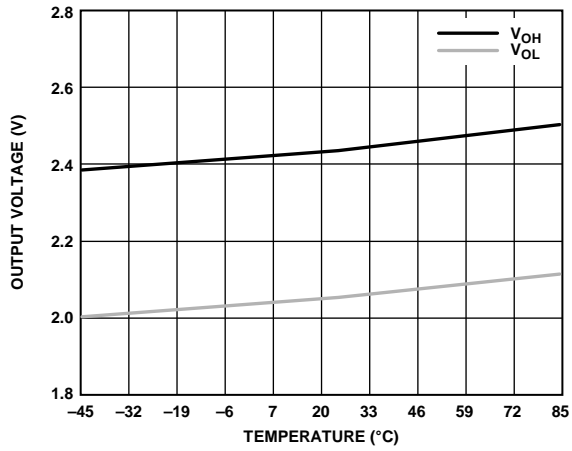


Figure 10. Output Voltage vs. Temperature

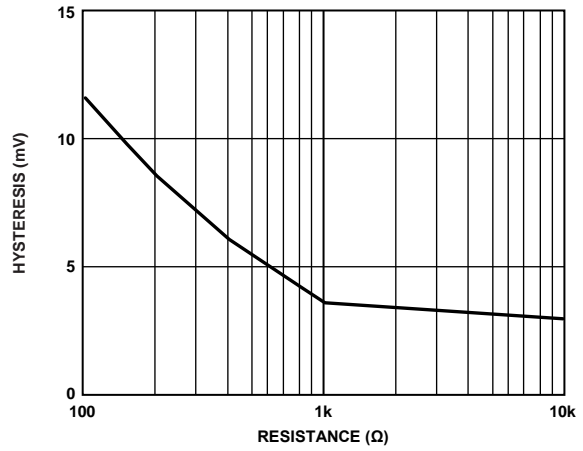


Figure 12. Comparator Hysteresis vs.  $R_{HYS}$  Control Resistance

## THEORY OF OPERATION

The [HMC674LC3C/HMC674LP3E](#) are latched comparators with a 9.3 GHz equivalent input bandwidth. These devices are comprised of three blocks: an input amplifier, a latch, and an output buffer. The latching circuit is level sensitive and consists of a single, high speed latch. The [HMC674LC3C/HMC674LP3E](#) comparators support 10 Gbps operation. The input signal minimum pulse width is 60 ps.

The [HMC674LC3C/HMC674LP3E](#) operate in either track (transparent) mode, where the output follows the logical value of the input, or latch (hold) mode, where the output value is held to the logical value of the comparison result of the input just prior to  $(LE - \overline{LE})$  going high. Select track mode operation by either setting  $(LE - \overline{LE})$  low or by floating the LE and  $\overline{LE}$  inputs. Select latch mode by setting  $(LE - \overline{LE})$  high. The input impedance of the LE and  $\overline{LE}$  inputs is 8 k $\Omega$ ; however, these inputs can be terminated with 50  $\Omega$  external resistors, if desired.

When the clock inputs are dc-coupled, they operate at an input common-mode voltage of 2 V. In this case, any termination resistors ideally return to 2 V. If the clock inputs are ac-coupled to the [HMC674LC3C/HMC674LP3E](#), return the input termination resistors to ground.

## POWER SEQUENCING

As long as the input signal is not near the  $-2$  V extreme, either  $V_{CC}$  or  $V_{EE}$  can be powered on first. However, if the input voltage is more negative than  $-1.8$  V, use the following power-up sequence:

1.  $V_{EE}$
2.  $V_{CCI}$  and  $V_{CCO}$  (if  $V_{CCO} = V_{CCI}$ )
3.  $V_{CCO}$  (if different than ground)

Note that the power-down sequence is the reverse of this sequence.

It is recommended to power up the [HMC674LC3C](#) or the [HMC674LP3E](#) before applying the input signal and to remove the input signal prior to powering either down. These recommendations are important if any of the inputs are more negative than  $-1.8$  V.

### APPLICATIONS INFORMATION

#### EVALUATION PRINTED CIRCUIT BOARD (PCB)

Figure 13 shows the front side of the evaluation PCB, and Figure 14 shows the back side of the evaluation PCB.

The evaluation PCB used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance, and

the package ground leads must be connected directly to the ground plane similar to that shown in Figure 15. Use a sufficient number of via holes to connect the top and bottom ground planes to provide good RF grounding to 10 GHz. The evaluation PCB shown in Figure 13 is available from Analog Devices, Inc., upon request.

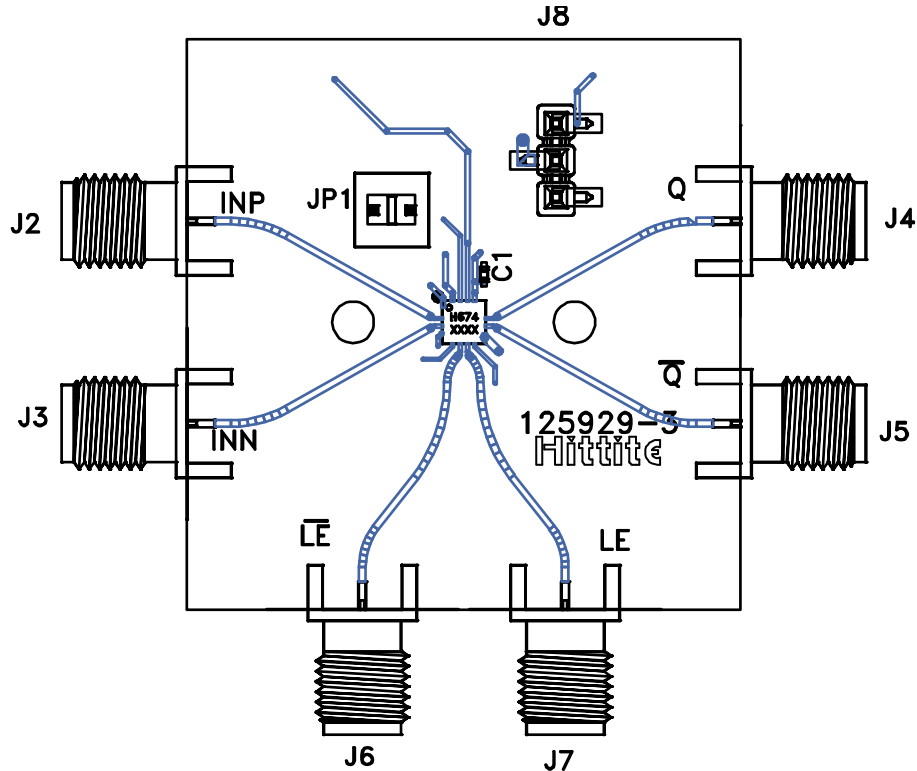


Figure 13. Front Side of the Evaluation PCB

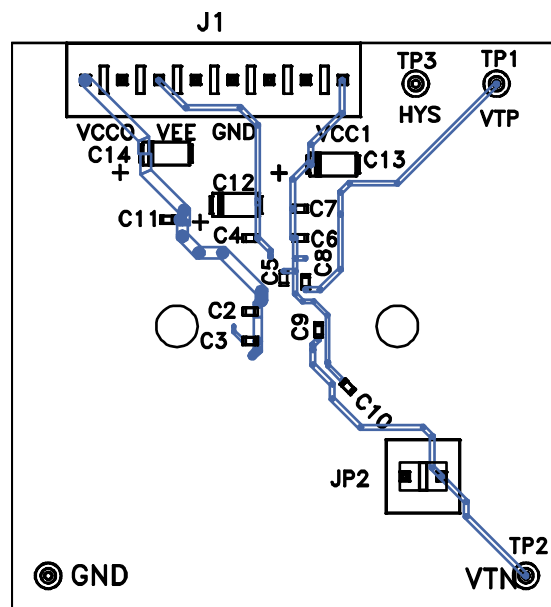


Figure 14. Back Side of the Evaluation PCB

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## APPLICATION CIRCUITS

See Figure 15 for the typical application circuit, Table 9 for the bill of materials, and Figure 16 for the output interfacing application circuit.

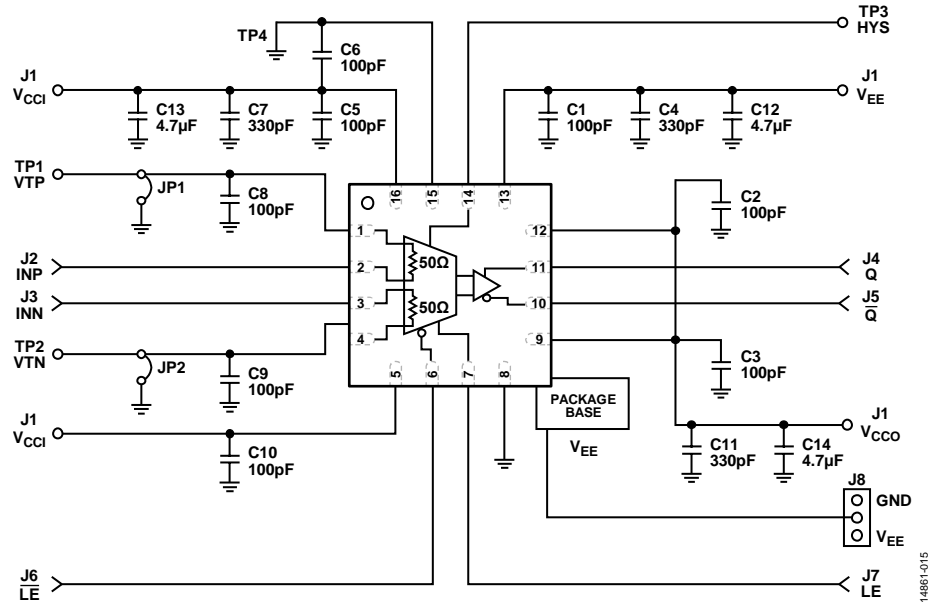


Figure 15. Typical Application Circuit

Table 9. Bill of Materials for the Evaluation PCB (125929-3)

Item	Description
J1	Eight position vertical header
J2 to J7	2.92 mm, 40 GHz jacks
J8	Terminal strip, single row, 3-pin surface mount (SMT)
JP1, JP2	Two position vertical header
C1 to C3, C5, C6, C8 to C10	100 pF capacitors, 0402 package
C4, C7, C11	330 pF capacitors, 0402 package
C12 to C14	4.7 μF tantalum capacitors
TP1 to TP4	DC pin, swage mount test points
U1	<a href="#">HMC674LC3C/HMC674LP3E</a> comparator
PCB	125929-3 <sup>1</sup> evaluation PCB, circuit board material is Rogers 4350 or Arlon 25FR

<sup>1</sup> Reference this number when ordering complete evaluation PCB.

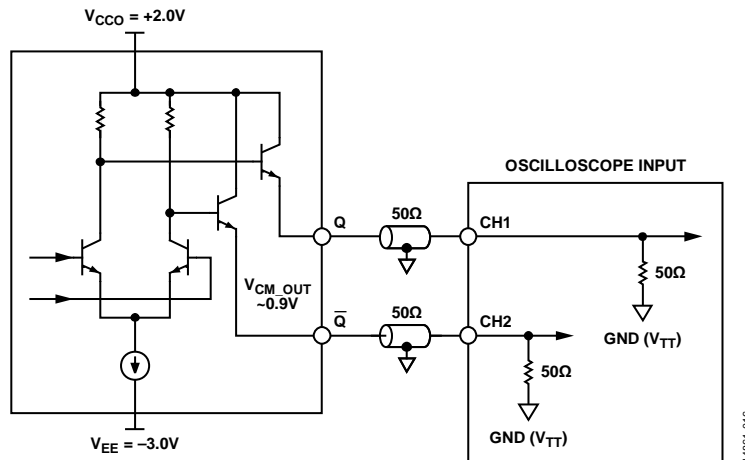


Figure 16. Output Interfacing Application Circuit, Output to Oscilloscope

OUTLINE DIMENSIONS

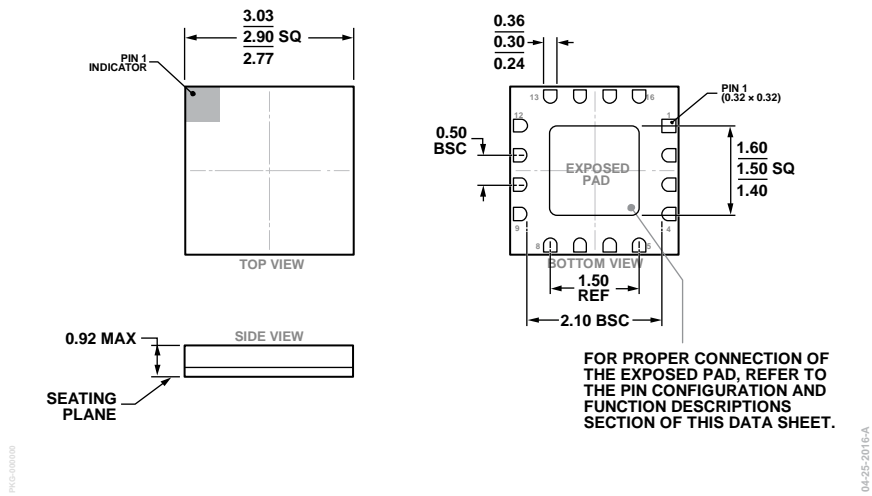
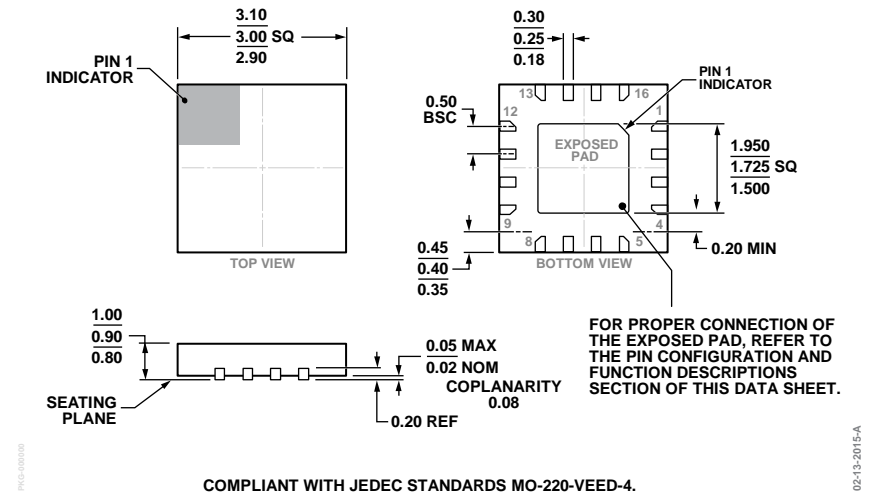


Figure 17. 16-Terminal Ceramic Leadless Chip Carrier [LCC] (E-16-1)  
Dimensions shown in millimeters



COMPLIANT WITH JEDEC STANDARDS MO-220-VEED-4.  
Figure 18. 16-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.90 mm Package Height (HCP-16-1)  
Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Body Material	Lead Finish	MSL Rating <sup>2</sup>	Package Description	Package Option	Branding
HMC674LC3C	-40°C to +85°C	Alumina, White	Gold over Nickel	MSL3	16-Terminal LCC	E-16-1	H674 XXXX
HMC674LC3CTR	-40°C to +85°C	Alumina, White	Gold over Nickel	MSL3	16-Terminal LCC	E-16-1	H674 XXXX
HMC674LC3CTR-R5	-40°C to +85°C	Alumina, White	Gold over Nickel	MSL3	16-Terminal LCC	E-16-1	H674 XXXX