

## 20 Gbps CLOCKED COMPARATOR

### Typical Applications

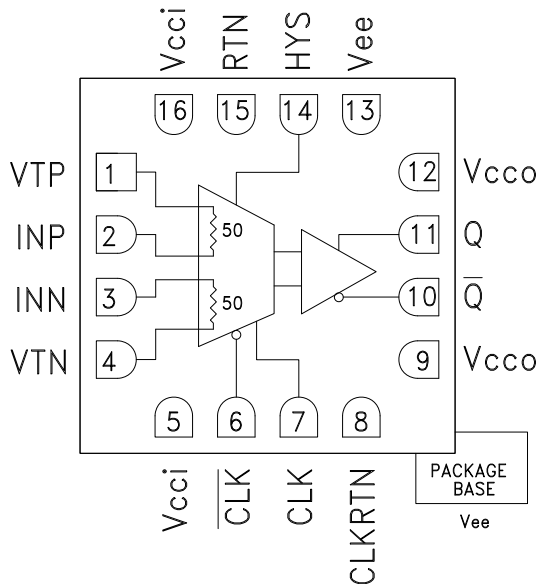
The HMC874LC3C is ideal for:

- ATE Applications
- High Speed Instrumentation
- Digital Receiver Systems
- Pulse Spectroscopy
- High Speed Trigger Circuits
- Clock & Data Restoration

### Features

- Propagation Delay Clock to Output: 120 ps
- Overdrive & Slew Rate Dispersion: 10 ps
- Minimum Pulse Width: 60 ps
- Resistor Programmable Hysteresis
- Differential Clock Control
- Input Bandwidth: 10 GHz
- Power Dissipation: 150 mW
- RSCML Version Available
- 16 Lead 3x3 mm SMT Package: 9 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC874LC3C is a SiGe monolithic, ultra fast comparator. The comparator supports 20 Gbps operation while providing 120 ps clock to data output delay and 60 ps minimum pulse width with 0.2 ps rms random jitter (RJ). 25 Gbps operation can be achieved with reduced output voltage swing. Overdrive and slew rate dispersion are typically 10 ps, making the device ideal for a wide range of applications from ATE to broadband communications. The output stages are designed to directly drive 400 mV into 50 ohms terminated to  $V_{tt} = (V_{cco} - 2.0 V)$ . The HMC874LC3C features high-speed latches with programmable hysteresis, and is configured to operate as a clocked comparator.

### Electrical Specifications

$T_A = +25\text{ }^\circ\text{C}$ ,  $V_{ccI} = +3.3 V$ ,  $V_{cco} = +2.0 V$ ,  $CLK / \overline{CLK} = 1.6 V$  to  $2.4 V$ ,  $V_{ee} = -3 V$ ,  $V_{tt} = 0 V$

Parameter	Conditions	Min.	Typ.	Max	Units
Input Voltage Range	Maximum DC Input Current = 20 mA	-2		2	V
Input Differential Voltage		-1.75		1.75	V
Input Offset Voltage ( $V_{os}$ )			±5		mV
Input Offset Voltage, Temperature Coefficient			15		$\mu V / ^\circ C$
Input Bias Current			15		$\mu A$
Input Bias Current Temperature Coefficient			50		$nA / ^\circ C$
Input Offset Current			4		$\mu A$
Input Impedance			50		$\Omega$
Common Mode Input Impedance			350		$K\Omega$
Differential Input Impedance			15		$K\Omega$
Hysteresis	$R_{hys} = \infty$		±1		mV

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### Clock Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
Clock Input Impedance	Each Pin		50		$\Omega$
Clock to Data Output Delay, t <sub>pd</sub>			120		ps
Clock Input Range		1.6	2.0	2.4	V
Clock Max Frequency, f <sub>max</sub>			25		GHz

### DC Output Characteristics, V<sub>cco</sub> = +2.0 V, V<sub>tt</sub> = 0 V

Parameter	Conditions	Min.	Typ.	Max	Units
Output Voltage High Level, V <sub>oh</sub>		1.03	1.09	1.14	V
Output Voltage Low Level, V <sub>ol</sub>		0.65	0.71	0.81	V
Output Voltage Differential Swing		440	760	980	mV <sub>pp</sub>

### AC Performance

Parameter	Conditions	Min.	Typ.	Max	Units
Propagation Delay - t <sub>pd</sub> , t <sub>pdl</sub> , t <sub>pdh</sub>	VOD = 500 mV	80	85	110	ps
Propagation Delay, Temperature Coefficient			0.45		ps / °C
Propagation Delay Skew (Rising to Falling Transition)	VOD = 500 mV		10		ps
VOD <sup>[1]</sup> Dispersion	50 mV < VOD < 1V		10		ps
t <sub>pd</sub> vs. Common Mode Dispersion, -1.75 V < V <sub>cm</sub> < 1.75 V	VOD = 500 mV		8		ps
Noise (RTI)			5.9		nV/ $\sqrt{\text{Hz}}$ RTI
Equivalent Input Bandwidth <sup>[2]</sup>		8.6	9.3	12	GHz
Deterministic Jitter (pp)	Deterministic Jitter at 10 Gbps with $\pm 100$ mV Overdrive		2		ps
Random Jitter (rms)	Random Jitter at 10 Gbps with $\pm 100$ mV Overdrive		0.2		ps rms
Input Signal Minimum Pulse Width	V <sub>CM</sub> = 0; $\pm 100$ mV Overdrive		60		ps
Q / QB Rise Time	From 20% to 80%		24		ps
Q / QB Fall Time	From 20% to 80%		15		ps

[1] VOD is the input overdrive voltage, for example, (V<sub>inp</sub> - V<sub>inn</sub> - V<sub>os</sub>) where V<sub>os</sub> = input offset voltage.

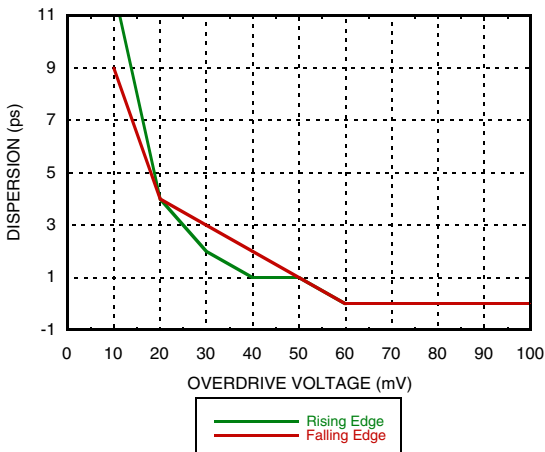
[2] Equivalent Input Bandwidth is calculated with the following formula: B<sub>weq</sub> = 0.22/f (TRCOMP2-TRIN2) where TRIN is the 20%/80% transition time of a quasi-Gaussian signal applied to the comparator input, and TRCOMP is the effective transition time digitized by the comparator.

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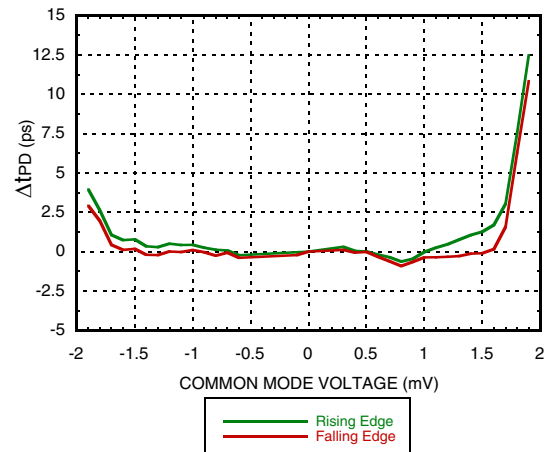
### Power Supply Requirements

Parameter	Conditions	Min.	Typ.	Max	Units
V <sub>cci</sub>		3.135	3.3	3.465	V
V <sub>cco</sub>		1.8	3.3	3.465	V
V <sub>ee</sub>		-3.15	-3.0	-2.85	V
Input Supply Current, I <sub>cci</sub>			9		mA
Output Supply Current, I <sub>cco</sub>			45		mA
V <sub>ee</sub> Current, I <sub>ee</sub>			19		mA
Power Dissipation, P <sub>d</sub>			140		mW
PSRR, V <sub>cci</sub>			38		dB
PSRR, V <sub>ee</sub>			38		dB

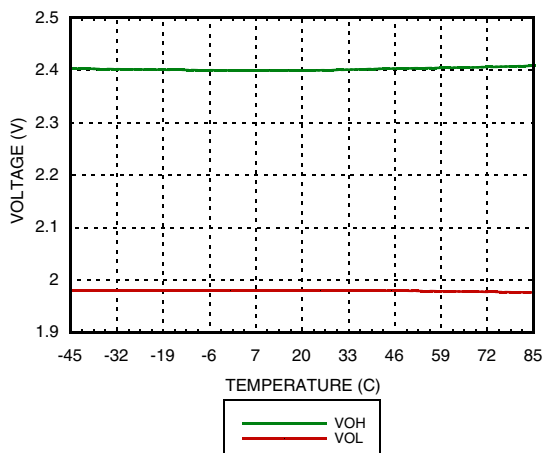
### Dispersion vs. Overdrive Voltage



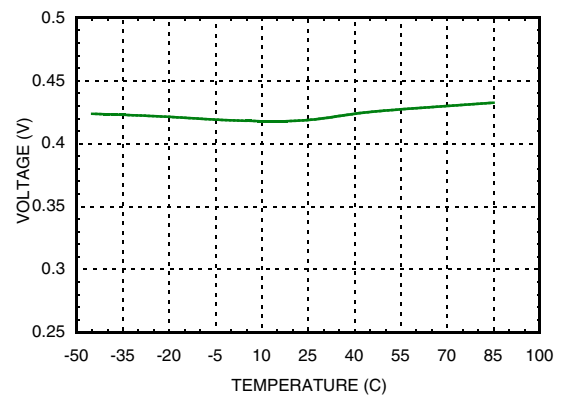
### Propagation Delay vs. Common Mode



### Output Voltage vs. Temperature

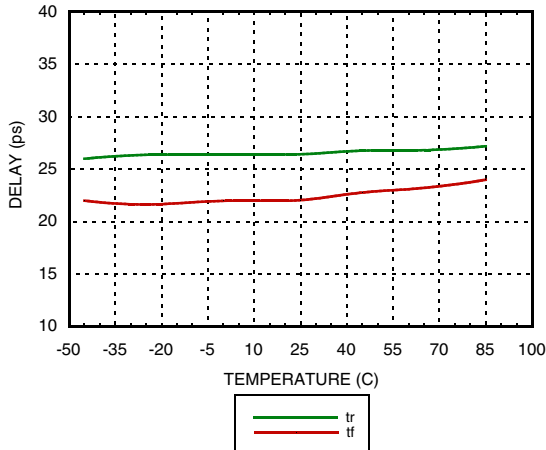


### Voltage Swing vs. Temperature

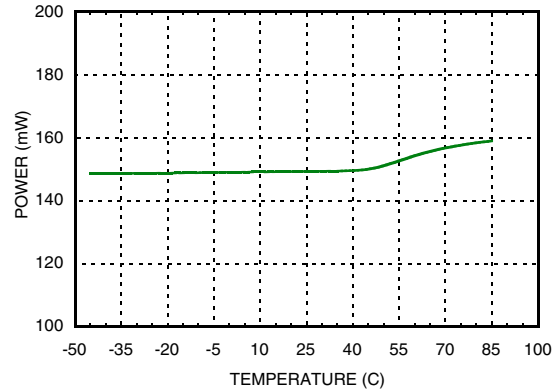


**20 Gbps CLOCKED COMPARATOR**

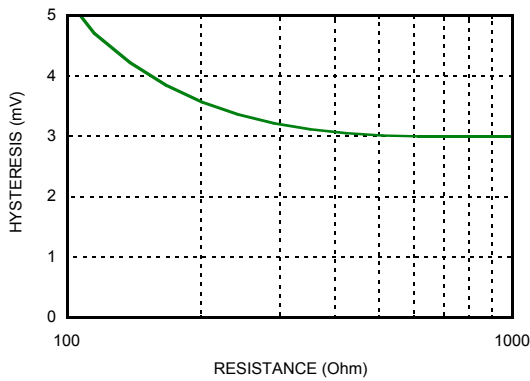
**Delay vs. Temperature**



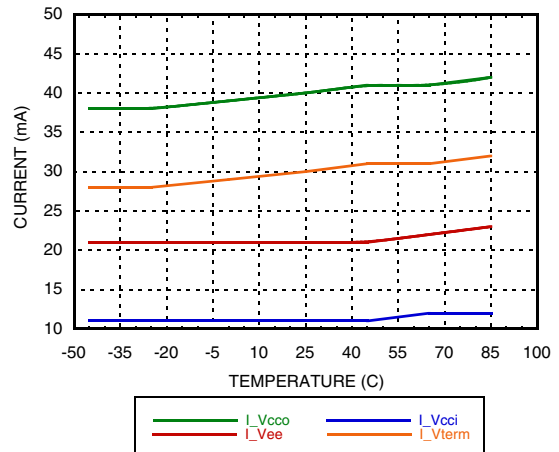
**Power Dissipation vs. Temperature**



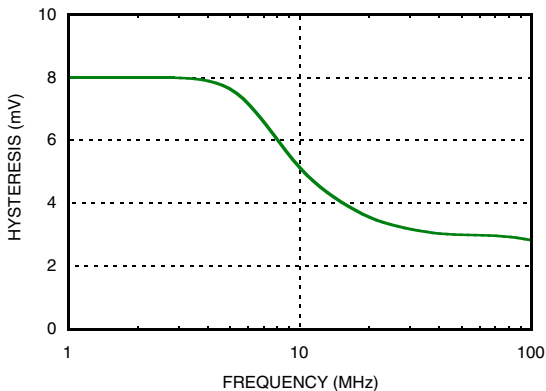
**Comparator Hysteresis vs. Rhys Control Resistor**



**Currents vs. Temperature**

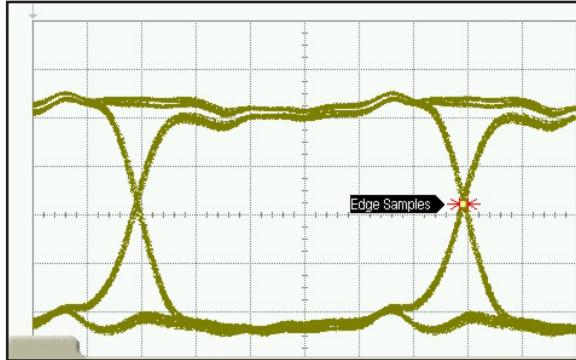


**Comparator Hysteresis vs. Clock Frequency ( $R_{hys} = \infty$ )**



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### Eye Diagram



TJ (1E-12):	6.71 ps	DJ(6-6):	3.08 ps	RJ(rms):	265 fs
RJ(6-6):	310 fs	DDJ(p-p):	3.24 ps	DCD:	-----
PJ(rms)	0.0 s			ISI J(p-p)	3.24 ps

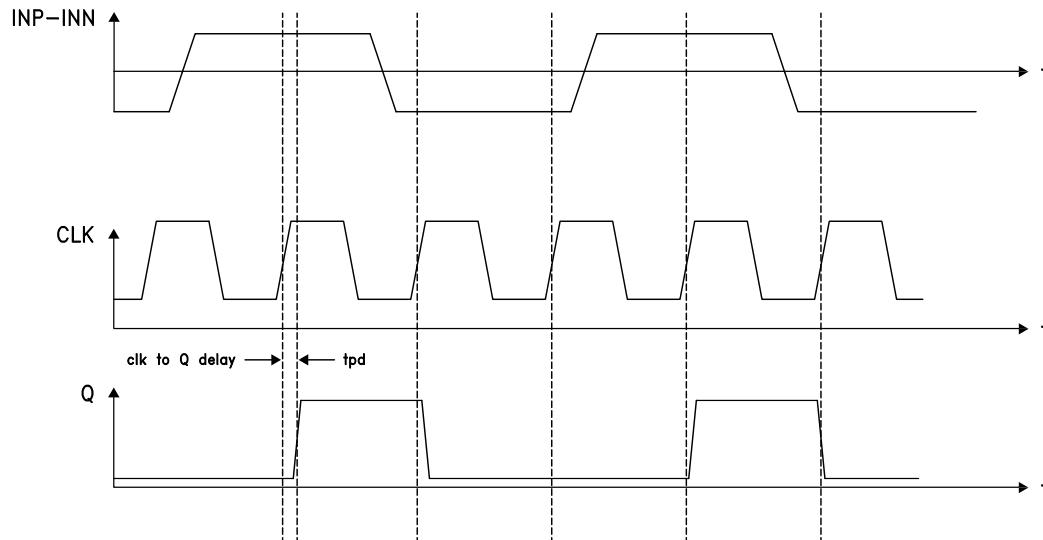
Bit Rate	5.00000 Gb/s
Pat Length	127 Bits
Div. Ratio	1:8

### Absolute Maximum Ratings

Input Supply Voltage (V <sub>cci</sub> to GND)	-0.5 V to +4 V
Output Supply Voltage (V <sub>cco</sub> to GND)	-0.5 V to +4 V
Positive Supply Differential (V <sub>cci</sub> - V <sub>cco</sub> )	-0.5 V to +3.5 V
Input Voltage	-2 V to +2 V
Differential Input Voltage	-2 V to +2 V
Input Voltage, Clock	-0.5 V to V <sub>cci</sub> +0.5 V
Applied Voltage (HYS)	V <sub>ee</sub> to GND
Maximum Input Current	±20 mA
Output Current	40 mA
Junction Temperature	125 °C
Continuous P <sub>diss</sub> (T = 85 °C) (Derate 20.4 mW/°C above 85 °C)	0.816 W
Thermal Resistance (R <sub>th</sub> ) (Junction to Lead)	49 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1A



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**20 Gbps CLOCKED COMPARATOR**
**Timing Diagram**

**Power Sequencing**

As long as the input signal is not near the -2 V extreme, either Vcc or Vee can be powered on first. However, if the input voltage is more negative than -1.8 V, we recommend the following power-up sequence.

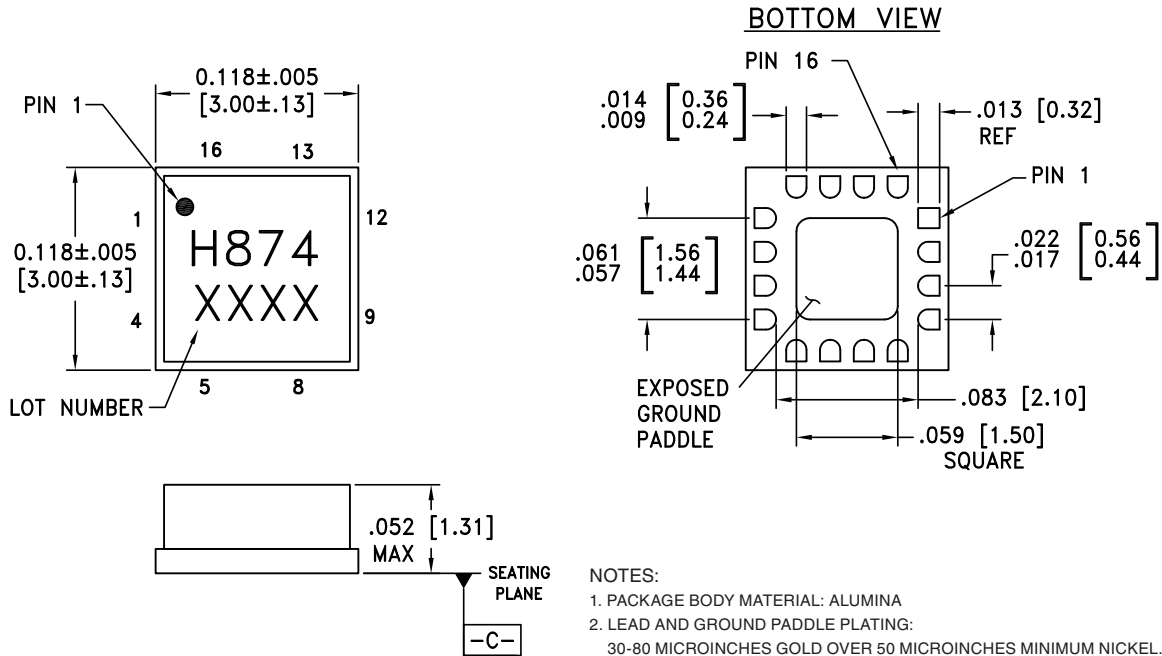
- 1) Vee
- 2) Vcci and Vcco (if Vcco = Vcci)
- 3) Vcco (if different than ground).

Power down would be the reverse of this sequence.

It is also recommended that the device be powered before applying the input signal and also that the input signal be removed prior to power down. This is most important if any of the inputs are more negative than -1.8 V.

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**Outline Drawing**



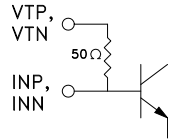
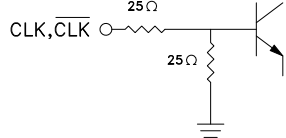
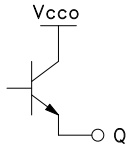
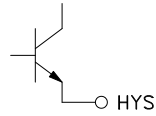
- NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
  2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
  3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
  4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
  5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
  6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
  7. PADDLE MUST NOT BE DC GND. THERMAL DISSIPATION PATH ONLY.

**Package Information**

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[2]</sup>
HMC874LC3C	Alumina, White	Gold over Nickel	MSL3 <sup>[1]</sup>	H874 XXXX

[1] Max peak reflow temperature of 260°C  
 [2] 4-Digit lot number XXXX

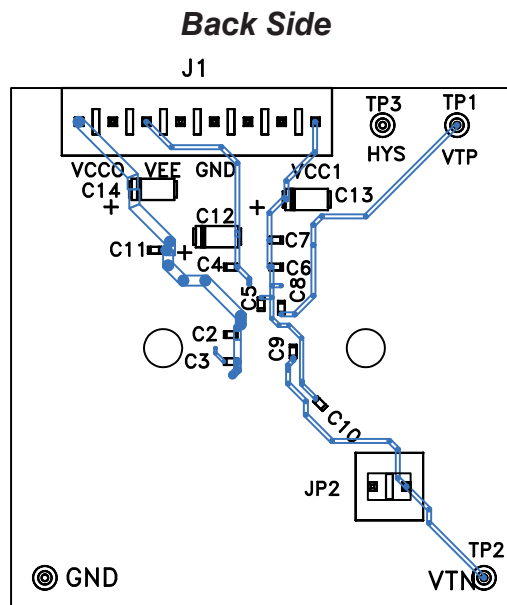
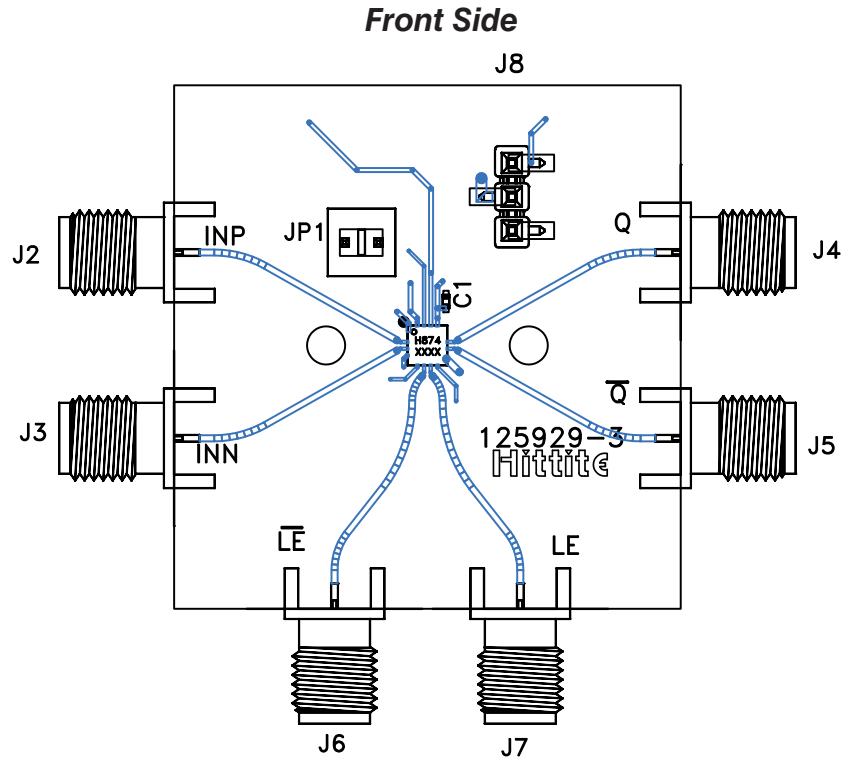
**20 Gbps CLOCKED COMPARATOR**
**Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1	VTP	Termination resistor return pin for INP Input.	
2	INP	Non-Inverting analog input	
3	INN	Inverting analog input	
4	VTN	Termination resistor return pin for INN input	
5, 16	Vcci	Positive supply voltage input stage.	
6	$\overline{\text{CLK}}$	Clock input pin, inverting side.	
7	CLK	Clock input pin, non-inverting side.	
8	CLKRTN	Clock RTN pin, connect to GND.	
9, 12	Vcco	Positive supply voltage for the output stage.	
10	$\overline{\text{Q}}$	Inverting output. Q bar is at logic low if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, after a positive transition on CLK and negative transition on $\overline{\text{CLK}}$ .	
11	Q	Non-inverting output. Q is at logic high if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, after a positive transition on CLK and negative transition on CLK.	
14	HYS	Hysteresis Control pin. This pin should be left disconnected to minimize hysteresis. Connect to Vee with a resistor to add the desired amount of hysteresis.	
13	Vee	Negative power supply, -3V.	
15	RTN	Return for ESD protection, connect to GND.	
	Package Base	Do not DC GND. Thermal dissipation path only.	



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**Evaluation PCB**



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### List of Materials for Evaluation PCB 125932 [1]

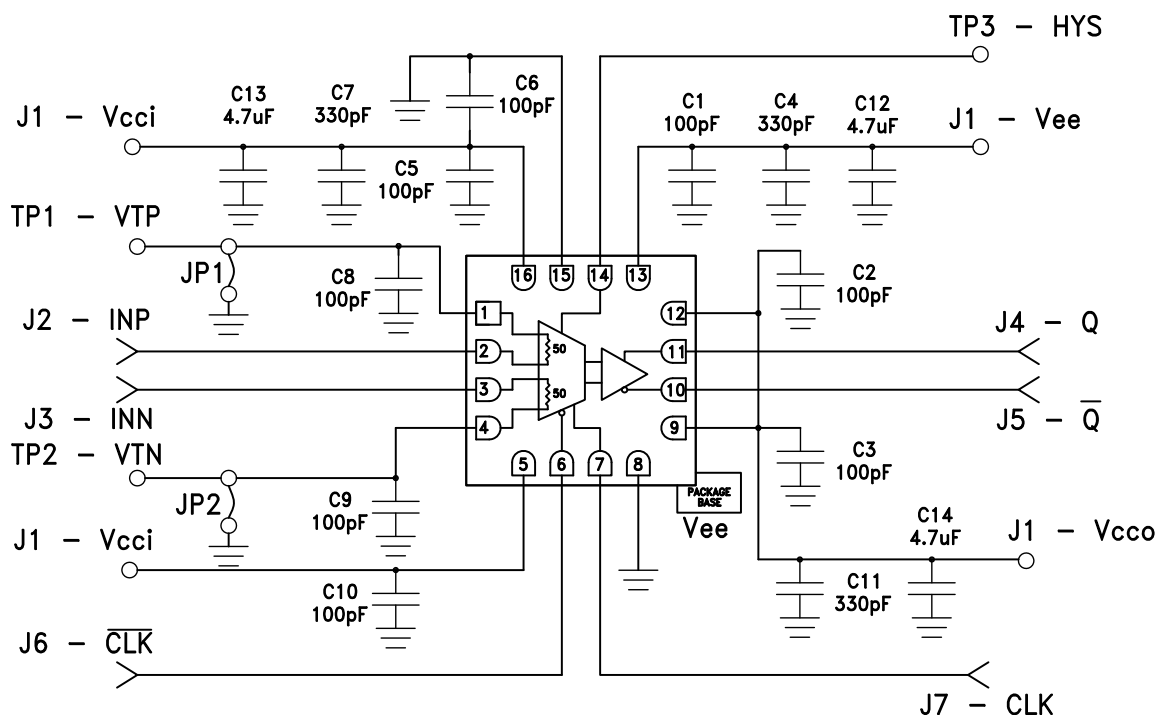
Item	Description
J1	8 Pos. Vertical TIN
J2 - J7	2.92 mm 40 GHz Jack
J8	Terminal Strip, Single Row 3 Pin SMT
JP1, JP2	2 Pos. Vertical TIN
C1 - C3, C5, C6, C8 - C10	100 pF Capacitor, 0402 Pkg.
C4, C7, C11	330 pF Capacitor, 0402 Pkg.
C11 - C13	4.7 uF Tantalum
TP1 - TP4	DC Pin, Swage Mount
U1	HMC874LC3C Comparator
PCB	125929 Evaluation PCB

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed paddle should not be electronically connected to DC GND, thermal dissipation path only. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 25 GHz. The evaluation circuit board shown is available from Hittite upon request.

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

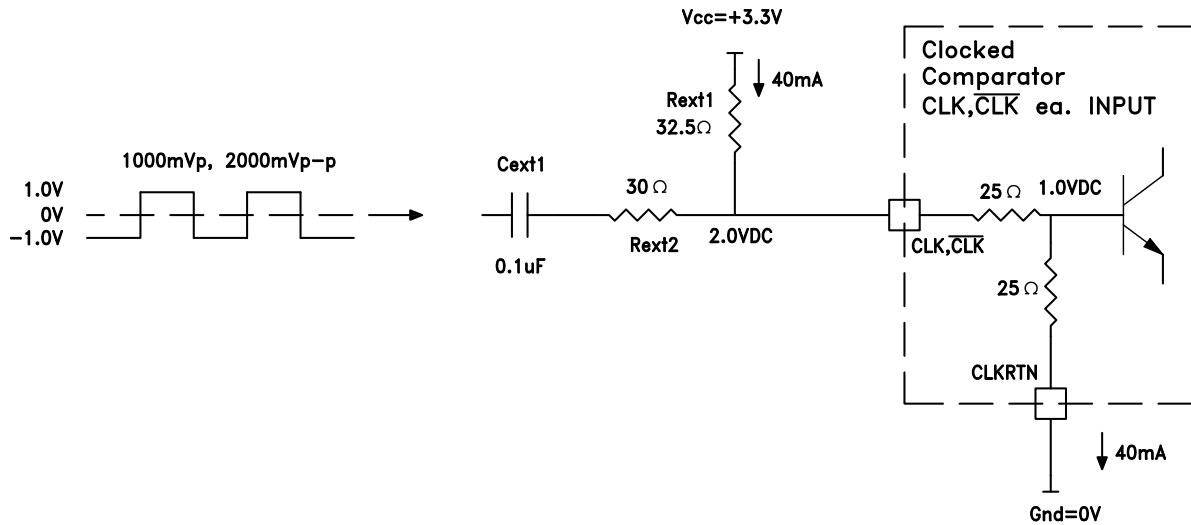
### Application Circuits



**20 Gbps CLOCKED COMPARATOR**

**Application Circuits: CLK,  $\overline{\text{CLK}}$  Interfacing**

**Figure A1: Resistor Network**



**Figure A2: Bias Tee**

