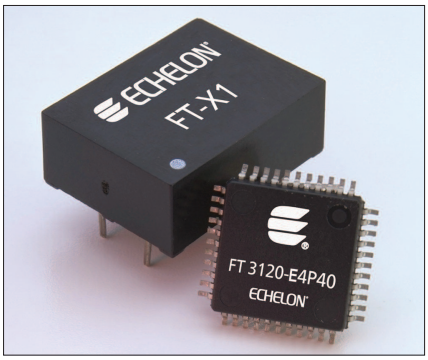
FT 3120® and FT 3150® Free Topology Smart Transceivers



FT 3120 transceiver in a 44-pin TQFP package[1]

Features

- Combines an ANSI/CEA 709.3-1999 compliant free topology twisted pair transceiver with a Neuron 3120 or Neuron 3150 network processor core
- Supports polarity insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring
- 78 kilobits per second bit rate for distances up to 500 meters in free topology or 2700 meters in bus topology with double terminations
- High performance Neuron network processor core enables concurrent processing of application code and network packets (40MHz maximum for FT 3120 smart transceiver, 20MHz maximum for FT 3150 smart transceiver)
- 4Kbytes of embedded EEPROM for application code and configuration data on the FT 3120 smart transceiver and 0.5Kbytes of embedded EEPROM for configuration data on the FT 3150 smart transceiver
- Interface for external memory for devices with larger memory requirements (FT 3150 smart transceiver only)
- 2Kbytes of embedded RAM for buffering network data and network variables
- 11 I/O pins with 34 programmable standard I/O modes minimizing external interface circuitry
- Unique 48-bit Neuron ID in every device for network installation and management
- Compact external transformer with patent pending architecture providing exceptional immunity from magnetic interference and high frequency common mode noise
- Compatible with TP/FT-10 channels using FTT-10 and/or FTT-10A Free Topology Transceivers and, with suitable DC blocking capacitors, LPT-10 Link Power Transceivers
- Communications parameters preprogrammed for the TP/FT-10 channel at 10MHz
- 5V operation with low power consumption
- -40 to +85°C operating temperature range[3, 4

Description

The FT 3120 and FT 3150 Free Topology Smart Transceivers integrate a Neuron® 3120 or Neuron 3150 network processor core, respectively, with a free topology twisted pair transceiver to create a low cost, smart transceiver on a chip. Combined with Echelon's high performance FT-X1 or FT-X2 Communication Transformer, the FT 3120 and FT 3150 smart transceivers set new benchmarks for performance, robustness, and low cost. Ideal for use in LonWorks® devices destined for building, industrial, transportation, home, and utility automation applications, the FT 3120 and FT 3150 Free Topology Smart Transceivers can be used in both new product designs and as a means of cost reducing existing nodes.

The integral transceiver is fully compatible with the TP/FT-10 channel and can communicate with devices using Echelon's FTT-10A Free Topology Transceiver, and, when used with suitable DC isolation capacitors, the LPT-11 Link Power Transceiver. The free topology transceiver supports polarity insensitive cabling using a star, bus, daisy-chain, loop, or combination topology (see Figure 1)—freeing the installer from the need to adhere to a strict set of wiring rules. Free topology wiring reduces the time and expense of node installation by allowing the wiring to be installed in the most expeditious and cost-effective manner. It also simplifies network expansion by eliminating restrictions on wire routing, splicing, and node placement.

The FT 3120 Free Topology Smart Transceiver is a complete system-on-a-chip that is targeted at cost-sensitive and small form factor designs with a need for up to 4Kbytes of application code. The Neuron 3120 core operates at up to 40MHz[2], and includes 4Kbytes of EEPROM and 2Kbytes of RAM. The Neuron firmware is pre-programmed in an on-chip ROM. The application code is stored in the embedded EEPROM memory and may be updated over the network. The FT 3120 smart transceiver is offered in a 32-lead SOIC package as well as a compact 44-lead TQFP package.

The FT 3150 Free Topology Smart Transceiver includes a 20MHz Neuron 3150 core, 0.5Kbytes of EEPROM, and 2Kbytes of RAM. Through its external memory bus, the FT 3150 smart transceiver can address up to 58Kbytes of external memory, of which 16Kbytes of external nonvolatile memory is dedicated to the Neuron firmware. The FT 3150 transceiver is supplied in a 64-lead TQFP package.

The embedded EEPROM may be written up to 10,000 times with no data loss. Data stored in the EEPROM will be retained for at least 10 years.[3]

Three different versions of the FT 3120 and FT 3150 Free Topology Smart Transceivers are available to meet a wide range of applications and packaging requirements. See FT 3120 and FT 3150 Free Topology Smart Transceiver Ordering Information below for product offerings and descriptions.

The FT-X1 is a through-hole communication transformer while the FT-X2 is a surface mount transformer. Either transformer can be used with the FT 3120 or FT 3150 Free Topology Smart Transceivers. the FT-X1 and FT-X2 transformers have similar noise immunity and performance characteristics.

Models 14212R-500, 14222R-800, 14230R-450, 14240R, and 14250R-300 are compliant with the European Directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

Flexible I/O, Simple Configuration

The FT 3120 and FT 3150 Free Topology Smart Transceivers provide 11 I/O pins which may be configured to operate in one or more of 34 predefined standard input/output modes. Combining a wide range of I/O models with two on-board timer/counters enable the FT 3120 and FT 3150 smart transceivers to interface to application circuits with minimal external logic or software development.

Easy Interface to Any Host MCU

The FT 3120 and FT 3150 Free Topology Smart Transceivers can be easily interfaced to other host MCUs via Echelon's ShortStack® or MIP firmware. When used with the ShortStack or MIP firmware, the Smart Transceiver enables any OEM product with a host microcontroller to quickly and inexpensively become a networked, Internet-accessible device. The ShortStack firmware uses an SCI or SPI serial interface to communicate between the host and the Smart Transceiver. The MIP uses a high performance parallel or dual-ported RAM interface.

Advanced Network Noise Protection

The FT 3120 and FT 3150 Free Topology Smart Transceivers are composed of two components — the FT 3120/FT 3150 IC and an external communication transformer. The transformer enables operation in the presence of high frequency common mode noise on unshielded twisted pair networks. Properly designed nodes can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective mag-

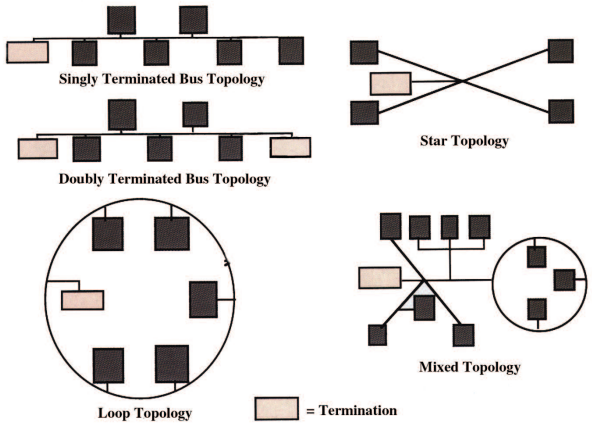


Figure 1. Typical Free Topologies Supported by the FT 3120 and FT 3150 Free Topology Smart Transceivers

Notes:

1 See table on FT 3120 and FT 3150 Free Topology Smart Transceiver Ordering Information for other product offerings and description.

2 The FT 3120 Free Topology Smart Transceiver is designed to run at frequencies up to 40MHz using an external clock oscillator. External oscillators may take several milliseconds to stabilize after power-up. The FT 3120 Free Topology Smart Transceiver operating at 40MHz should be held in reset until the CLK1 input is stable. With some oscillators, this may require the use of a power-on-reset-pulse stretching Low-Voltage Detection chip/circuit. Check the oscillator specifications for more information on startup stabilization times.

3 EEPROM programming must be limited to -25 to 85°C for a 10-year data retention over the -40 to 85°C operating temperature range.

4 Maximum junction temperature should not exceed 105ºC. Tjunction can be calculated as follows: Tjunction = TAmbient + V•I•θJA where θJA for 32-pin SOIC = 51°C/W, θJA for 44-pin TQFP = 43°C/W, and θJA for 64-pin TQFP = 44°C/W.

netic shields in most applications. The transformer is provided in a potted, 6-pin, through-hole plastic package.

FT-X1/FT-X2 Communication Transformers must be ordered separately. See FT 3120 and FT 3150 Free Topology Smart Transceiver Ordering Information for product offerings and descriptions. The FT 3120 / FT 3150 Free Topology Smart Transceiver IC and the FT-X1/FT-X2 Communication Transformer are designed to be used as a pair and therefore must be implemented together in all designs. No transformer other than the FT-X1 or FT-X2 Communication Transformer may be used with either the FT 3120 or FT 3150 Free Topology Smart Transceiver IC, or the smart transceiver warranty will be void.

A typical FT 3120 or FT 3150 based device requires a power source, crystal and an I/O interface to the device being controlled (see Figure 3 for a typical FT 3120 / FT 3150 based device).

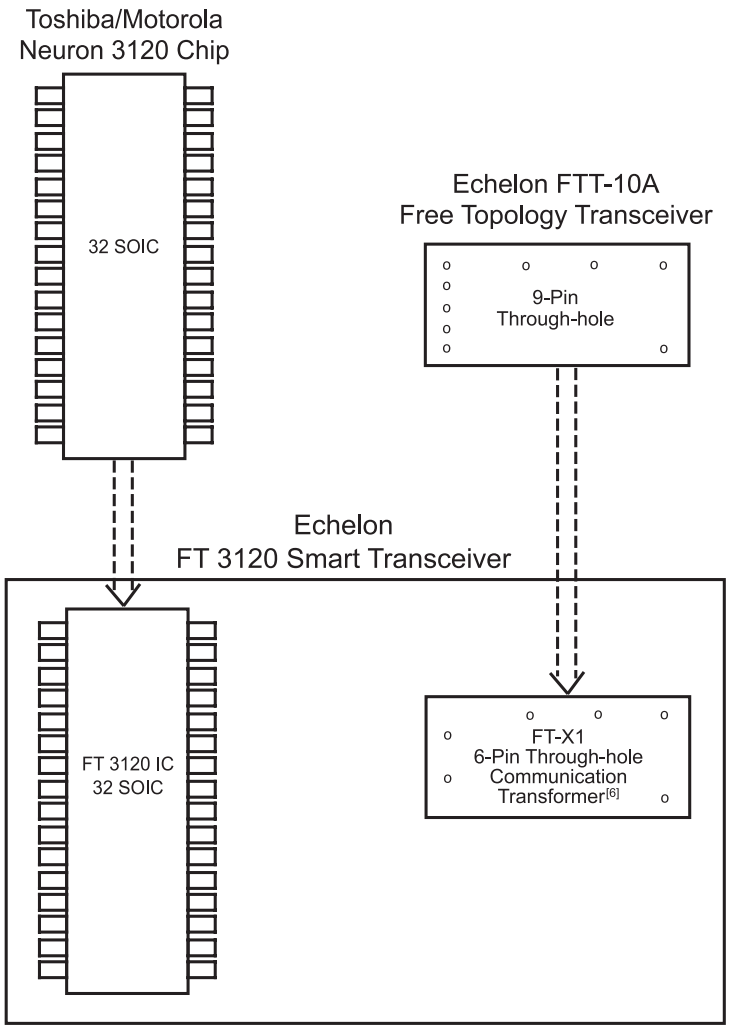


Figure 2. Upgrading to an FT 3120-E4S40 IC and FT-X1 Communication Transformer from a 32-pin SOIC Neuron 3120 Chip and FTT-10A

Notes:
5 Certain devices providing Rx packet detection LEDs may not be pin compatible with the FT 3120 and FT 3150 Free Topology Smart Transceiver. Contact Echelon for details.
6 The FT-X1/FT-X2 Communication Transformer must be ordered separately and must be used with the FT 3120 / FT 3150 Free Topology Smart Transceiver IC in all designs.

Figure 3. Typical FT 3120 / FT 3150 Free Topology Smart Transceiver based Node

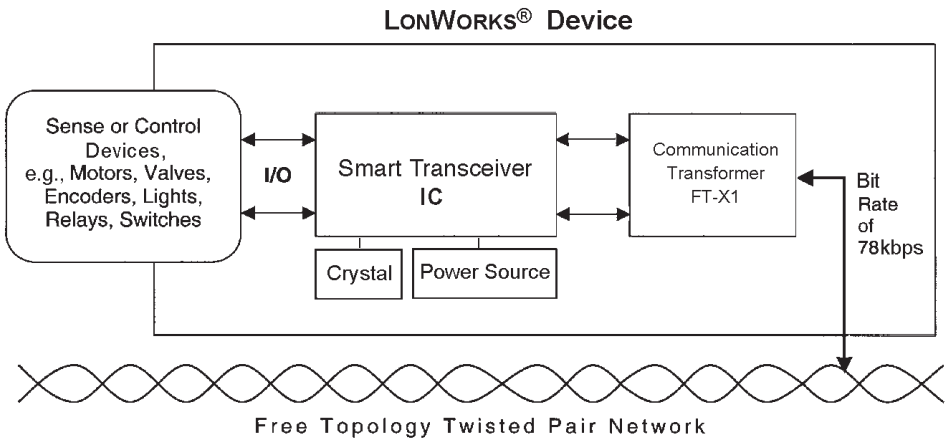


Figure 4. FT 3120 / FT 3150 Free Topology Smart Transceiver Block Diagram

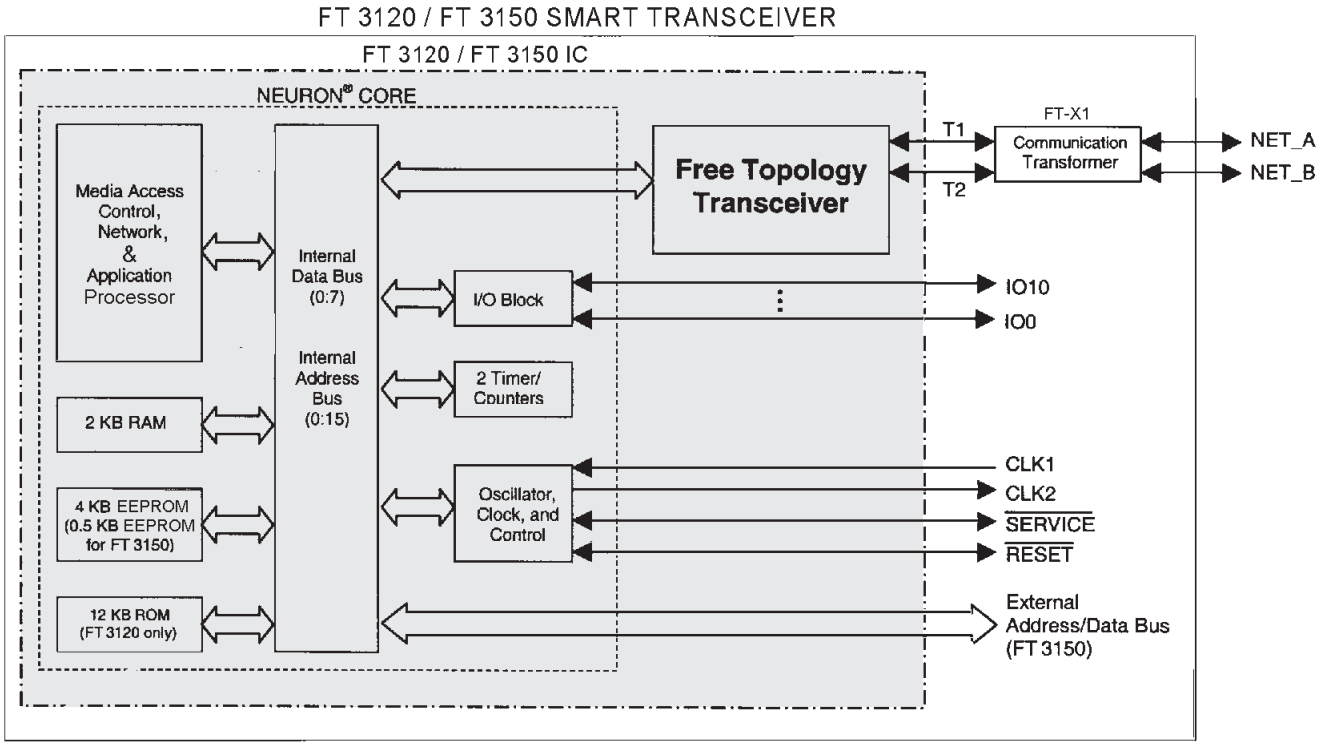


Figure 5. FT 3120 / FT 3150 Free Topology Smart Transceiver IC Pin Configurations

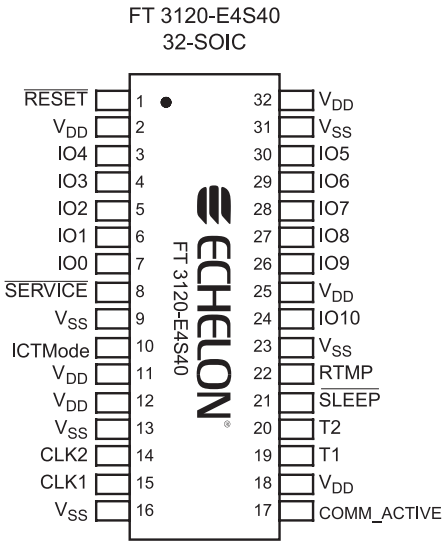


Figure 5a.

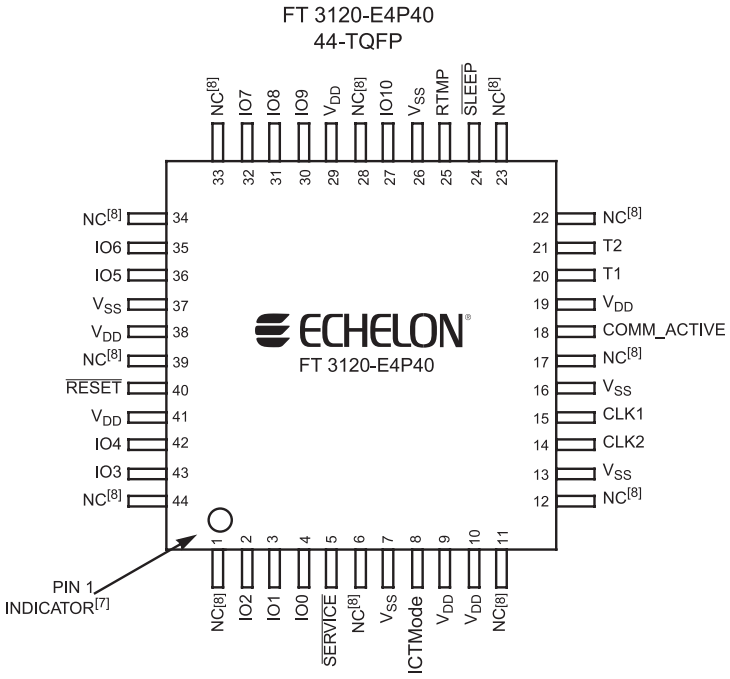


Figure 5b.

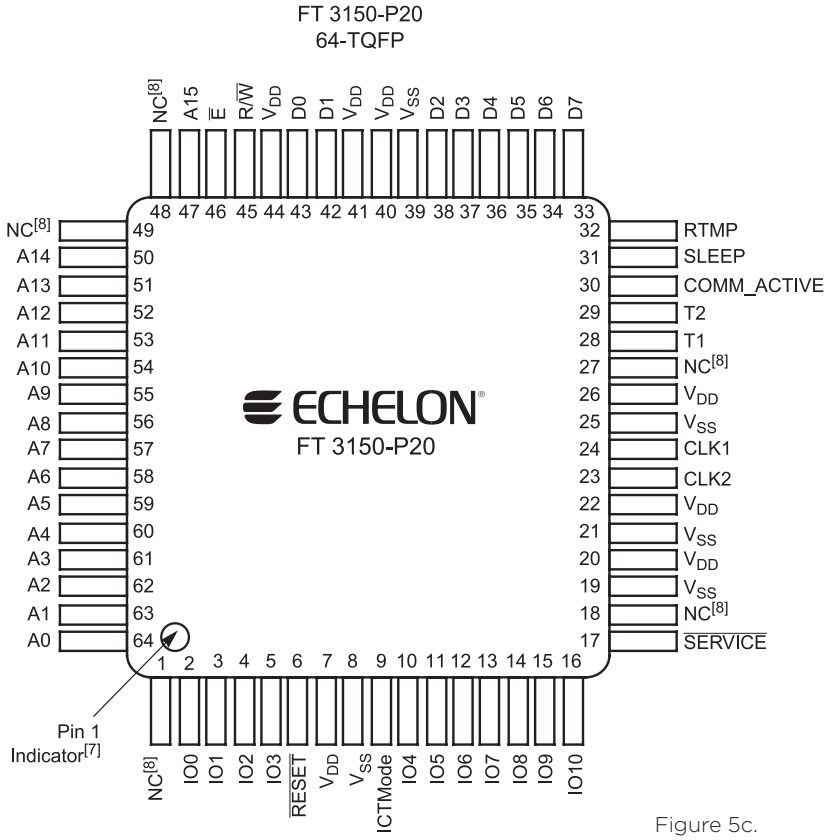


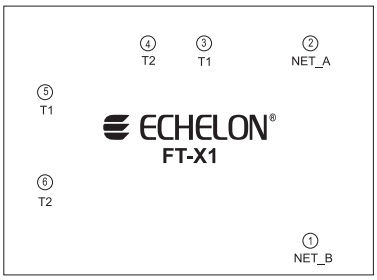
Figure 5c.

Notes:
7 The small dimple at the bottom left of the marking indicates pin 1.
8 NC (No Connect) — Should not be used. (These pins are reserved for internal testing.)

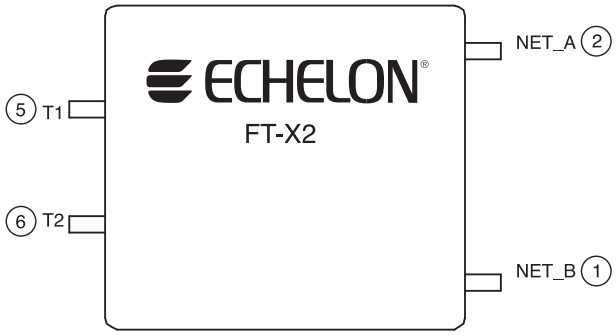
FT 3120 / FT 3150 Free Topology Smart Transceiver IC Pin Descriptions

Pin Name	Type	Pin Functions	FT 3150-P20 TQFP-64 Pin Number	FT 3120-E4S40 SOIC-32 Pin Number	FT 3120-E4P40 TQFP-44 Pin Number
CLK1	Input	Oscillator connection or external clock input.	24	15	15
CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1. Maximum of one external HCMOS equivalent load.	23	14	14
~~RESET~~	I/O (Built-in Pull-up)	Reset pin (active LOW). Note: The allowable external capacitance connected to the ~~RESET~~ pin is 100pF-1000pF.	6 1	40	
~~SERVICE~~	I/O (Built-in Configurable Pull-up)	Service pin (active LOW). Alternates between input and output at a 76Hz rate.	17 8	5	
IO0-IO3	I/O	Large current-sink capacity (20mA). General I/O port. The output of timer/counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5	7, 6, 5, 4	4, 3, 2, 43
IO4-IO7	I/O (Built-in Configurable Pull-up)	General I/O port. The input of timer/counter 1 may be derived from one of IO4-IO7. The input to timer/counter 2 may be derived from IO4.	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8-IO10	I/O	General I/O port. May be used for serial communication under firmware control.	14, 15, 16	27, 26, 24	31, 30, 27
D0-D7	I/O	Bi-directional memory data bus.	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
$\overline{R/W}$	Output	Read/write control output for external memory.	45	N/A	N/A
$\overline{E}$	Output	Enable clock control output for external memory.	46	N/A	N/A
A0-A15	Output	Memory address output port.	47, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 61, 62, 63, 64	N/A	N/A
V_{DD}	Power	Power input (5V nom). All V_{DD} pins must be connected together externally.	7, 20, 22, 26, 40, 41, 44	2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41
V_{SS}	Power	Power input (0V, GND). All V_{SS} pins must be connected together externally.	8, 19, 21, 25, 39	9, 13, 16, 23, 31	7, 13, 16, 26, 37
ICTMode	Input	In-circuit test mode control. Driving the ICTMode high and $\overline{RESET}$ low will put the device in the In-Circuit Test mode (all pins are placed in a high impedance state).	9	10	8
T1	I/O	Analog pin to be interfaced with T1 of the external transformer. Corresponds to CP0 on Toshiba and Cypress Neuron Chips.	28 19	20	
T2	I/O	Analog pin to be interfaced with T2 of the external transformer. Corresponds to CP1 on Toshiba and Cypress Neuron Chips.	29 20	21	
COMM_ACTIVE	Output	May be used to monitor, transmit/receive activity. Driven high during data transmissions, driven low when receiving data and kept at high impedance otherwise.	30	17	18
~~SLEEP~~	Output	~~SLEEP~~. May be configured as an output to indicate when the FT 3120 / FT 3150 is in sleep mode. Corresponds to CP3 on Toshiba and Cypress Neuron Chips.	31	21	24
RTMP	Input	Reserved for future use. Must be pulled up to 5V. Corresponds to CP4 on Toshiba and Cypress Neuron Chips.	32	22	25
NC	—	No connect. Must be left open.	1, 18, 27, 48, 49	N/A	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

FT-X1 Communication Transformer Pin Configuration



FT-X2 Communication Transformer Pin Configuration



FT-X1/FT-X2 Communication Transformer Pin Descriptions

Pin Name	Pin Function	Transformer Pin Number
NET_B	Network Port, polarity Insensitive	1
NET_A	Network Port, polarity Insensitive	2
T1	Internally connects to pin 5. Alternate connection to T1 pin on the FT 3120 / FT 3150 IC. Corresponds to the RXD pin on the FTT-10A (for replacement with FT-X1).	3 (Not used on FT-X2)
T2	Internally connects to pin 6. Alternate connection to T2 pin on the FT 3120 / FT 3150 IC. Corresponds to the TXD pin on the FTT-10A (for replacement with FT-X1).	4 (Not used on FT-X2)
T1	Connects to the ESD/transient protection circuitry and T1 pin on the FT 3120 / FT 3150 IC. Internally connects to pin 3 of the FT-X1. Corresponds to the T1 pin on the FTT-10A (for replacement with FT-X1).	5
T2	Connects to the ESD/transient protection circuitry and T2 pin on the FT 3120 / FT 3150 IC. Internally connects to pin 4 of the FT-X1. Corresponds to the T2 pin on the FTT-10A (for replacement with FT-X1).	6

Electrical Characteristics (VDD = 4.75-5.25V)

Parameter	Description		Min.	Max.	Unit	
V_{IL}	Input Low Voltage IO0-IO10, SERVICE, D0-D7, RESET			 0.8	V	
V_{IH}	Input High Voltage IO0-IO10, SERVICE, D0-D7, RESET		 2.0		V	
V_{OL}	Low-Level Output Voltage I_{out} < 20µA Standard Outputs (I_{OL} = 1.4 mA)[9] High Sink (IO0-IO3), SERVICE, RESET (I_{OL} = 20 mA) High Sink (IO0-IO3), SERVICE, RESET (I_{OL} = 10 mA) Maximum Sink (COMM_ACTIVE) (I_{OL} = 40 mA) Maximum Sink (COMM_ACTIVE) (I_{OL} = 15 mA)			 0.1 0.4 0.8 1.0 0.4	V 0.4 	
V_{OH}	High-Level Output Voltage I_{out} < 20µA Standard Outputs (I_{OH} = -1.4 mA)[9] High Sink (IO0-IO3), SERVICE (I_{OH} = -1.4 mA) Maximum Sink (COMM_ACTIVE) (I_{OL} = -40 mA) Maximum Sink (COMM_ACTIVE) (I_{OL} = -15 mA)		 V_{DD} - 0.1 V_{DD} - 0.4 V_{DD} - 0.4 V_{DD} - 1.0 V_{DD} - 0.4		V	
V_{hys}	Hysteresis (Excluding CLK1)		175		mV	
I_{in}	Input Current (Excluding Pull-ups) (V_{SS} to V_{DD})[10]			+/- 10	µA	
I_{pu}	Pull-up Source Current (V_{out} = 0 V, Output = High-Z)[10]		60	260	µA	
I_{DD}	Operating Mode Supply Current [11, 12]	40MHz Clock	$I_{DD(receive)}$	60	mA	
			$I_{DD(transmit)}$	75	mA	
		20MHz Clock	$I_{DD(receive)}$	42	mA	
			$I_{DD(transmit)}$	57	mA	
		10MHz Clock	$I_{DD(receive)}$	35	mA	
			$I_{DD(transmit)}$	50	mA	
		5MHz Clock	$I_{DD(receive)}$	20	mA	
			$I_{DD(transmit)}$	35	mA	

LVI Trip Point (VDD)

Part Number	Min.	Typ.	Max.	Unit
FT 3120 and FT 3150	3.8	4.1	4.4	V

External Memory Interface Timing — FT 3150
(VDD = 4.75 to 5.25 V, TA = -40 to +85 C)[3]

See Figures 7 through 12 for detailed measurement information)

Parameter	Description	C_L	Min.	Max.	Unit
tcyc	Memory Cycle Time (System Clock Period)		100	400	ns
PW_{EH}	Pulse Width, E High[13]		$t_{cyc}/2$ - 5	tcyc/2 + 5	ns
PW_{EL}	Pulse Width, E Low		$t_{cyc}/2$ - 5	tcyc/2 + 5	ns
t_{AD}	Delay, E High to Address Valid	30ρF		35	ns
		50ρF		45	
t_{AH}	Address Hold Time After E High	≥30ρF	10		ns
t_{RD}	Delay, E High to R/W Valid Read	30ρF		25	ns
		50ρF		45	
t_{RH}	R/W Hold Time Read After E High	≥30ρF	5		
t_{WR}	Delay, E High to R/W Valid Write	30ρF		25	ns
		50ρF		45	
t_{WH}	R/W Hold Time Write After E High	≥30ρF	5		
t_{DSR}	Read Data Setup Time to E High	30ρF	15		ns
		50ρF	25		
t_{DHR}	Data Hold Time Read After E High	≥30ρF	0		
t_{DHW}	Data Hold Time Write After E High[14]	≥30ρF	10		
t_{DDW}	Delay, E Low to Data Valid	30ρF		12	ns
		50ρF		60	
tacc[15]	External Read Access Time ($t_{acc} = t_{cyc} - t_{AD} - t_{DSR}$) at 20MHz Input Clock	30ρF		50	ns
tacc[15]	External Read Access Time ($t_{acc} = t_{cyc} - t_{AD} - t_{DSR}$) at 10MHz Input Clock	50ρF		130	ns

Notes:
9 Standard outputs are IO4-IO10. (RESET is an open drain input/output. CLK2 must have ☒ 15pF load.) For FT 3150, standard outputs also include A0-A15, D0-D7, E, and R/W.
10 IO4-IO7 and SERVICE have configurable pull-ups. RESET has a permanent pull-up.
11 Supply current measurement conditions: all outputs under no-load conditions, all inputs ☒ 0.2V or ☒ (VDD - 0.2V), configurable pull-ups off and crystal oscillator clock input disabled.
12 Maximum supply current values are at midpoint of supply voltage range.
13 tcyc = 2/f where f is the input clock (CLK1) frequency (20, 10, or 5 MHz).
14 The data hold parameter, tDHW, is measured to disable levels shown in Figure 12, rather than to the traditional data invalid levels.
15 This parameter considers only the memory read access time from address to data. This does not allow for chip enable decode. A more thorough analysis should be performed for any given design.

External Memory Interface Timing Diagram

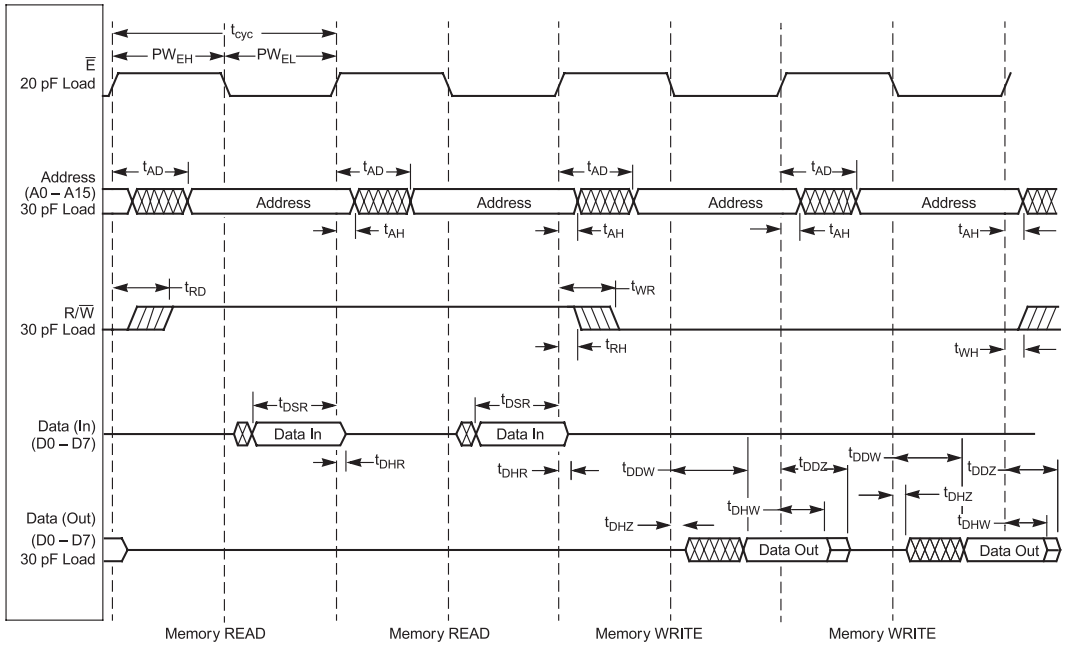
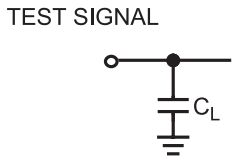


Figure 7



C_L = 20 pF for $\overline{E}$

C_L as specified in table for all other signals

Figure 8

Signal Loading for Timing Specifications

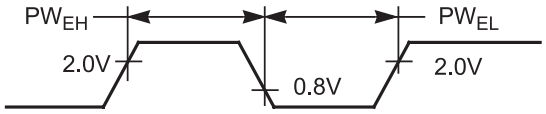


Figure 9

Test Point Levels for E Pulse Width Measurements

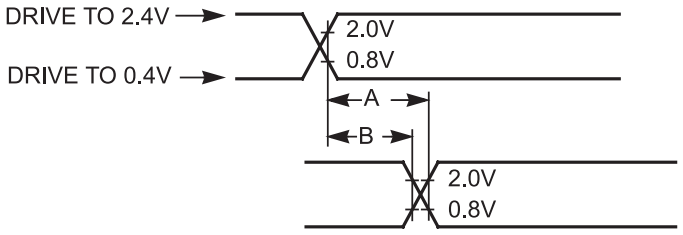


Figure 10

A — Signal valid-to-signal valid specification (maximum or minimum)
B — Signal valid-to-signal invalid specification (maximum or minimum)

Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified

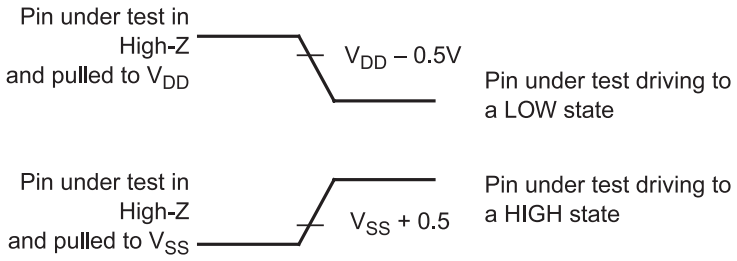


Figure 11

Test Point Levels for High Impedence-to-Driven Time Measurements

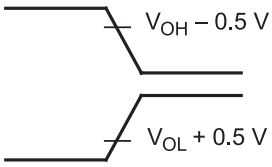


Figure 12

V_{OH} – Measured high output drive level
V_{OL} – Measured low output drive level

Test Point Levels for Driven-to High Impedence Time Measurements

Recommended FT 3120 / FT 3150 Free Topology Smart Transceiver IC Pad Layouts

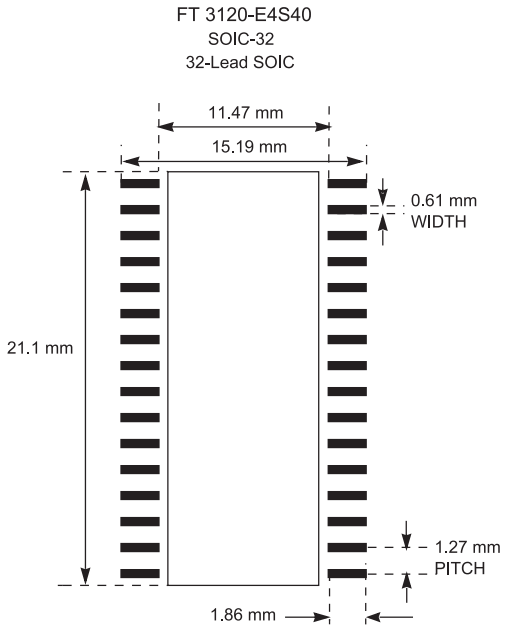


Figure 13a

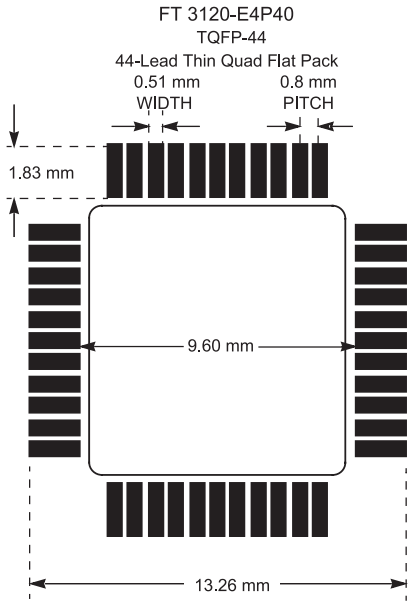


Figure 13b

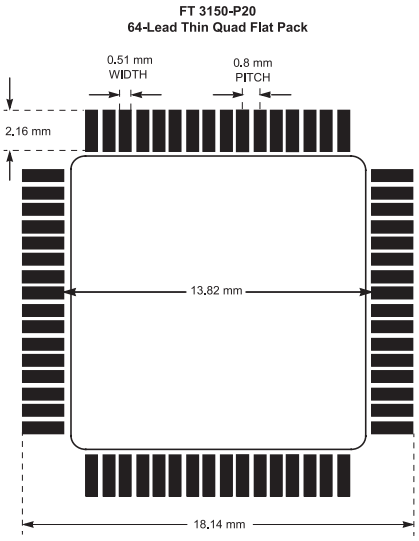


Figure 13c

Recommended FT-X2 Pad Layout (4 pins)

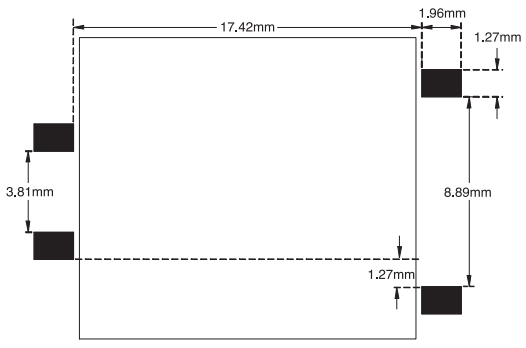


Figure 14

FT 3120 / FT 3150 Free Topology Smart Transceiver IC Package Diagrams

32-Lead (450 MIL) Molded SOIC S34

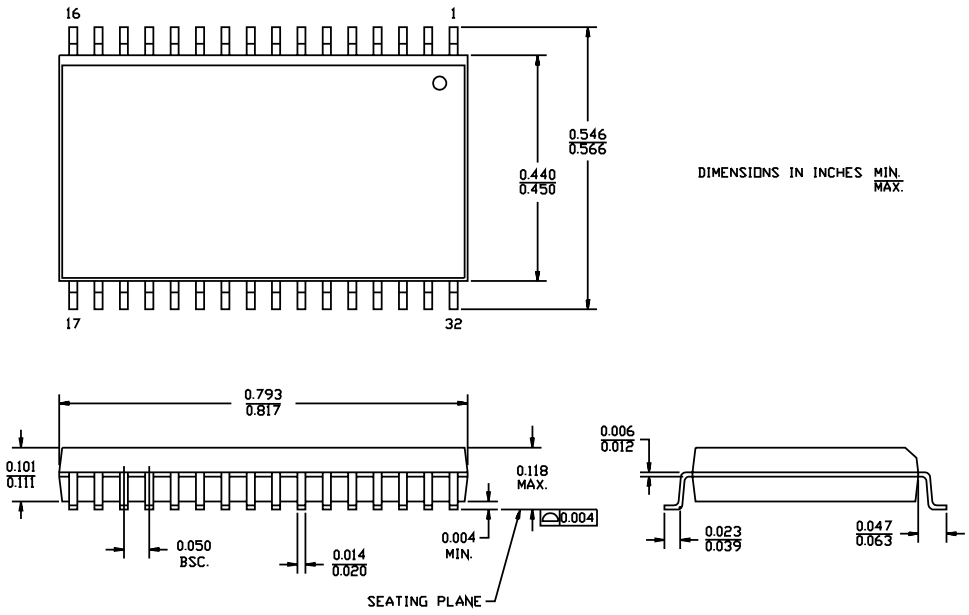


Figure 15a

44-Lead Thin Plastic Quad Flat Pack A44

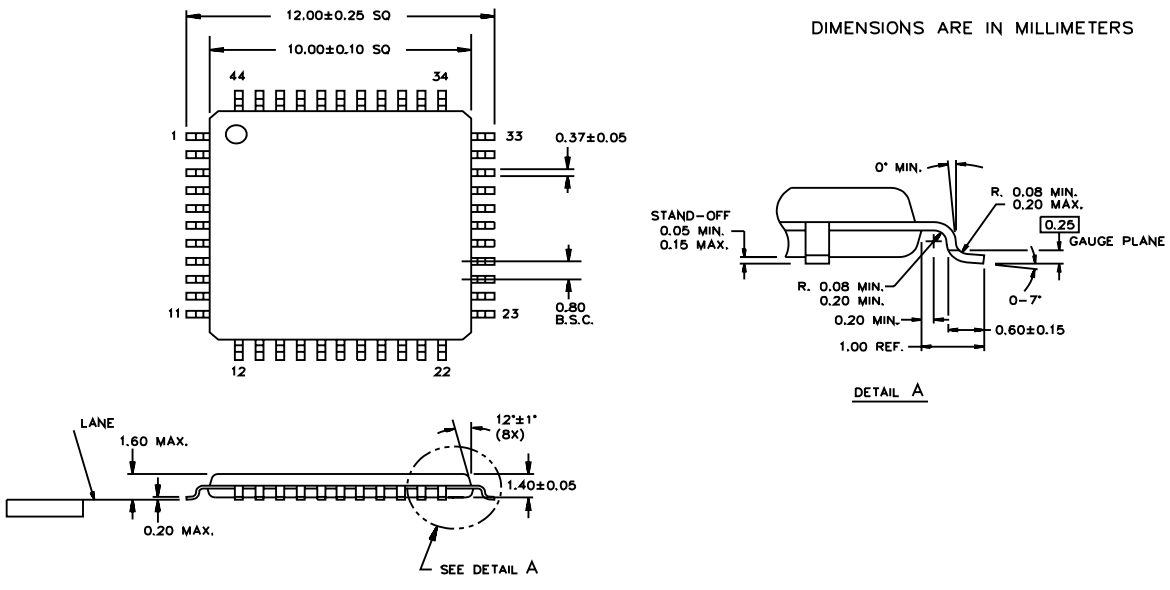
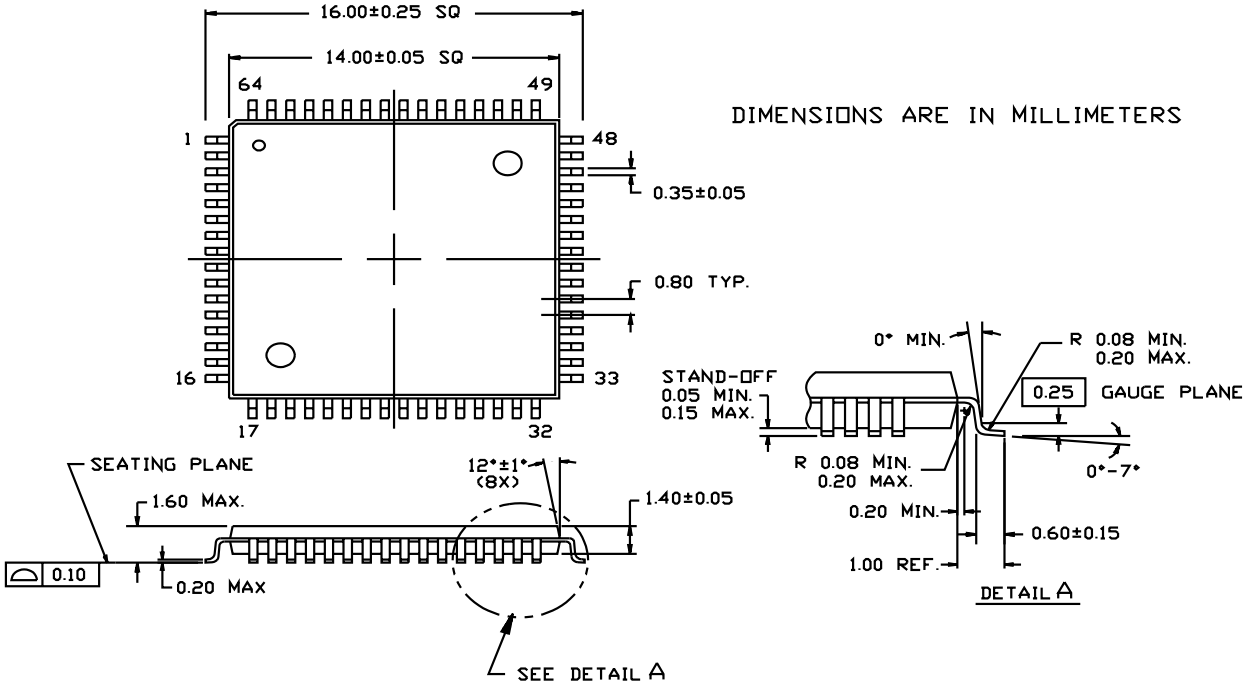


Figure 15b

64-Lead Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm) A65



FT-X1 Communication Transformer Top View

(Dimensions in mm)

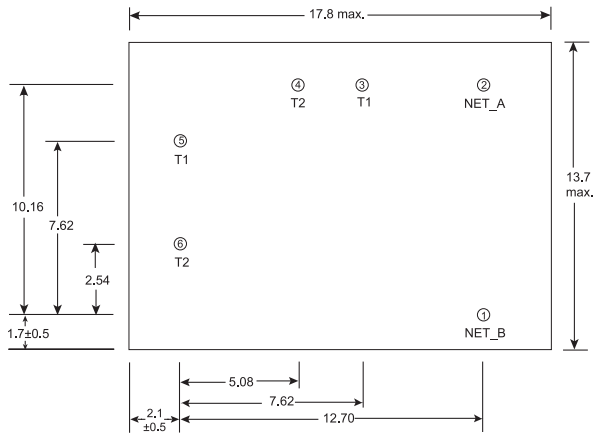


Figure 16a

FT-X1 Communication Transformer Side View

(Dimensions in mm)

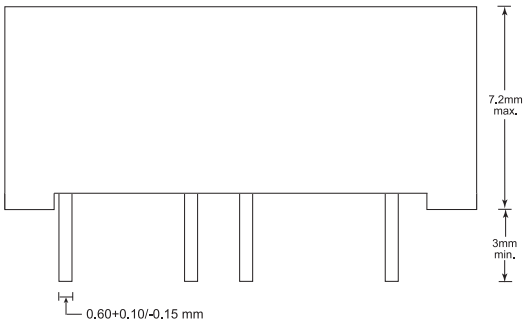


Figure 16b

FT-X2 Communication Transformer SMT Package Diagram

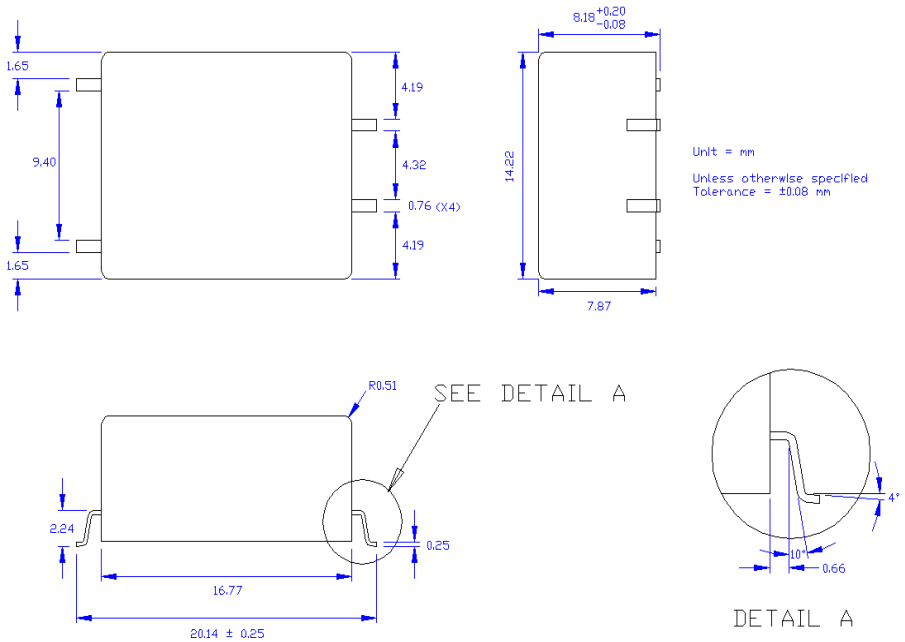


Figure 17

General Specifications

Data Communications Type	Differential Manchester coding
Network Polarity	Polarity insensitive
Isolation Between Network and	
0-60Hz, 60 seconds	1000Vrms
0-60Hz, continuous	277Vrms[16]
EMI	Designed to comply with FCC Part 15 Level B and EN55022 Level B
ESD	Designed to comply with EN 61000-4-2, Level 4
Radiated Electromagnetic Susceptibility	Designed to comply with EN 61000-4-3, Level 3
Fast Transient/Burst Immunity	Designed to comply with EN 61000-4-4, Level 4
Surge Immunity	Designed to comply with EN 61000-4-5, Level 3
Conducted RF Immunity	Designed to comply with EN 61000-4-6, Level 3
Safety Approvals (FT-X1/FT-X2 Communication Transformer)	Recognized by UL to Standards UL 60950, 2000 and CSA C22.2 No. 60950, 2000 Recognized by TÜV EN 60950
Transmission Speed	78 kilobits per second
Number of Transceivers Per Segment	Up to 64
Network Wiring	24 to 16AWG twisted pair; see User's Guide or *Junction Box and Wiring Guidelines* application note for qualified cable types
Network Length in Free Topology[17]	1000m (3,280 feet) maximum total wire with one repeater 500m (1,640 feet) maximum total wire with no repeaters 500m (1,640 feet) maximum device-to-device distance
Network Length in Doubly Terminated Bus Topology[17]	5400m (17,710 feet) with one repeater 2700m (8,850 feet) with no repeaters

General Specifications (continued)

Maximum Stub Length in Doubly-Terminated Bus Topology	3m (9.8 feet)
Network Termination	One terminator in free topology; two terminators in bus topology (see *FT 3120 / FT 3150 Free Topology Smart Transceiver Data Book*)
Power-down Network Protection	High impedance when unpowered
Physical Layer Repeater	The FT 3120/FT 3150 Free Topology Smart Transceiver cannot be used to implement a physical layer repeater. In the event that the limits on the number of transceivers or total wire distance are exceeded, FTT-10A transceivers may be used to create physical layer repeaters. See *FTT-10A Free Topology Transceiver User's Guide* for more details.
Operating Temperature	-40 to 85°C[3]
Operating Humidity	25-90% RH @50°C, non-condensing
Non-operating Humidity	95% RH @ 50°C, non-condensing
Vibration	1.5g peak-to-peak, 8Hz-2kHz
Mechanical Shock	100g (peak)
Reflow Soldering Temperature Profile	Refer to Joint Industry Standard document *IPC/JEDEC J-STD-020C* (July 2004)
Peak Reflow Soldering Temperature	220ºC (Models 14210-500 and 14211-500) 235ºC (Models 14220-800, 14221-800, and 14230-450) 245ºC (Model 14212R-500) 260ºC (Models 14222R-800 and 14230R-450) 245ºC (FT-X2 Model 14250R-300)

Ordering Information

(**Note:** The FT 3120/FT 3150 Free Topology Smart Transceiver IC and the FT-X1/FT-X2 Communication Transformer must be ordered in the same quantities.)

The following tables lists the non-RoHS compliant Free Topology Smart Transceivers. These products will be discontinued after Q4 2005.

Free Topology Smart Transceiver IC Product Number	Model Number	Firmware Version	Maximum Input Clock	EEPROM	RAM	ROM	External Memory Interface	IC Package	(Factory Default On-Chip) Data Comm Parameters
FT 3120-E4S40	14210-500	v13	40MHz	4K Bytes	2K Bytes	12K Bytes	No	32 SOIC	TP/XF-1250
FT 3120-E4S40	14211-500	v13	40MHz	4K Bytes	2K Bytes	12K Bytes	No	32 SOIC	TP/FT-10 @ 10MHz
FT 3120-E4P40	14220-800	v13	40MHz	4K Bytes	2K Bytes	12K Bytes	No	44 TQFP	TP/XF-1250
FT 3120-E4P40	14221-800	v13	40MHz	4K Bytes	2K Bytes	12K Bytes	No	44 TQFP	TP/FT-10 @ 10MHz
FT 3150-P20	14230-450	N/A	20MHz	0.5K Bytes	2K Bytes	N/A	Yes	64 TQFP	N/A

Free Topology Smart Transceiver IC Product Number	Model Number	Firmware Version	Maximum Input Clock	EEPROM	RAM	ROM	External Memory Interface	IC Package	(Factory Default On-Chip) Data Comm Parameters
FT 3120-E4S40	14212R-500	v16	40MHz	4K Bytes	2K Bytes	12K Bytes	No	32 SOIC	TP/FT-10 @ 10MHz
FT 3120-E4P40	14222R-800	v16	40MHz	4K Bytes	2K Bytes	12K Bytes	No	44 TQFP	TP/FT-10 @ 10MHz
FT 3150-P20	14230R-450	N/A	20MHz	0.5K Bytes	2K Bytes	N/A	Yes	64 TQFP	N/A

Notes:
16 Safety agency hazardous voltage barrier requirements are not supported.
17 Network segment length varies depending on wire type. See Junction Box and Wiring Guidelines application note for detailed specifications.