ECHELON

FT 5000 Smart Transceiver
FT-X3 Communications Transformer

The Next-generation Free Topology Smart Transceiver

The FT 5000 Smart Transceiver is our next-generation chip for smart networks. It is the key product in the LONWORKS® 2.0 platform—the next generation of LONWORKS products designed to greatly increase the power and capability of LONWORKS enabled devices, while lowering development and node costs.

The FT 5000 Smart Transceiver integrates a high-performance Neuron® Core with a free topology twisted-pair transceiver. Combined with the new low-cost FT-X3 Communications Transformer and inexpensive serial memory, the FT 5000 Smart Transceiver provides a lower-cost, higher-performance LONWORKS solution than previous-generation FT Smart Transceivers.

FEATURES

- 3.3V operation.
- Higher-performance Neuron® Core — internal system clock scales up to 80MHz.
- Substantial device price reduction.
- Serial memory interface for inexpensive external EEPROM and flash non-volatile memories.
- Supports up to 254 Network Variables (NVs) and 127 aliases.
- Low-cost surface mount FT-X3 Communications Transformer.
- User-programmable interrupts provide faster response time to external events.
- Includes hardware UART with 16-byte receive and transmit FIFOs.
- 7 mm x 7 mm 48-pin QFN package.
- Supports polarity-insensitive free topology star, daisy chain, bus, loop, or mixed topology wiring.
- Compliant with TP/FT-10 channels using FT 3120®/FT 3150® Smart Transceivers and FTT-10/FTT-10A/ LPT-10/LPT-11 Transceivers.
- 12 I/O pins with 35 programmable standard I/O models.
- Supports up to 42KB of application code space.
- 64KB RAM (44KB user-accessible) and 16KB ROM on-chip memories.
- Unique 48-bit Neuron ID in every device for network installation and management.
- Very high common-mode noise immunity.
- -40°C to +85°C operating temperature range.

DESCRIPTION

The FT 5000 Smart Transceiver includes three independent 8-bit logical processors to manage the physical MAC layer, the network, and the user application. These are called the Media-Access Control (MAC) processor, the network (NET) processor, and the application (APP) processor, respectively (see Figure 1). At higher system clock rates, there is also a fourth processor to handle interrupts.

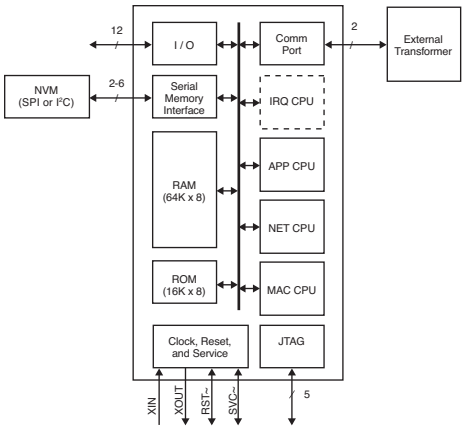


Figure 1: FT 5000 Smart Transceiver Chip

The FT 5000 Smart Transceiver supports polarity-insensitive cabling using a star, bus, daisy-chain, loop, or combination topology (see Figure 2). Thus, installers don't have to follow a strict set of wiring rules imposed by other networking technologies. Instead, they can install wiring in the fastest and most cost-effective manner, thereby saving time and money. Free topology wiring also simplifies network expansion by eliminating restrictions on wire routing, splicing, and device placement.

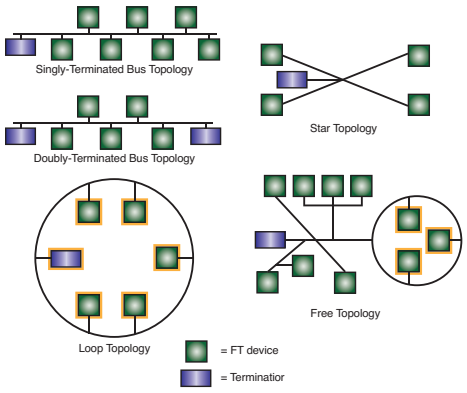


Figure 2: Free Topology Network Configurations

The FT-X3 Communications Transformer is a surface mount communications transformer that's compatible with both the FT 5000 Smart Transceiver and the previous-

generation FT 3120/FT 3150 Smart Transceivers. The FT-X3 Communications Transformer provides equivalent noise immunity to both the FT-X1 and FT-X2 Communication Transformers, the previous-generation communication transformers. However, the FT-X3 Communications Transformer is not pin-compatible with the FT-X2 Communication Transformer (which is also a surface mount transformer). The FT 5000 Smart Transceiver can also be used with the FT-X1 and FT-X2 Communication Transformers.

Backward Compatibility

The FT 5000 Smart Transceiver is fully compliant with the TP/FT-10 channel and can communicate with devices that use Echelon's FTT-10/FTT-10A Transceivers, FT 3120/FT 3150 Smart Transceivers, or LPT-10/LPT-11 Link Power Transceivers.

The Neuron Core in the FT 5000 Smart Transceiver uses the same instruction set and architecture as the previous-generation Neuron Core, with two new additional instructions for hardware multiplication and division. The Series 5000 Neuron Core is source code compatible with applications written for the Series 3100 Neuron Core. Applications written for the Series 3100 Neuron Core must be recompiled with the NodeBuilder® FX Development Tool or the Mini FX Evaluation Kit before they can be used with the FT 5000 Smart Transceiver.

The FT 5000 Smart Transceiver uses Neuron firmware version 19. Firmware versions prior to version 19 are not compatible with the FT 5000 Smart Transceiver. The Neuron firmware is pre-programmed into the on-chip ROM. The FT 5000 Smart Transceiver can also be configured to read newer firmware from external memories, allowing the firmware to be upgraded over time.

Enhanced Performance

Faster system clock. The internal system clock for the FT 5000 Smart Transceiver can be user-configured to run from 5MHz to 80MHz. The required external crystal provides a 10MHz clock frequency, and an internal PLL boosts the frequency to a maximum of 80MHz as the internal system clock speed. The previous-generation Neuron 3120/3150 Core divided the external oscillator frequency by two to create the internal system clock. An FT 5000 Smart Transceiver running with an 80MHz internal system clock is thus 16 times faster than a 10MHz Neuron 3120/3150 Core running.

The 5MHz internal system clock mode in the FT 5000 Smart Transceiver provides backward compatibility to support timing-critical applications designed for the 10MHz FT 3150 or FT 3120 Smart Transceiver.

The Neuron Core inside the FT 5000 Smart Transceiver includes a built-in hardware multiplier and divider to increase the performance of arithmetic operations.

Support for more network variables. Because it uses Neuron firmware version 19, the FT 5000 Smart Transceiver supports applications with up to 254 network variables and 127 aliases for Neuron hosted devices (devices without a host microprocessor). A Series 3100 Neuron Chip or Smart Transceiver with Neuron firmware version 15 or earlier supports up to 62 network variables and 62 aliases for Neuron hosted devices. Series 3100 chips with Neuron firmware version 16 or later support up to 254 network variables. You must use the NodeBuilder FX Development Tool to take advantage of 254 network variables.

Interrupts. The FT 5000 Smart Transceiver lets developers define application interrupts to handle asynchronous events triggered by selected state changes on any of the 12 I/O pins, by on-chip hardware timer-counter units, or by an on-chip high-performance hardware system timer. An application uses the Neuron C **interrupt()** clause to define the interrupt condition and the interrupt task that handles the condition. The Neuron C program runs the interrupt task whenever the interrupt condition is met. See the *Neuron C Programmer's Guide* for more information about writing interrupt tasks and handling interrupts.

JTAG. The FT 5000 Smart Transceiver provides an interface for the Institute of Electrical and Electronics Engineers (IEEE) Standard Test Access Port and Boundary-Scan Architecture (IEEE 1149.1-1990) of the Joint Test Action Group (JTAG) to allow a Series 5000 chip to be included in the boundary-scan chain for device production tests. A Boundary Scan Description Language (BSDL) file for the FT 5000 Smart Transceiver can be downloaded from Echelon's Web site.

I/O Pins and Counters

The FT 5000 Smart Transceiver provides 12 bidirectional I/O pins that are 5V-tolerant and can be configured to operate in one or more of 35 predefined standard input/output models. The chip also has two 16-bit timer/counters that reduce the need for external logic and software development.

Memory Architecture

The FT 5000 Smart Transceiver uses inexpensive external serial EEPROM and flash memories for non-volatile application and data storage, and optionally for future Neuron firmware upgrades. It has 16KB of ROM and 64KB (44KB user-accessible) of RAM on the chip. It has no on-chip non-volatile memory (EEPROM or flash) for application use. Each chip, however, contains its unique Neuron identifier (Neuron ID) in an on-chip, non-volatile, read-only memory.

The application code and configuration data are stored in the external non-volatile memory (NVM) and copied into the internal RAM during device reset; the instructions then execute from internal RAM. Writes to NVM are shadowed in the internal RAM and pushed out to external NVM by the Neuron firmware (see Figure 2). The application does not manage NVM directly.

External memories supported. The FT 5000 Smart Transceiver supports two serial interfaces for accessing off-chip, non-volatile memories: serial Inter-Integrated Circuit (I2C) and serial peripheral interface (SPI). EEPROM and flash memory devices can use either the I2C interface or the SPI interface. However, at the time of publication, there are no serial flash parts that use the I2C protocol and meet the required specifications for the Series 5000 external memory interface.

External serial EEPROMs and flash devices, which are inexpensive and come in very small form factors, are available from multiple vendors.

The FT 5000 Smart Transceiver requires at least 2KB of off-chip memory available in an EEPROM device to store the configuration data. The application code can be stored either in the EEPROM (by using a larger-capacity EEPROM device) or in a flash memory device used in addition to the 2KB (minimum) EEPROM. Thus, the external memory for the FT 5000 Smart Transceiver has one of the configurations listed in Table 1:

Configu-ration	EEPROM		Flash	Comments
	I²C	SPI	SPI	
1	☑			A single I²C EEPROM memory device, from 2KB to 64KB in size.
2	☑		☑	One I²C EEPROM (at least 2KB in size, up to 64KB in size, but the system uses only the first 2KB of the EEPROM memory). One SPI flash memory device.
3		☑		A single SPI EEPROM memory device, from 2KB to 64KB in size.
4		☑	☑	One SPI EEPROM (at least 2KB in size, up to 64KB in size, but the system uses only the first 2KB of the EEPROM memory). One SPI flash memory device.

Table 1: Allowed External Memory Device Configurations

As Table 1 shows, the FT 5000 Smart Transceiver supports using a single EEPROM memory device, or a single EEPROM memory device plus a single flash memory device.

If the FT 5000 Smart Transceiver detects an external flash memory device, the flash memory represents the entire user non-volatile memory for the device. That is, any additional EEPROM memory beyond the mandatory 2KB is not used.

Using the I²C interface. When using the I²C interface for external EEPROM, the FT 5000 Smart Transceiver is always the master I²C device (see Figure 3). The clock speed supported for the I²C serial memory interface is 400kHz (fast I²C mode). The I²C memory device must specify I²C address 0. Both 1-byte and 2-byte address modes are supported, but 3-byte addressing mode is not.

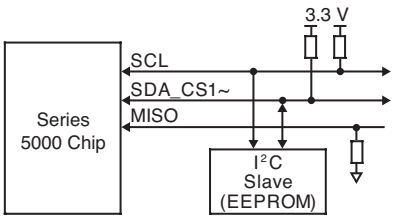


Figure 3: Using the I²C Interface for External NVM EEPROM Memory

Using the SPI interface. The FT 5000 Smart Transceiver is always the master SPI device; any external NVM devices are always slave devices. The FT 5000 Smart Transceiver can support up to two SPI slave devices from the serial memory interface: one EEPROM device at CS0~ and one flash device at CS1~ (see Figure 4). The FT 5000 Smart Transceiver supports 2-byte addressing mode for SPI EEPROM devices, but does not support 3-byte addressing. The FT 5000 Smart Transceiver runs the SPI protocol from the serial memory interface at 2.5 MHz and supports SPI Mode 0. In Mode 0, the base value of the clock is zero; the data is read on the clock's rising edge and changed on the clock's falling edge. Most external NVMs support SPI Mode 0 and 3.

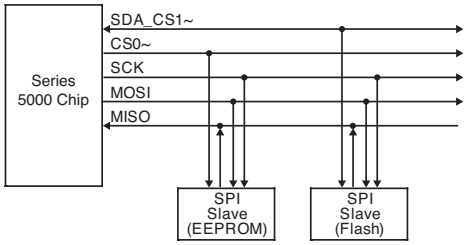


Figure 4: Using the SPI Interface for External NVM Memories

Using both I²C and SPI interfaces. Figure 5 shows an FT 5000 Smart Transceiver that includes both an I²C memory device (a 2KB EEPROM device) and a SPI memory device (a flash memory device). Although both EEPROM and flash memory share the SDA_CS1~ pin, there is no conflict because only one of them can be active at a time. SDA is an active high signal and CS1~ is an active low signal. While small applications could use EEPROM both for application code and configuration data, larger applications might find it economical to use a small EEPROM for configuration data and a flash device for application code. The choice between EEPROM and flash can be affected by multiple factors, including:

- Use of a single external memory versus two memories.
- Cost comparison between a large EEPROM device and a combination of a small EEPROM and large flash devices.
- Use of non-volatile variables by the application, which can require a large number of writes to the device.

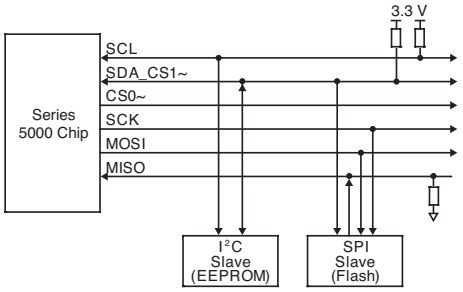


Figure 5: Using both I²C and SPI Interfaces for External NVM Memories

Memory devices supported. The FT 5000 Smart Transceiver supports any EEPROM device that uses the SPI or I²C protocol, and meets the clock speed and addressing requirements described above. While all EEPROM devices have a uniform write procedure, flash devices from various manufacturers differ slightly in their write procedure. Thus, a small library routine is stored in the external EEPROM device that helps the system write successfully to the external flash device. Echelon has qualified the following SPI flash memory devices for use with the FT 5000 Smart Transceiver:

- Atmel® AT25F512B 512-Kilobit 2.7-volt Minimum SPI Serial Flash Memory.
- Numonyx™ M25P05-A 512-Kbit, serial flash memory, 50MHz SPI bus interface.
- Silicon Storage Technology SST25VF512A 512 Kbit SPI Serial Flash.

Additional devices may be qualified in the future.

Memory map. An FT 5000 Smart Transceiver has a memory map of 64KB. A Neuron C application program uses this memory map to organize its memory and data access. The memory map is a logical view of device memory, rather than a physical view, because the chip's processors only directly access RAM. The memory map divides the FT 5000 Smart Transceiver's physical 64KB RAM into the following types of logical memory, as shown in Figure 6:

- Neuron firmware image (stored in on-chip ROM or external NVM).
- On-chip RAM or NVM. Memory ranges for each are configurable within the device hardware template. The non-volatile memory represents the area shadowed from external NVM into the RAM.
- On-chip RAM for stack segments and RAMNEAR data.

- Mandatory external EEPROM that holds configuration data and non-volatile application variables.
- Reserved space for system use.

If a 64KB external serial EEPROM or flash device is used, the maximum allowed size of application code is 42KB as defined by extended NVM area in the memory map. An additional 16KB of the remaining space can hold an external system firmware image, in case a future firmware upgrade is required.

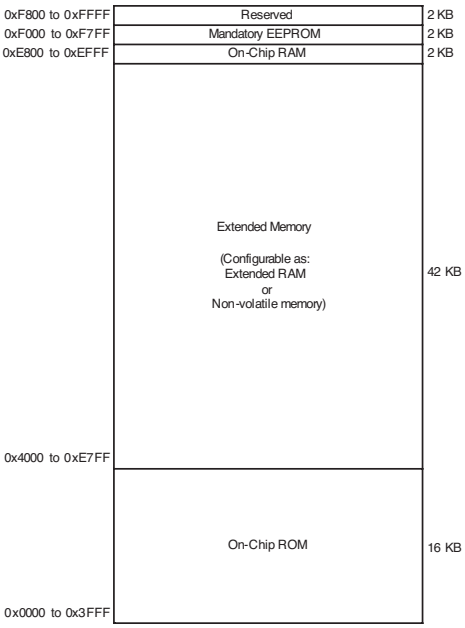


Figure 6: FT 5000 Smart Transceiver Memory Map

Programming memory devices. Because the FT 5000 Smart Transceiver does not have any on-chip user-accessible NVM, only the external serial EEPROM or flash devices need to be programmed with the application and configuration data. The memory devices can be programmed in any of the following ways:

- In-circuit programming on the board.
- Over the network.
- Pre-programming before soldering on the board.

Noise Immunity

A LonWorks device based on the FT 5000 Smart Transceiver is composed of two components: the FT 5000 Smart Transceiver and an external communications transformer (the FT-X3). The transformer enables operation in the presence of high frequency common-mode noise on unshielded twisted-pair networks. Properly designed devices can meet the rigorous Level 3 requirements of EN 61000-4-6 without the need for a network isolation choke. The transformer also offers outstanding immunity from magnetic noise, eliminating the need for protective magnetic shields in most applications.

The FT 5000 Smart Transceiver and the FT-X3 Communications Transformer are designed to be used as a pair, and therefore must be implemented together in all designs. No transformer other than the FT-X3 (or FT-X1 or FT-X2) communications transformer may be used with the FT 5000 Smart Transceiver or the smart transceiver warranty will be void.

Migration Considerations

Most device designs that use the previous-generation FT 3120/3150 Smart Transceiver can transition to the FT 5000 Smart Transceiver. However, because the two generations have different supply voltage and memory architecture, hardware redesign of the boards is required to transition to the FT 5000 Smart Transceiver.

See the *Series 5000 Chip Data Book* for more information about migrating device designs for FT 3120/3150 Smart Transceivers to the FT 5000 Smart Transceiver.

End-to-End Solutions

A typical FT 5000 Smart Transceiver-based device requires a power source, crystal, external memory, and an I/O interface to the device being controlled (see Figure 7 for a typical FT 5000 Smart Transceiver-based device).

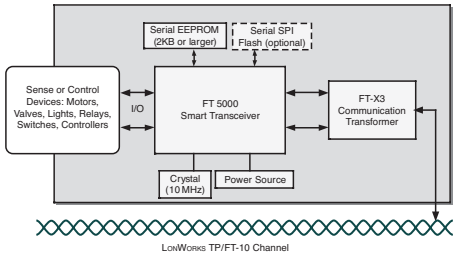


Figure 7: Typical LonWorks based Device

Echelon provides all of the building blocks required to successfully design and field cost-effective, robust products based on the FT 5000 Smart Transceivers. Our end-to-end solutions include a comprehensive set of development tools, network interfaces, routers, and network tools. In addition, pre-production design review services, training, and worldwide technical support (including onsite support) are available through Echelon's Support technical assistance program.

FT 5000 Smart Transceiver IC Pin Configuration

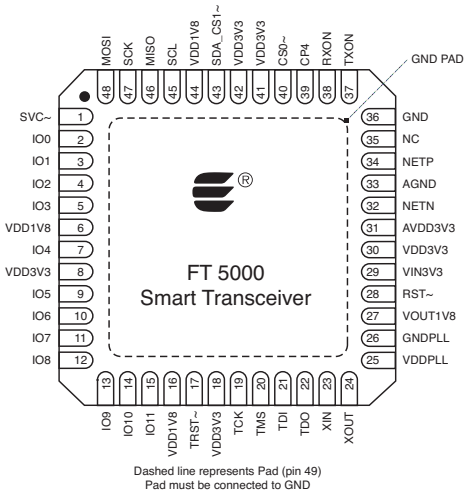


Figure 8: FT 5000 Smart Transceiver Pinout

FT 5000 Smart Transceiver IC Pin Descriptions

All digital inputs are low-voltage transistor-transistor logic (LVTTL) compatible, low leakage, 5V-tolerant. All digital outputs are slew-rate limited to reduce Electromagnetic Interference (EMI).

Pin Name	Pin Number	Type	Description
SVC~	1	Digital I/O	Service (active low)
IO0	2	Digital I/O	IO0 for I/O Objects
IO1	3	Digital I/O	IO1 for I/O Objects
IO2	4	Digital I/O	IO2 for I/O Objects
IO3	5	Digital I/O	IO3 for I/O Objects
VDD1V8	6	Power	1.8 V Power Input (from internal voltage regulator)
IO4	7	Digital I/O	IO4 for I/O Objects
VDD3V3	8	Power	3.3 V Power
IO5	9	Digital I/O	IO5 for I/O Objects
IO6	10	Digital I/O	IO6 for I/O Objects
IO7	11	Digital I/O	IO7 for I/O Objects
IO8	12	Digital I/O	IO8 for I/O Objects
IO9	13	Digital I/O	IO9 for I/O Objects
IO10	14	Digital I/O	IO10 for I/O Objects
IO11	15	Digital I/O	IO11 for I/O Objects
VDD1V8	16	Power	1.8 V Power Input (from internal voltage regulator)
TRST~	17	Digital Input	JTAG Test Reset (active low)
VDD3V3	18	Power	3.3 V Power
TCK	19	Digital Input	JTAG Test Clock

Pin Name	Pin Number	Type	Description
TMS	20	Digital Input	JTAG Test Mode Select
TDI	21	Digital Input	JTAG Test Data In
TDO	22	Digital Output	JTAG Test Data Out
XIN	23	Oscillator In	Crystal oscillator Input
XOUT	24	Oscillator Out	Crystal oscillator Output
VDDPLL	25	Power	1.8 V Power Input (from internal voltage regulator)
GNDPLL	26	Power	Ground
VOUT1V8	27	Power	1.8 V Power Output (of internal voltage regulator)
RST~	28	Digital I/O	Reset (active low)
VIN3V3	29	Power	3.3 V input to internal voltage regulator
VDD3V3	30	Power	3.3 V Power
AVDD3V3	31	Power	3.3 V Power
NETN	32	Communi-cations	Network Port (polarity insensitive)
AGND	33	Ground	Ground
NETP	34	Communi-cations	Network Port (polarity insensitive)
NC	35	N/A	Do Not Connect
GND	36	Ground	Ground
TXON	37	Digital I/O	TxActive for optional network activity LED
RXON	38	Digital I/O	RxActive for optional network activity LED
CP4	39	N/A	Connect to V_{DD33} through a 4.99 kΩ pullup resistor
CS0~	40	Digital I/O	SPI slave select 0 (CS0~, active low) (for external memory connection only)
VDD3V3	41	Power	3.3 V Power
VDD3V3	42	Power	3.3 V Power
SDA_CS1~	43	Digital I/O	I²C: serial data (SDA) SPI: slave select 1 (CS1~, active low) (for external memory connection only)
VDD1V8	44	Power	1.8 V Power Input (from internal voltage regulator)
SCL	45	Digital I/O	I²C: serial clock (SCL) (for external memory connection only)
MISO	46	Digital I/O	SPI master input, slave output (MISO) (for external memory connection only)
SCK	47	Digital I/O	SPI serial clock (SCK) (for external memory connection only)
MOSI	48	Digital I/O	SPI master output, slave input (MOSI) (for external memory connection only)
PAD	49	Ground Pad	Ground

Table 2: FT 5000 Smart Transceiver Pin Description

Electrical Characteristics
FT 5000 Smart Transceiver Operating Conditions

Parameter[1]	Description	Minimum	Typical	Maximum
V_{DD3}	Supply voltage	3.00 V	3.3 V	3.60 V
V_{LVI}	Low-voltage indicator trip point	2.70 V		2.96 V
T_A	Ambient temperature	-40° C		+85° C
f_{XIN}	XIN clock frequency[2]	-	10,0000 MHz	-
I_{DD3-RX}	Current consumption in receive mode[3] 5MHz 10MHz 20MHz 40MHz 80MHz		 9 mA 9 mA 15 mA 23 mA 38 mA	 15 mA 15 mA 23 mA 33 mA 52 mA
I_{DD3-TX}	Current consumption in transmit mode[3,4]		I_{DD3-RX} + 15 mA	I_{DD3-RX} + 18mA

Table 3: FT 5000 Smart Transceiver Operating Conditions

Notes

1. *All parameters assume nominal supply voltage (V_{DD3} = 3.3 V ± 0.3 V) and operating temperature (T_A between -40°C and +85°C), unless otherwise noted.*
2. *See* Clock Requirements *in the* Series 5000 Chip Data Book *for more detailed information about the XIN clock frequency.*
3. *Assumes no load on digital I/O pins, and that the I/O lines are not switching.*
4. *Current consumption in Transmit mode represents a peak value rather than a continuous usage value because a Series 5000 device does not typically transmit data continuously.*

Digital Pin Characteristics

The digital I/O pins (IO0–IO11) have LVTTL-level inputs. Pins IO0–IO7 also have low-level-detect latches. The RST~ and SVC~ pins have internal pull-ups, and the RST~ pin has hysteresis.

Table 4 below lists the characteristics of the digital I/O pins, which include IO0–IO11 and the other digital pins listed in Table 2.

Parameter[1]	Description	Minimum	Typical	Maximum
V_{OH}	Output drive high at I_{OH} = 8 mA	2.4 V		V_{DD3}
V_{OL}	Output drive low at I_{OL} = 8 mA	GND		0.4 V
V_{IH}	Input high level	2.0 V		5.5 V
V_{IL}	Input low level	GND		0.8 V
V_{HYS}	Input hysteresis for **RST~** pin		300 mV	
I_{IN}	Input leakage current	-		10 µA
R_{PU}	Pullup resistance[2]	13 kΩ		23 kΩ
I_{PU}	Pullup current when pin at 0 V[2]	130 µA		275 µA

Table 4: FT 5000 Smart Transceiver Digital Pin Characteristics

Notes

1. *All parameters assume nominal supply voltage (V_{DD3} = 3.3 V ± 0.3 V) and operating temperature (T_A between -40°C and +85°C), unless otherwise noted.*
2. *Applies to RST~ and SVC~ pins only.*

Recommended FT 5000 Smart Transceiver Pad Layout

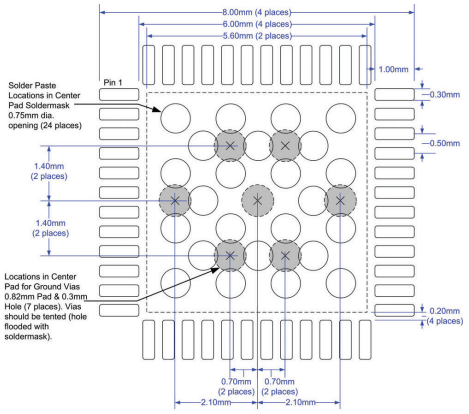
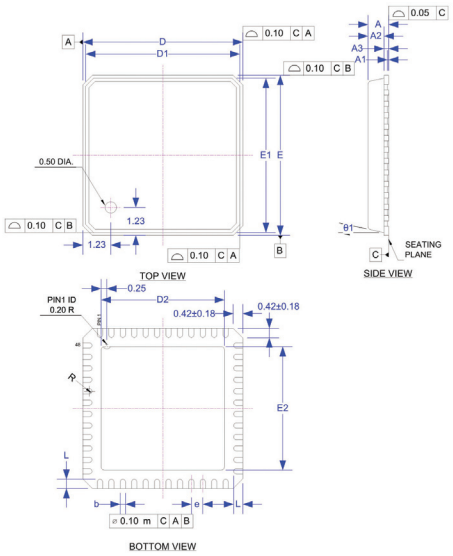


Figure 9: FT 5000 Smart Transceiver Pad Layout

FT 5000 Smart Transceiver IC Mechanical Specification



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 bsc			0.276 bsc		
D1	6.75 bsc			0.266 bsc		
D2	5.20	5.40	5.60	0.205	0.213	0.220
E	7.00 bsc			0.276 bsc		
E1	6.75 bsc			0.266 bsc		
E2	5.20	5.40	5.60	0.205	0.213	0.220
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

Figure 10: FT 5000 Smart Transceiver IC Mechanical Specifications

Notes

1. *All dimensions are in millimeters.*
2. *Dimensions and tolerances conform to ASME Y14.5M.-1994.*
3. *Package warpage max. 0.08 mm.*
4. *Package corners unless otherwise specified are R0.175±0.025 mm.*

FT-X3 Communications Transformer Pin Descriptions

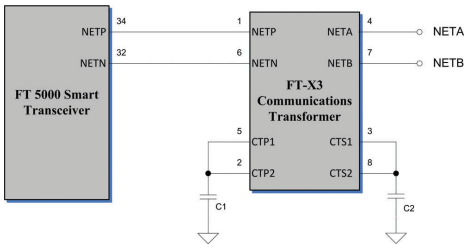


Figure 11: FT-X3 Communications Transformer Pinout Diagram

Pin Name	Pin Number	Description
NETP	1	NETP connection from FT 5000 Smart Transceiver
CTP1	2	Center tap primary 1
CTS2	3	Center tap secondary 2
NETA	4	NETA connection to LonWorks network
CTP2	5	Center tap primary 2
NETN	6	NETN connection from FT 5000 Smart Transceiver
NETB	7	NETB connection to LonWorks network
CTS1	8	Center tap secondary 1

Table 5: FT-X3 Communications Transformer Pin Assignments

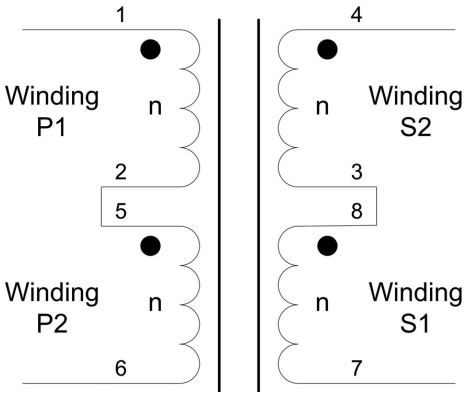


Figure 12: FT-X3 Communications Transformer Electrical Connection Schematic (winding connections are made on the PCB)

Recommended FT-X3 Communications Transformer Pad Layout

The FT-X3 Communications Transformer is rotationally symmetric. Hence, the transformer package does not have a marking for Pin 1.

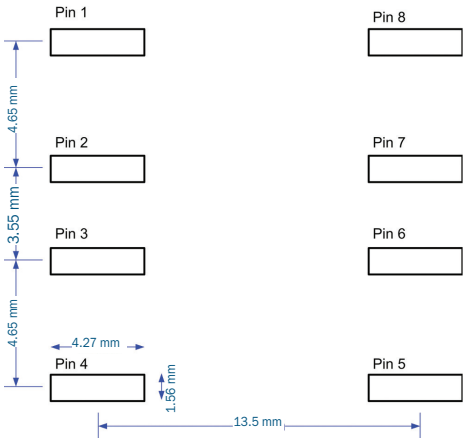
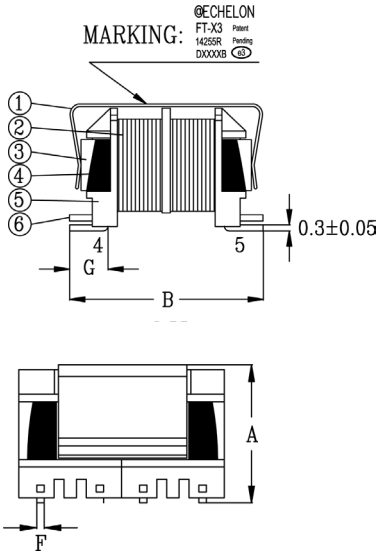
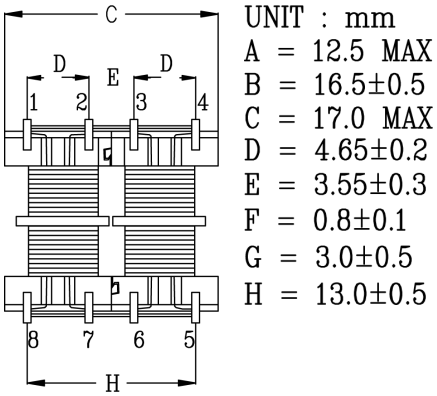


Figure 13: FT-X3 Transformer SMT Layout Pad Pattern

Recommendation: Add vias to the ends of each pin pad connection (just outside of the SMT pad rectangles) to provide additional mechanical support for the transformer.

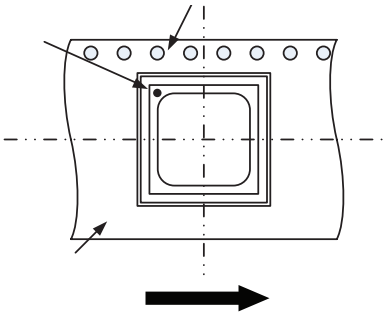
FT-X3 Communications Transformer Mechanical Specification





FT 5000 Tape and Reel Information

Devices are uniformly loaded in the carrier tape such that the device pin one is oriented in quadrant 1 toward the side of the tape having round sprocket holes. Figure 15 illustrates the pin-one location.



User Direction of Feed

Figure 15: FT 5000 Pin One Orientation

Figure 16 shows the outline dimensions of the carrier tape.

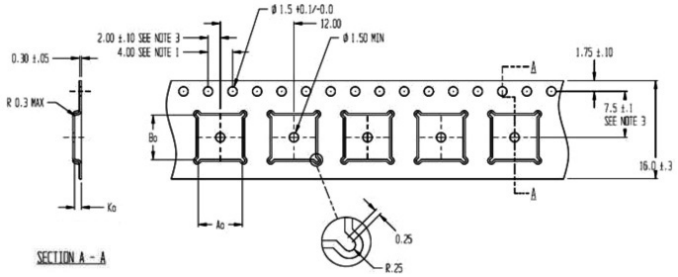


Figure 16: Carrier Tape Outline Drawing

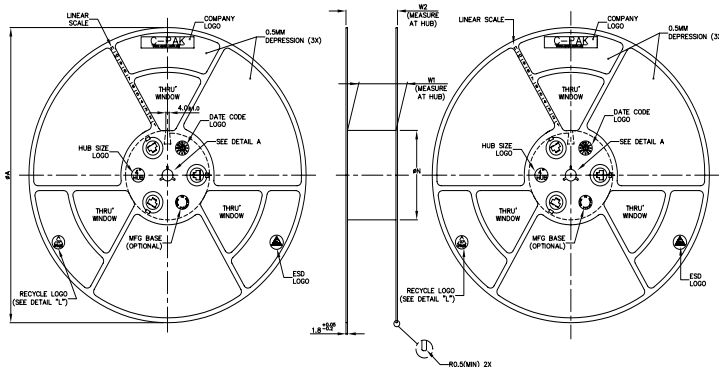
Ao = Bo = 7.25
Ko = 1.10

Notes

1. *All dimensions are in millimeters.*
2. *Tolerances unless noted: 1PL + 0.2. 2PL + 0.1*
3. *10 Sprocket hole pitch cumulative tolerance +0.2*
4. *Camber in compliance with EIA 481.*
5. *Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.*

For more information, refer to EIA-481-B, *Taping of Surface Mount Components for Automatic Placement*.

Figure 17 shows the FT 5000 Series 13" Reel Drawing and Specification.

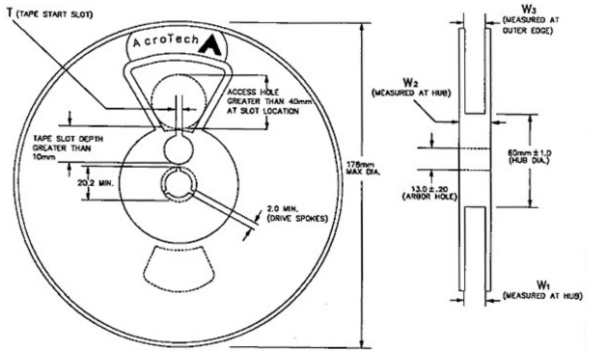


PRODUCT SPECIFICATIONS				
TAPE WIDTH	øA (MAX)	øN (MIN)	W1 +2.0 -0.0	W2 (MAX)
©8MM	330	100	8.4	14.4
12MM	330	100	12.4	18.4
16MM	330	100	16.4	22.4
24MM	330	100	24.4	30.4
32MM	330	100	32.4	38.4
44MM	330	100	44.4	50.4
56MM	330	100	56.4	62.4

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^6 TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^5 AND BELOW 10^5	CONDUCTIVE (GENERIC)	BLACK ONLY
C	10^5 TO 10^9	CONDUCTIVE (CUSTOM)	BLACK ONLY

Figure 17: FT 5000 13" Reel and Hub Drawing

Figure 18 shows the 5000 Series 7" Reel Drawing and Specification.



TAPE SIZE	T	W_1	W_2	W_3
8mm	4.0 ±0.25	+1.5 8.4-0.0	14.4 MAX.	7.9 MIN. 10.9 MAX.
12mm	5.0 ±0.50	+2.0 12.4-0.0	18.4 MAX.	11.9 MIN. 15.4 MAX.
16mm	7.0 ±0.50	+2.0 16.4-0.0	22.4 MAX.	15.9 MIN. 19.4 MAX.
24mm	11.0 ±0.50	+2.0 24.4-0.0	30.4 MAX.	23.9 MIN. 27.4 MAX.
32mm	11.0 ±0.50	+2.0 32.4-0.0	38.4 MAX.	31.9 MIN. 35.4 MAX.
44mm	11.0 ±0.50	+2.0 44.4-0.0	50.4 MAX.	43.9 MIN. 47.4 MAX.

Figure 18: FT 5000 7" Reel and Hub Drawing

FT-X3 Packing Specifications

Figure 19 shows the placement of each device on the carrier tape.

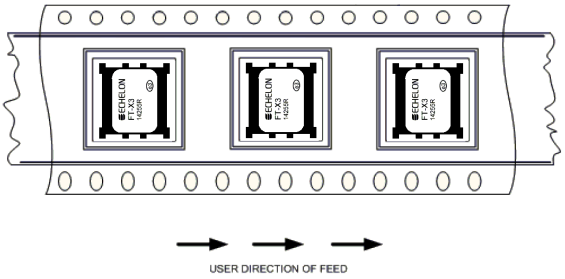
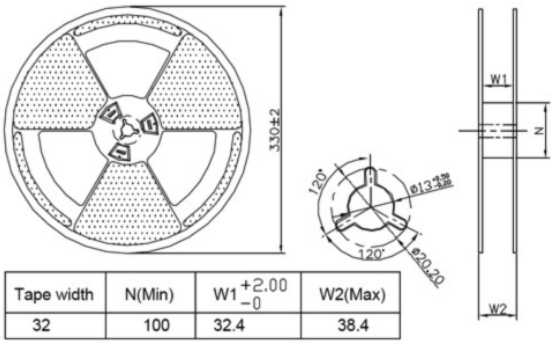


Figure 19: FT-X3 Device Placement on the Carrier Tape

Figure 20 shows the 1.3" Reels/4" Hub.



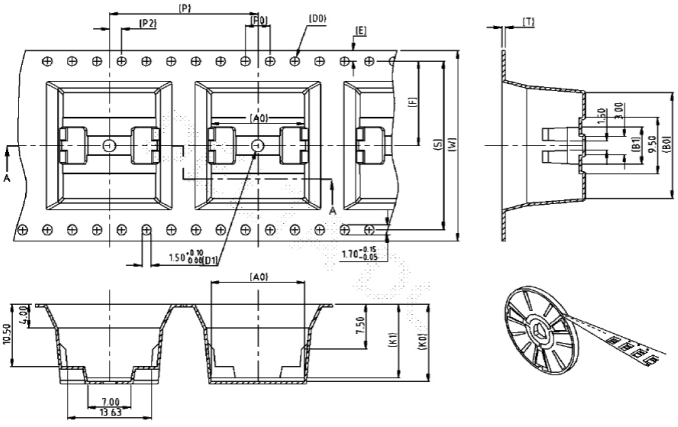
Tape width	N(Min)	W1 $^{+2.00}_{-0}$	W2(Max)
32	100	32.4	38.4

Figure 20: FT-X3 Reel and Hub Drawing

Notes

1. *All dimensions are in millimeters.*
2. *Tolerances unless noted: 1PL + ; 2PL + 0.2; 3PL + 0.1; ANG + 0.5"; FRACT +*

Figure 21 shows the FT-X3 Packing Specification



W	32.00±0.30	P	24.00±0.10	AO	15.10±0.10	BO	17.80±0.15
S	28.40±0.10	PO	4.00±0.10			B1	6.30±0.10
E	1.75±0.10	P2	2.00±0.10				
F	14.20±0.10	DO	Ø1.50 $^{+0.10}_{0}$	KO	13.00±0.10		
T	0.50±0.04	D1	Ø2.00 MIN	K1	12.40±0.10	COLOR : BK/ANT	

Figure 21: FT-X3 Packing Drawing

Notes

1. *Material: Black conductive polystyrene PS*
2. *Inspect per EIA-481-3 standard.*
3. *Tape thickness: 0.5 ±0.05 mm*
4. *10 Sprocket hole pitch cumulative tolerance ±0.20*
5. *Carrier chamber is within 1 mm in 100 mm*
6. *Packing length per 22" reel: 10.2 meters*
7. *Packing length per 13" reel: 3.4 meters*
8. *Component load per 13" reel: 100 PCS*
9. *Compression strength: 1.5 kgf min.*
10. *Environment-Related substance must meet DELTA's general spec no. 10000-0162*

SPECIFICATIONS

Data Communications Type
Differential Manchester encoding.

Network Polarity
Polarity insensitive.

Isolation between Network and FT 5000 IC
0-60Hz, 60 seconds: 1,000Vrms; 0-60Hz, continuous: 277Vrms[1].

EMI
Designed to comply with FCC Part 15 Subpart B and EN55022 Level B.

ESD
Designed to comply with EN 61000-4-2, Level 4.

Radiated Electromagnetic Susceptibility
Designed to comply with EN 61000-4-3, Level 3.

Fast Transient/Burst Immunity
Designed to comply with EN 61000-4-4, Level 4.

Surge Immunity
Designed to comply with EN 61000-4-5, Level 3.

Conducted RF Immunity
Designed to comply with EN 61000-4-6, Level 3.

Transmission Speed
78 kilobits per second.

Number of Transceivers per Segment
Up to 64.

Network Wiring
24 to 16AWG twisted pair; see *Series 5000 Chip Data Book* or *Junction Box and Wiring Guidelines* engineering bulletin for qualified cable types.

Network Length in Free Topology[2]
500m (1,640 feet) maximum total wire with no repeaters.
500m (1,640 feet) maximum device-to-device distance.

Network Length in Doubly-terminated Bus Topology[2]
2700m (8,850 feet) with no repeaters.

Maximum Stub Length in Doubly-terminated Bus Topology
3m (9.8 feet).