

## EiceDRIVER™ 1ED31xxMC12H Compact

### Datasheet

Single-channel 5.7 kV (rms) isolated gate driver IC with active Miller clamp or separate output

### Feature list

- Single channel isolated gate driver
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to 14.0 A typical peak output current
- 40 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 200 kV/μs
- Separate source and sink outputs or active Miller clamp with active shutdown and short circuit clamping
- Galvanically isolated coreless transformer gate driver
- 3.3 V and 5 V input supply voltage
- Suitable for operation at high ambient temperature and in fast switching applications
- Certification: VDE 0884-11 with  $V_{IORM} = 1767$  V (peak) (Certificate no. 40052310) and UL 1577 with  $V_{ISO} = 5.7$  kV (rms) for 1 min (File E311313)

### Potential applications

- AC and brushless DC motor drives
- High voltage DC-DC converter and DC-AC inverter
- Induction heating resonant application
- UPS-systems
- Commercial air-conditioning (CAC)
- Server and telecom switched mode power supplies (SMPS)
- Solar inverters, e.g. for 1500 V (DC) systems



PG-DSO-8

### Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

**Device information**

**Device information**

Product type	Typical output current and configuration	UVLO ( $V_{UVLO,L2,min}$ )	Certification	Package marking
1ED3120MC12H	5.5 A separate source and sink	8.0 V	VDE + UL	3120MC12
1ED3121MC12H	5.5 A separate source and sink	10.5 V	VDE + UL	3121MC12
1ED3122MC12H	10.0 A and 3.0 A clamp	8.0 V	VDE + UL	3122MC12
1ED3123MC12H	14.0 A separate source and sink	8.0 V	VDE + UL	3123MC12
1ED3124MC12H	14.0 A separate source and sink	10.5 V	VDE + UL	3124MC12
1ED3131MC12H	5.5 A separate source and sink, 180 ns minimum input pulse suppression time	10.5 V	VDE + UL	3131MC12

**Description**

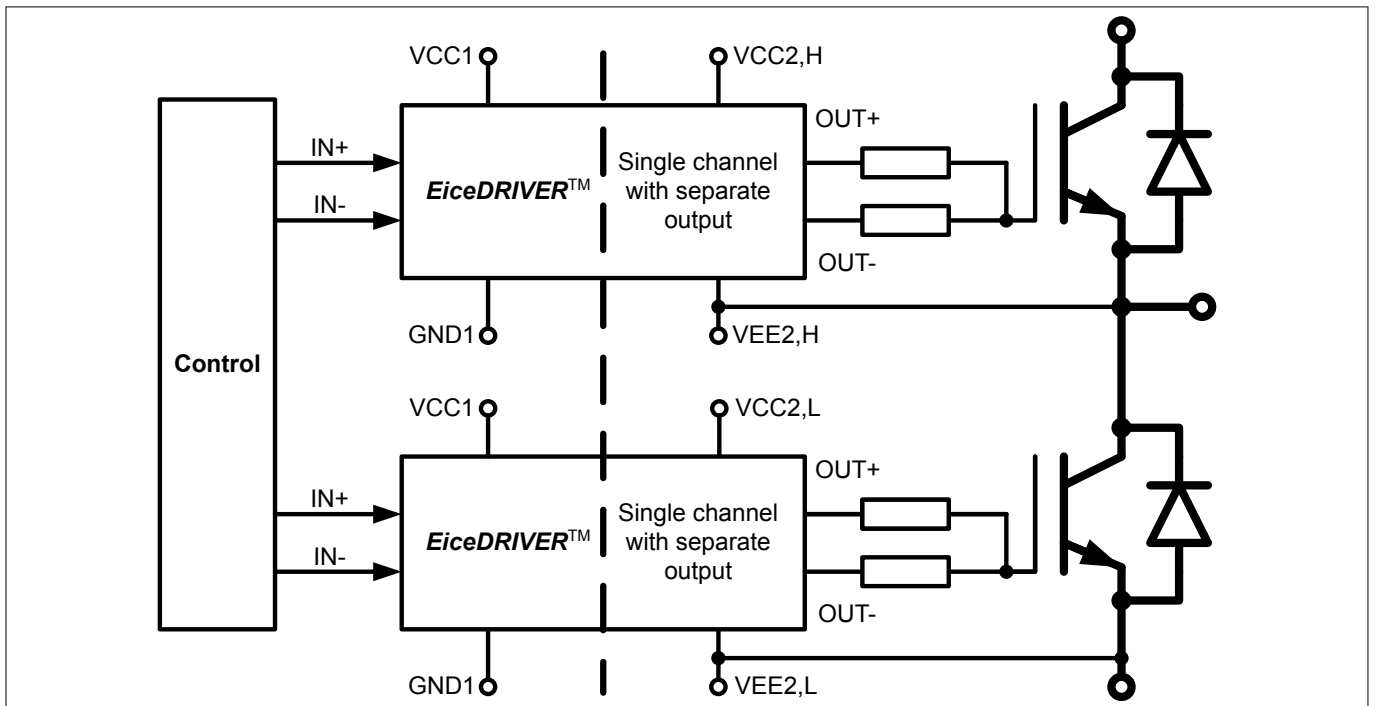
The 1ED31xxMC12H (1ED-X3 Compact) gate driver ICs are galvanically isolated single channel gate driver ICs for IGBT, MOSFET and SiC MOSFET in PG-DSO-8 package. They provide a typical output current of up to 14.0 A on separate source and sink pins or a typical output current of 10.0 A with an additional 3.0 A active Miller clamp.

The input logic pins operate on a wide input voltage range from 3 V to 15 V using CMOS threshold levels to support 3.3 V microcontrollers.

Data transfer across the isolation barrier is realized by the coreless transformer technology.

All variants have logic input and driver output undervoltage lockout (UVLO), and active shutdown.

The gate drivers are certified according to VDE 0884-11 and UL 1577



**Figure 1 Typical application using separate output variant**

## Table of contents

	<b>Table of contents</b> .....	3
<b>1</b>	<b>Block diagram reference</b> .....	4
<b>2</b>	<b>Related products</b> .....	5
<b>3</b>	<b>Pin configuration and description</b> .....	6
<b>4</b>	<b>Functional description</b> .....	8
4.1	Supply .....	8
4.2	Protection features .....	9
4.2.1	Undervoltage lockout (UVLO) .....	9
4.2.2	Active shut-down .....	9
4.2.3	Short circuit clamping .....	9
4.2.4	Active Miller clamp .....	9
4.3	Non-inverting and inverting inputs .....	10
4.4	Driver outputs .....	10
<b>5</b>	<b>Electrical characteristics and parameters</b> .....	11
5.1	Absolute maximum ratings .....	11
5.2	Operating parameters .....	12
5.3	Electrical characteristics .....	13
5.3.1	Power supply .....	13
5.3.2	Logic input .....	13
5.3.3	Gate driver .....	14
5.3.4	Dynamic characteristics .....	15
5.3.5	Active shut down .....	16
<b>6</b>	<b>Insulation characteristics</b> .....	17
6.1	Certified according to VDE 0884-11 reinforced insulation (Certificate no. 40052310) .....	17
6.2	Recognized under UL 1577 (File E311313) .....	18
<b>7</b>	<b>Package dimensions</b> .....	19
	<b>Revision history</b> .....	19
	<b>Disclaimer</b> .....	20

1 Block diagram reference

1 Block diagram reference

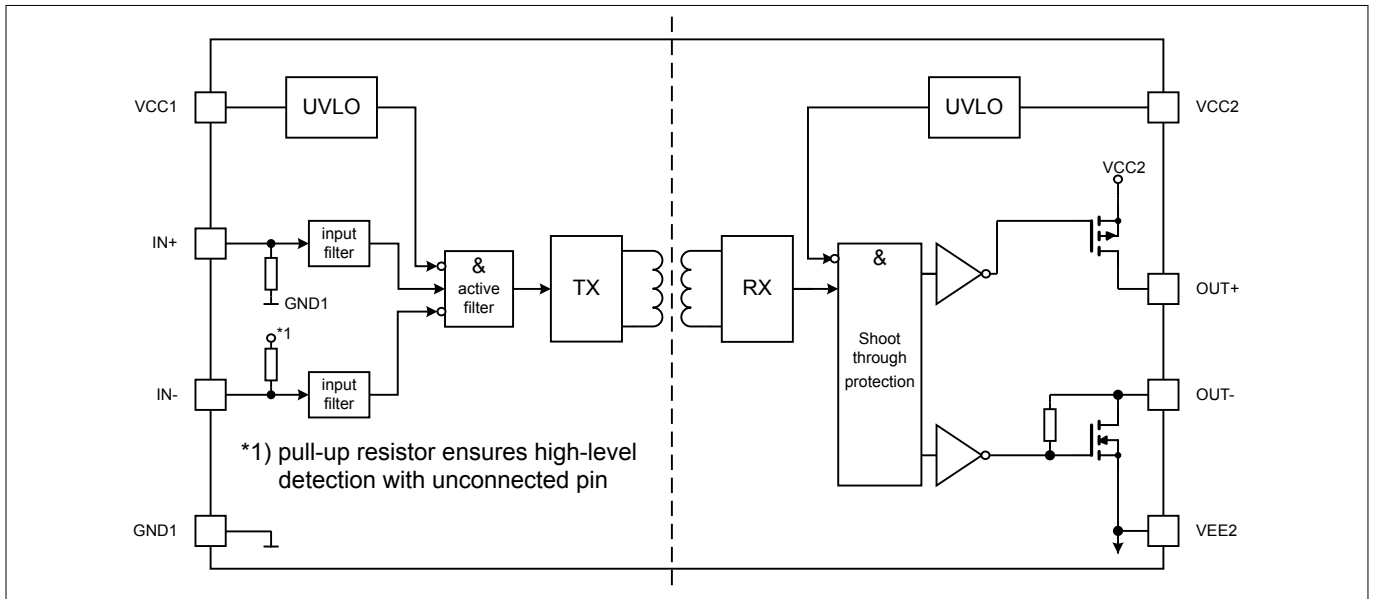


Figure 2 Block diagram separate source and sink output variants

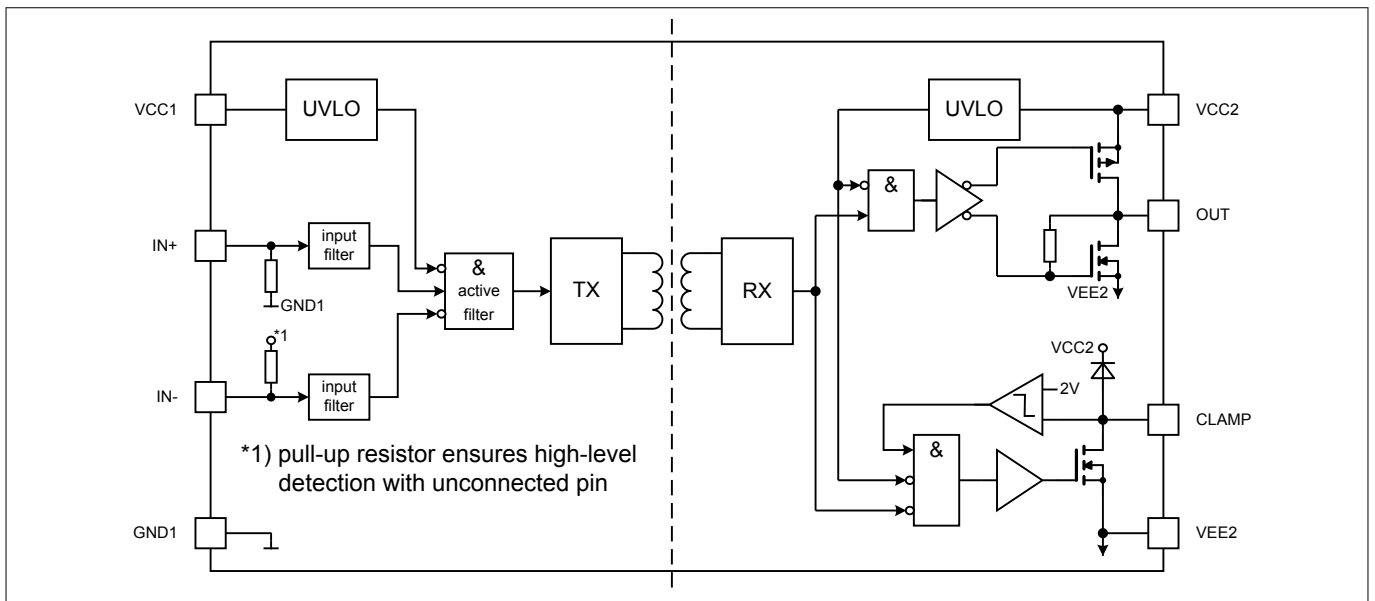


Figure 3 Block diagram output with CLAMP variants

**2 Related products**

**2 Related products**

*Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.*

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	<a href="#">IKQ75N120CS6</a>	High Speed 1200 V, 75 A IGBT with anti-parallel diode in TO247-3
	<a href="#">IKW15N120BH6</a>	High Speed 1200 V, 15 A IGBT with anti-parallel diode in TO247
	<a href="#">IHW40N120R5</a>	Reverse conducting 1200 V, 40 A IH IGBT with integrated diode in TO247
CoolSiC™ SiC MOSFET Discrete	<a href="#">IMBF170R650M1</a>	1700 V, 650 mΩ SiC MOSFET in TO263-7 package
	<a href="#">IMBG120R045M1H</a>	1200 V, 45 mΩ SiC MOSFET in TO263-7 package
	<a href="#">IMZ120R350M1H</a>	1200 V, 350 mΩ SiC MOSFET in TO247-4 package
CoolSiC™ SiC MOSFET Module	<a href="#">FS45MR12W1M1_B11</a>	EasyPACK™ 1B 1200 V / 45 mΩ sixpack module
	<a href="#">FF23MR12W1M1_B11</a>	EasyDUAL™ 1B 1200 V, 23 mΩ half-bridge module
	<a href="#">FF6MR12W2M1_B11</a>	EasyDUAL™ 2B 1200 V, 6 mΩ half-bridge module
	<a href="#">F3L11MR12W2M1_B74</a>	EasyPACK™ 2B 1200 V, 11 mΩ 3-Level module in Advanced NPC (ANPC) topology
	<a href="#">F4-23MR12W1M1_B11</a>	EasyPACK™ 1B 1200 V, 23 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	<a href="#">F4-100R17N3E4</a>	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	<a href="#">F4-200R17N3E4</a>	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	<a href="#">FS150R17N3E4</a>	EconoPACK™ 3 1700 V, 150 A sixpack IGBT module
	<a href="#">FF650R17IE4</a>	PrimePACK™ 3 1700 V, 650 A half-bridge dual IGBT module
	<a href="#">FF1000R17IE4</a>	PrimePACK™ 3 1700 V, 1000 A half-bridge dual IGBT module
	<a href="#">FF1200R17IP5</a>	PrimePACK™ 3+ 1700 V, 1200 A dual IGBT module
	<a href="#">FF1500R17IP5</a>	PrimePACK™ 3+ 1700 V, 1500 A dual IGBT module
	<a href="#">FF1500R17IP5R</a>	PrimePACK™ 3 1700 V, 1500 A dual IGBT module
	<a href="#">FF1800R17IP5</a>	PrimePACK™ 3+ 1700 V, 1800 A dual IGBT module
	<a href="#">FP10R12W1T7_B11</a>	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	<a href="#">FS100R12W2T7_B11</a>	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	<a href="#">FP150R12KT4_B11</a>	EconoPIM™ 3 1200V three-phase PIM IGBT module
	<a href="#">FS200R12KT4R_B11</a>	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

**Table 1 Evaluation boards**

Part number	Description
<a href="#">EVAL-1ED3121MX12H</a>	Half-bridge evaluation board for 1ED3121MU12H
<a href="#">EVAL-1ED3122MX12H</a>	Half-bridge evaluation board for 1ED3122MU12H
<a href="#">EVAL-1ED3124MX12H</a>	Half-bridge evaluation board for 1ED3124MU12H

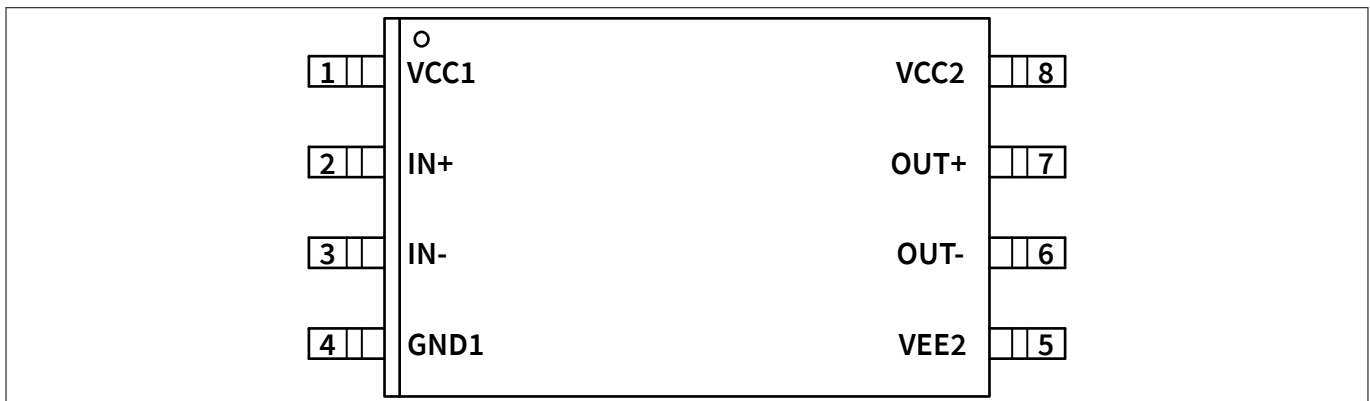
**3 Pin configuration and description**

**3 Pin configuration and description**

**Pin configuration PG-DSO-8 of 1ED3121MC12H, 1ED3124MC12H, 1ED3120MC12H, 1ED3123MC12H and 1ED3131MC12H**

**Table 2 Pin configuration**

Pin No.	Name	Function
1	VCC1	Positive logic supply
2	IN+	Non-inverted driver input (active high)
3	IN-	Inverted driver input (active low)
4	GND1	Logic ground
5	VEE2	Power ground
6	OUT-	Driver sink output
7	OUT+	Driver source output
8	VCC2	Positive power supply output side



**Figure 4 PG-DSO-8 (top view)**

**Pin configuration PG-DSO-8 of 1ED3122MC12H**

**Table 3 Pin configuration**

Pin No.	Name	Function
1	VCC1	Positive logic supply
2	IN+	Non-inverted driver input (active high)
3	IN-	Inverted driver input (active low)
4	GND1	Logic ground
5	VEE2	Power ground
6	CLAMP	Active Miller clamp output
7	OUT	Driver source and sink output
8	VCC2	Positive power supply output side

3 Pin configuration and description



Figure 5 PG-DSO-8 (top view)

Pin description

- *VCC1*: Logic input supply voltage of 3.3 V up to 15 V wide operating range
- *GND1*: Ground connection of input circuit.
- *IN+*: Non-inverted control signal for driver output. An internal filter provides robustness against noise at *IN+*. An internal weak pull-down resistor favors off-state.
- *IN-*: Inverted control signal for driver output. An internal filter provides robustness against noise at *IN-*. An internal weak pull-up resistor favors off-state.
- *VCC2*: Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin.
- *VEE2*: Reference ground of the output driving circuit. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter) this pin is connected to the negative supply voltage.
- *OUT+*: Driver source output pin to turn on external IGBT. During on-state the driving output is switched to *VCC2*. Switching of this output is controlled by *IN+* and *IN-*. This output will also be turned off at an UVLO event.
- *OUT-*: Driver sink output pin to turn off external IGBT. During off-state the driving output is switched to *VEE2*. Switching of this output is controlled by *IN+* and *IN-*. In case of UVLO an active shut down keeps the output voltage at a low level.
- *OUT*: Combined source and sink output pin to external IGBT. The output voltage will be switched between *VCC2* and *VEE2*. Switching of this output is controlled by *IN+* and *IN-*. In case of an UVLO event this output will be switched off and an active shut down keeps the output voltage at a low level.
- *CLAMP*: The clamp function ties its output to *VEE2* during off-state. It activates as soon as the gate voltage has dropped below 2.0 V referred to *VEE2* after a turn-off command. Connect this pin directly to the IGBT gate to avoid parasitic turn-on of the connected IGBT.

**4 Functional description**

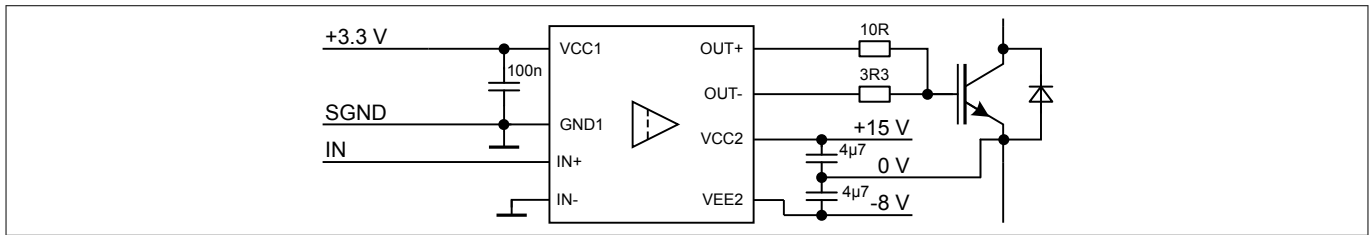
**4 Functional description**

The 1ED31xxMC12H (1ED-X3 Compact) are general purpose IGBT gate drivers. Basic control and protection features support fast and easy design of highly reliable systems.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its input voltage supply range supports the direct connection of various signal sources like DSPs and microcontrollers.

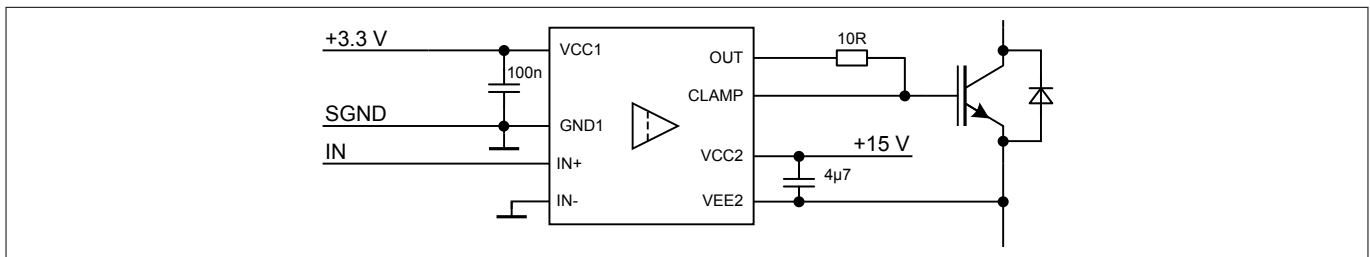
**4.1 Supply**

The driver can operate over a wide supply voltage range, either unipolar or bipolar.



**Figure 6 Application example bipolar supply**

With bipolar supply the driver is typically operated with a positive voltage of 15 V at VCC2 and a negative voltage of -8 V at VEE2 relative to the emitter of the IGBT. Negative supply can help to prevent a dynamic turn on due to the additional charge which is generated from IGBT's input capacitance.



**Figure 7 Application example unipolar supply**

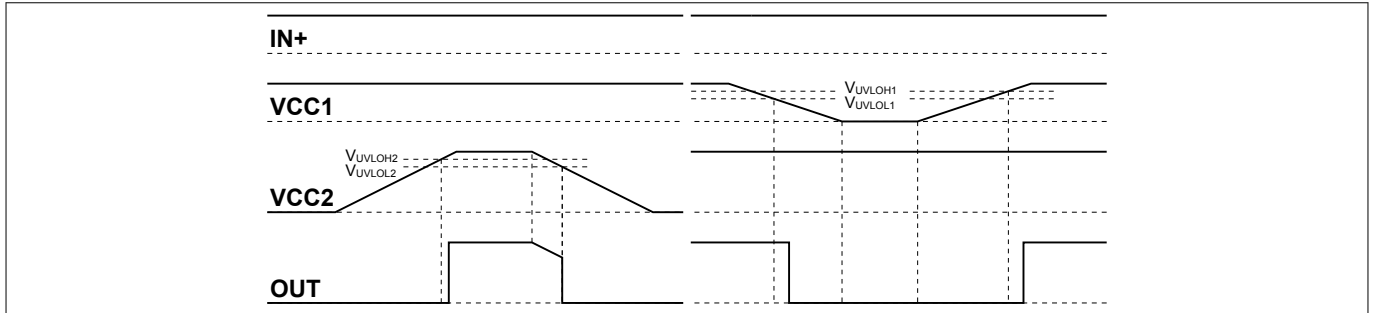
For unipolar supply configuration the driver is typically supplied with a positive voltage of 15 V at VCC2. In this case, careful evaluation for turn off gate resistor selection is recommended to avoid dynamic turn on. Both supply options are usable with either output configuration separate source and sink as well as output with active Miller clamp.



**4 Functional description**

**4.2 Protection features**

**4.2.1 Undervoltage lockout (UVLO)**



**Figure 8 UVLO behavior**

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for input and output independently. Operation starts only after both VCC levels have increased beyond the respective  $V_{UVLOH}$  levels.

If the power supply voltage  $V_{VCC1}$  of the input chip drops below  $V_{UVLOL1}$  a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at  $IN+$  and  $IN-$  are ignored until  $V_{VCC1}$  reaches the power-up voltage  $V_{UVLOH1}$  again.

If the power supply voltage  $V_{VCC2}$  of the output chip goes down below  $V_{UVLOL2}$  the IGBT is switched off and signals from the input chip are ignored until  $V_{VCC2}$  reaches the power-up voltage  $V_{UVLOH2}$  again.

*Note:*  $V_{VCC2}$  is always referred to  $VEE2$  and does not differentiate between unipolar or bipolar supply.

**4.2.2 Active shut-down**

The active shut-down feature ensures a safe IGBT off-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT gate is clamped at  $OUT-$  or  $CLAMP$  to  $VEE2$ .

**4.2.3 Short circuit clamping**

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An internal protection circuit at  $OUT+$  or  $CLAMP$  limits this voltage to a value slightly higher than the supply voltage. A maximum current of 500 mA may be fed back to the supply through this path for 10  $\mu$ s. If higher currents are expected or tighter clamping is desired external Schottky diodes may be added.

**4.2.4 Active Miller clamp**

In a half bridge configuration the switched off IGBT tends to dynamically turn on during turn on phase of the opposite IGBT. A Miller clamp allows sinking the Miller current across a low impedance path in this high  $dV/dt$  situation. Therefore in many applications, the use of a negative supply voltage can be avoided. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage drops below typical 2 V (referred to  $VEE2$ ). The clamp is designed for a Miller current in the same range as the nominal output current.

4 Functional description

4.3 Non-inverting and inverting inputs

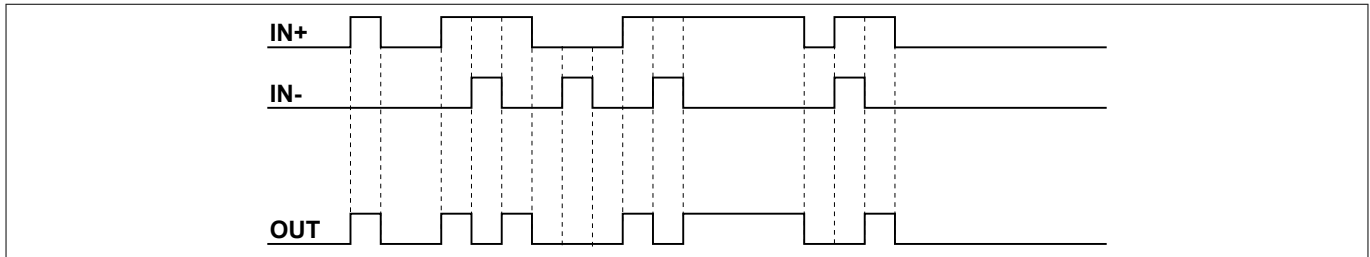


Figure 9 Logic input to output switching behavior

There are two possible input modes to control the IGBT. At non-inverting mode *IN+* controls the driver output while *IN-* is set to low. At inverting mode *IN-* controls the driver output while *IN+* is set to high. A minimum input pulse width is defined to filter occasional glitches.

4.4 Driver outputs

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the driver's supply is stable. Due to the low internal voltage drop, switching behavior of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

**5 Electrical characteristics and parameters**

**5 Electrical characteristics and parameters**

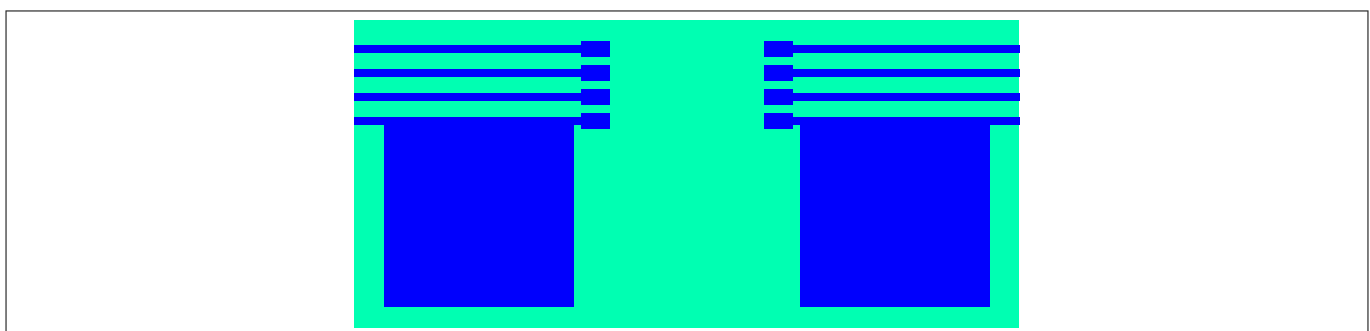
**5.1 Absolute maximum ratings**

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to *GND1*.

**Table 4 Absolute maximum ratings**

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Input to output offset voltage	$V_{\text{OFFSET}}$	-	2300	V	$V_{\text{VEE2,max}} - V_{\text{VEE2,min}}$ with $V_{\text{VEE2,max}} \geq V_{\text{GND1}} \geq V_{\text{VEE2,min}}$ <sup>1) 2)</sup>
Power supply output side	$V_{\text{VCC2}}$	-0.3	40	V	<sup>3)</sup>
Gate driver output ( <i>OUT+</i> , <i>OUT-</i> , <i>OUT</i> , <i>CLAMP</i> )	$V_{\text{OUT}}$	$\text{VEE2} - 0.3$	$\text{VCC2} + 0.3$	V	<sup>3)</sup>
Power supply input side	$V_{\text{VCC1}}$	-0.3	17	V	$\text{VCC1} - \text{GND1}$
Logic input voltages ( <i>IN+</i> , <i>IN-</i> )	$V_{\text{IN}}$	-0.3	6.5	V	$\text{IN} - \text{GND1}$
Junction temperature	$T_{\text{J}}$	-40	150	°C	-
Storage temperature	$T_{\text{Stg}}$	-55	150	°C	-
Power dissipation (input side)	$P_{\text{D,IN}}$	-	100	mW	$T_{\text{A}} = 65^{\circ}\text{C}$ <sup>4)</sup>
Power dissipation (output side)	$P_{\text{D,OUT}}$	-	700	mW	$T_{\text{A}} = 65^{\circ}\text{C}$ <sup>5)</sup>
Thermal resistance junction to ambient	$R_{\text{thJA,OUT}}$	-	88	K/W	$T_{\text{A}} = 85^{\circ}\text{C}$ 300 mil, 1s0p, $P_{\text{J}} = 266$ mW
Characterization parameter junction to package top input side	$\psi_{\text{Jtop}}$	-	6	K/W	
ESD robustness	$V_{\text{ESD,HBM}}$	-	4	kV	Human body model <sup>6)</sup>
	$\text{ESD,CDM}$	-	TC 1000	-	Charged device model <sup>7)</sup>

- 1) for functional operation only
- 2) See also [Chapter 6.1](#) on page 17
- 3) With respect to *VEE2*
- 4) IC input-side power dissipation is derated linearly with 11.4 mW/°C above 141 °C
- 5) IC output-side power dissipation is derated linearly with 11.4 mW/°C above 88 °C
- 6) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
- 7) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)



**Figure 10 Reference layout for thermal data (Copper thickness 35 μm)**

This PCB layout represents the reference layout used for the thermal characterization of the 300 mil package.

**5 Electrical characteristics and parameters**

**5.2 Operating parameters**

Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to *GND1*.

**Table 5 Electrical characteristics**

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Power supply output side	$V_{VCC2}$	10	35	V	1)
Power supply input side	$V_{VCC1}$	3.1	15	V	–
Logic input voltages ( $IN+$ , $IN-$ )	$V_{IN}$	-0.3	5.5	V	–
Switching frequency	$f_{SW}$	–	1	MHz	max $P_D$ applies
Ambient temperature	$T_A$	-40	125	°C	–
Common mode transient immunity (CMTI)	CMTI	-200	200	kV/ $\mu$ s	$V_{OFFSET, test} = 1500$ V

1) With respect to *VEE2*

**5 Electrical characteristics and parameters**

**5.3 Electrical characteristics**

*Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at  $T_A = 25^\circ\text{C}$ . Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 3 and VEE2 for pins 6 to 8).*

**5.3.1 Power supply**

**Table 6 Power supply**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	$V_{UVLOH1}$	–	–	3.1	V	–
UVLO threshold input side (off)	$V_{UVLOL1}$	2.5	–	–	V	–
UVLO hysteresis input side	$V_{HYS1}$	0.1	0.2	–	V	–
UVLO threshold output side (on)	$V_{UVLOH2,1}$	–	–	10.0	V	1ED3120MC12H, 1ED3122MC12H, 1ED3123MC12H
UVLO threshold output side (off)	$V_{UVLOL2,1}$	8.0	–	–	V	
UVLO threshold output side (on)	$V_{UVLOH2,2}$	–	–	12.5	V	1ED3121MC12H, 1ED3124MC12H, 1ED3131MC12H
UVLO threshold output side (off)	$V_{UVLOL2,2}$	10.5	–	–	V	
UVLO hysteresis output side	$V_{HYS2}$	0.8	–	–	V	–
Quiescent current input side	$I_{Q1}$	–	–	1.1	mA	static, output low
Quiescent current output side	$I_{Q2}$	–	–	2	mA	
Start up time	$t_{START}$	–	2.5	20	$\mu\text{s}$	1)
UVLO detection filter time	$t_{UVLOft}$	50	–	–	ns	1)

1) Parameter is not subject to production test - verified by design/characterization

**5.3.2 Logic input**

**Table 7 Logic input**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
$IN+$ , $IN-$ logic low input voltage	$V_{IN,L}$	–	–	1.1	V	–
$IN+$ , $IN-$ logic high input voltage	$V_{IN,H}$	2.5	–	–	V	–
$IN+$ , $IN-$ low/high hysteresis	$V_{IN,HYS}$	0.5	0.8	–	V	–
$IN+$ , $IN-$ input current	$I_{IN}$	–	–	100	$\mu\text{A}$	$V_{CC1} = 5\text{V}$ ; $V_{IN} \leq V_{CC1}$
$IN+$ pull down resistor	$R_{IN,PD}$	–	75	–	k $\Omega$	to GND1
$IN-$ pull up resistor	$R_{IN,PU}$	–	75	–	k $\Omega$	ensures high-level detection with unconnected pin

**5 Electrical characteristics and parameters**

**5.3.3 Gate driver**

All gate driver output parameters valid for  $V_{CC2} = 15\text{ V}$  supply voltage unless specified otherwise.

**Table 8 Gate driver**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
1ED3120MC12H, 1ED3121MC12H, 1ED3131MC12H						
High level output peak current	$I_{OUT,H}$	2.0	5.5	–	A	<sup>1)</sup> $V_{CC2-OUT+} = 15\text{ V}$ , Output on
High level output on resistance	$R_{DSON,H}$	0.60	0.95	1.45	$\Omega$	$I_{OUT,H} = 0.1\text{ A}$
Low level output peak current	$I_{OUT,L}$	2.0	5.5	–	A	<sup>1)</sup> $OUT-VEE2 = 15\text{ V}$ , Output off
Low level output on resistance	$R_{DSON,L}$	0.50	0.75	1.05	$\Omega$	$I_{OUT,L} = 0.1\text{ A}$
1ED3122MC12H						
High level output peak current	$I_{OUT,H}$	4.0	10.0	–	A	<sup>1)</sup> $V_{CC2-OUT} = 15\text{ V}$ , Output on
High level output on resistance	$R_{DSON,H}$	0.30	0.55	0.85	$\Omega$	$I_{OUT,H} = 0.1\text{ A}$
Low level output peak current	$I_{OUT,L}$	4.0	9.0	–	A	<sup>1)</sup> $OUT-VEE2 = 15\text{ V}$ , Output off
Low level output on resistance	$R_{DSON,L}$	0.30	0.45	0.65	$\Omega$	$I_{OUT,L} = 0.1\text{ A}$
Low level clamp peak current	$I_{CLAMP,L}$	2.0	3.0	–	A	<sup>1)</sup> $V_{CLAMP} = 2.0\text{ V}$
Low level clamp on resistance	$R_{DSON,CLP}$	0.33	0.55	0.76	$\Omega$	$I_{CLAMP,L} = 0.1\text{ A}$
CLAMP threshold voltage	$V_{CLAMP}$	1.6	2.0	2.4	V	CLAMP-VEE2
CLAMP comparator to CLAMP activation delay time	$t_{CLPDLY}$	–	–	80	ns	<sup>1)</sup> $V_{CLAMP} \leq 2.0\text{ V}$
1ED3123MC12H, 1ED3124MC12H						
High level output peak current	$I_{OUT,H}$	6.0	13.5	–	A	<sup>1)</sup> $V_{CC2-OUT+} = 15\text{ V}$ , Output on
High level output on resistance	$R_{DSON,H}$	0.27	0.45	0.65	$\Omega$	$I_{OUT,H} = 0.1\text{ A}$
Low level output peak current	$I_{OUT,L}$	6.0	14.0	–	A	<sup>1)</sup> $OUT-VEE2 = 15\text{ V}$ , Output off
Low level output on resistance	$R_{DSON,L}$	0.21	0.35	0.60	$\Omega$	$I_{OUT,L} = 0.1\text{ A}$
all variants						
High level output voltage	$\Delta V_{OUT,H}$	–	–	0.3	V	$V_{CC2}-V_{OUT,H}$ ; $I_{OUT} = 20\text{ mA}$
Low level output voltage	$\Delta V_{OUT,L}$	–	–	0.1	V	$V_{CC2}-V_{OUT,H}$ ; $I_{OUT} = 20\text{ mA}$
Short circuit clamp voltage between $OUT+/CLAMP$ and $V_{CC2}$	$V_{CLP}$	–	–	2.0	V	Output on, $I_{OUT} = 500\text{ mA}$ , $t < 10\ \mu\text{s}$

<sup>1)</sup> Parameter is not subject to production test - verified by design/characterization

5 Electrical characteristics and parameters

5.3.4 Dynamic characteristics

Dynamic characteristics are measured with  $V_{VCC1} = 5\text{ V}$  and  $V_{VCC2} = 15\text{ V}$ .

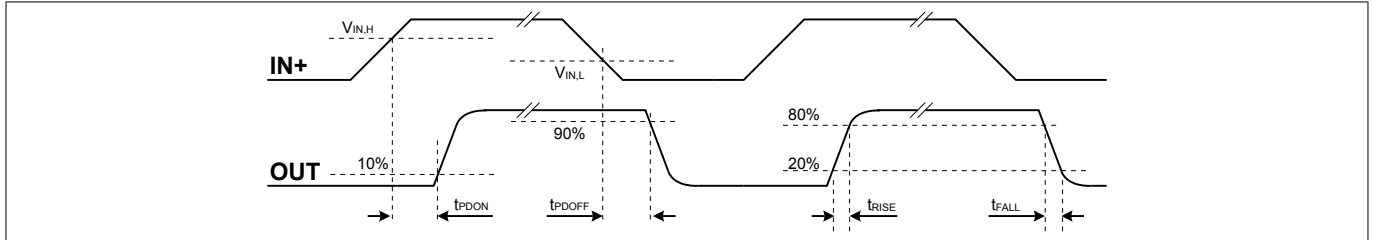


Figure 11 Propagation delay, rise and fall time

Table 9 Filter and propagation delay characteristics (1ED3131MC12H only)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	$t_{PDON}$	-	270	280	ns	$C_{LOAD} = 100\text{ pF}$ , $IN$ turn-on threshold to 10% output on
Input to output propagation delay OFF	$t_{PDOFF}$	-	270	280	ns	$C_{LOAD} = 100\text{ pF}$ , $IN$ turn-off threshold to 90% output off
Input to output propagation delay distortion	$t_{PDISTO}$	-15	0	15	ns	$t_{PDOFF} - t_{PDON}$
Input pulse suppression time (filter time)	$t_{INFLT}$	180	-	-	ns	shorter pulses will not propagate to the output
Minimum input pulse length	$t_{MININ}$	-	-	220	ns	-
Input to output propagation delay variation due to temperature	$t_{PD,T}$	-	-	14	ns	1)
Input to output propagation delay distortion variation due to temperature	$t_{PDISTO,T}$	-	-	5	ns	1)
Input to output, part to part propagation delay ON variation	$ t_{PDON,P2P} $	-	-	15	ns	1) 2) $C_{LOAD} = 100\text{ pF}$

1) Parameter is not subject to production test - verified by design/characterization

Table 10 Filter and propagation delay characteristics (all other variants)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	$t_{PDON}$	80	90	100	ns	$C_{LOAD} = 100\text{ pF}$ , $IN$ turn-on threshold to 10% output on
Input to output propagation delay OFF	$t_{PDOFF}$	80	90	100	ns	$C_{LOAD} = 100\text{ pF}$ , $IN$ turn-off threshold to 90% output off

(table continues...)

**5 Electrical characteristics and parameters**

**Table 10 (continued) Filter and propagation delay characteristics (all other variants)**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input to output propagation delay distortion	$t_{PDISTO}$	-5	0	5	ns	$t_{PD OFF} - t_{PD ON}$
Input pulse suppression time (filter time)	$t_{INFLT}$	30	-	-	ns	shorter pulses will not propagate to the output
Minimum input pulse length	$t_{MININ}$	-	-	40	ns	-
Input to output propagation delay variation due to temperature	$t_{PD,T}$	-	-	14	ns	1)
Input to output propagation delay distortion variation due to temperature	$t_{PDISTO,T}$	-	-	3	ns	1)
Input to output, part to part propagation delay ON variation	$ t_{PD on,P2P} $	-	-	7	ns	1) 2) $C_{LOAD} = 100 \text{ pF}$

- 1) Parameter is not subject to production test - verified by design/characterization  
 2) Absolute value at same ambient and operating conditions.

**Table 11 Dynamic output characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Rise time	$t_{RISE}$	-	-	15	ns	$C_{LOAD} = 100 \text{ pF}$
Fall time	$t_{FALL}$	-	-	15	ns	$C_{LOAD} = 100 \text{ pF}$
Rise time	$t_{RISE}$	-	-	30	ns	$C_{LOAD} = 1 \text{ nF}$
Fall time	$t_{FALL}$	-	-	30	ns	$C_{LOAD} = 1 \text{ nF}$

**5.3.5 Active shut down**

**Table 12 Active shut down**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Active shut down voltage, cold	$V_{ACTSD,C}$	-	-	1.9	V	$I_{OUT} = 10 \text{ mA}$ ; $V_{CC2}$ un-supplied; $T_A < 20^\circ\text{C}$
Active shut down voltage, hot	$V_{ACTSD,H}$	-	-	1.7	V	1) $I_{OUT} = 10 \text{ mA}$ ; $V_{CC2}$ un-supplied; $T_A \geq 20^\circ\text{C}$

- 1) Parameter is not subject to production test - verified by design/characterization



**6 Insulation characteristics**

**6 Insulation characteristics**

**Table 13 Safety limiting values**

This coupler is suitable for rated insulation only within the given safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

Description	Symbol	Characteristic	Unit
Maximum ambient safety temperature	$T_S$	150	°C
Maximum input-side power dissipation at $T_A = 25^\circ\text{C}^{1)}$	$P_{SI}$	100	mW
Maximum output-side power dissipation at $T_A = 25^\circ\text{C}^{2)}$	$P_{SO}$	1314	mW

1) IC input-side power dissipation is derated linearly with 11.4 mW/°C above 141 °C

2) IC output-side power dissipation is derated linearly with 8.8 mW/°C above 25°C

**6.1 Certified according to VDE 0884-11 reinforced insulation (Certificate no. 40052310)**

Valid for parts with part name 1ED31xxMC12H, x indicate different variants.

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

**Table 14 Reinforced insulation according to VDE 0884-11**

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V (rms) for rated mains voltage ≤ 300 V (rms) for rated mains voltage ≤ 600 V (rms) for rated mains voltage ≤ 1000 V (rms)		I-IV I-IV I-III I-II	–
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	$CLR$	>8	mm
Minimum external creepage	$CPG$	>8	mm
Minimum comparative tracking index	$CTI$	400	–
Apparent charge, method a $V_{pd(iini),a} = V_{IOTM}, V_{pd(m)} = 1.6 \times V_{IORM}, t_{ini} = 1 \text{ min}$	$q_c$	<5	pC
Apparent charge, method b $V_{pd(iini),b} = V_{IOTM} \times 1.2, V_{pd(m)} = 1.875 \times V_{IORM}, t_{ini} = 1 \text{ s}$	$q_c$	<5	pC
Isolation resistance at $T_{A,max}$	$R_{IO}$	$> 10^{11}$	Ω
Isolation resistance at $T_S$	$R_{IO_S}$	$> 10^9$	Ω
Maximum rated transient isolation voltage	$V_{IOTM}$	8000	V (peak)
Maximum repetitive insulation voltage	$V_{IORM}$	1767	V (peak)
Maximum surge isolation voltage for reinforced insulation $V_{TEST} = V_{IOSM} \times 1.6$	$V_{IOSM}$	6875	V (peak)

**(table continues...)**

**6 Insulation characteristics**

**Table 14 (continued) Reinforced insulation according to VDE 0884-11**

<b>Description</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
Insulation capacitance	$C_{10}$	0.9	pF

**6.2 Recognized under UL 1577 (File E311313)**

**Table 15 Recognized under UL 1577**

<b>Description</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
Insulation withstand voltage/1 min	$V_{ISO}$	5700	V (rms)
Insulation test voltage/1 s	$V_{ISO, TEST}$	6840	V (rms)

7 Package dimensions

7 Package dimensions

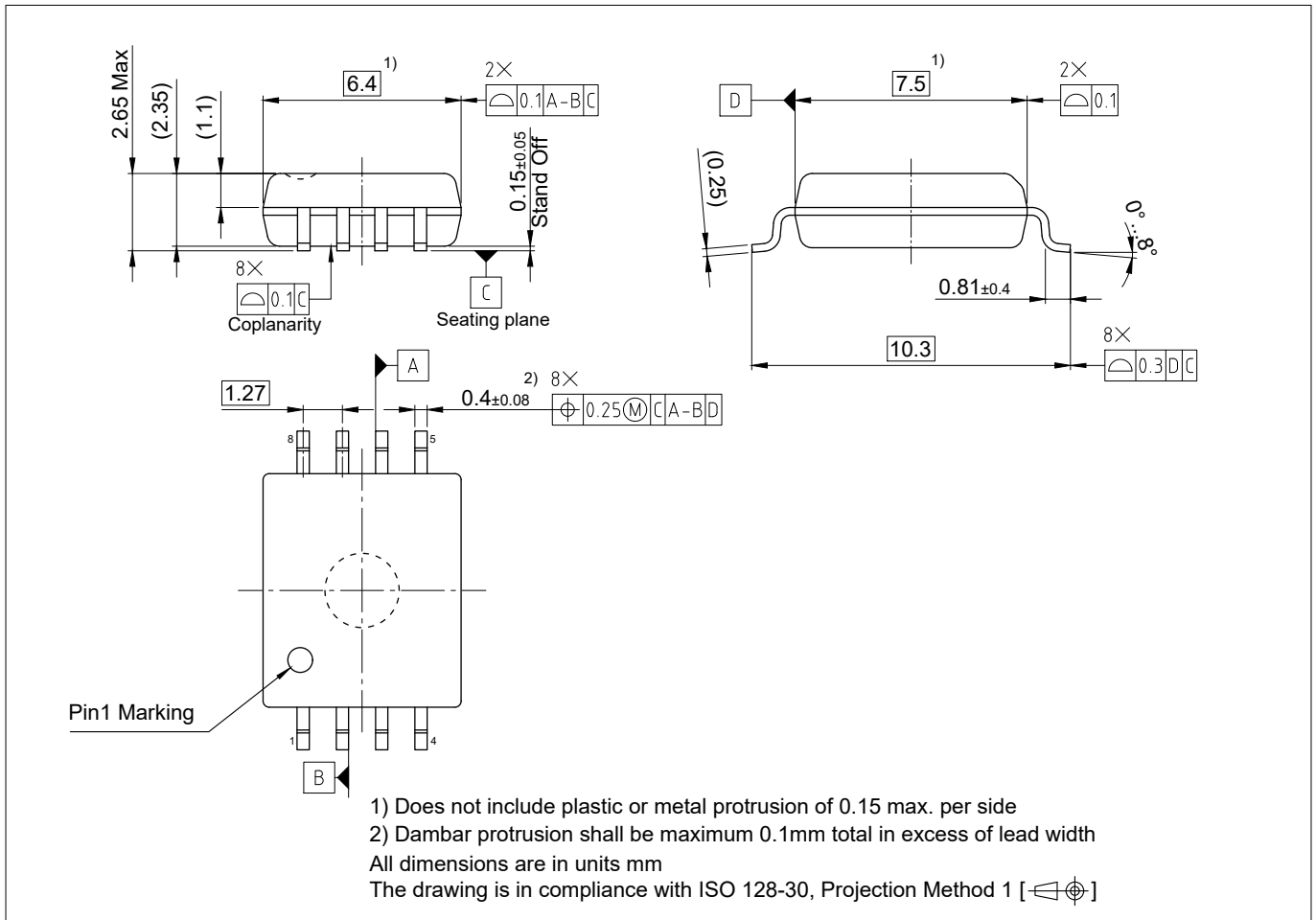


Figure 12 PG-DSO-8 (Plastic (green) dual small outline package, 300 mil)

Revision history

Reference	Description
v2.0 (2021-03-01)	<ul style="list-style-type: none"> <li>Final datasheet derived from 1ED31xxMU12H</li> <li><math>R_{DS(on)}</math> parameter values update</li> <li>ESD definition and VDE certification values updated</li> </ul>
(2021-09-01)	New version number schema: Target/Preliminary datasheet: 0.XY; Final datasheet: 1.XY
1.10 (2021-10-04)	<ul style="list-style-type: none"> <li>Certification information update (VDE certification)</li> <li>Fix unit and conditions in certification table according to standards</li> <li>Related product list update</li> <li>Added package marking information</li> </ul>