

Description

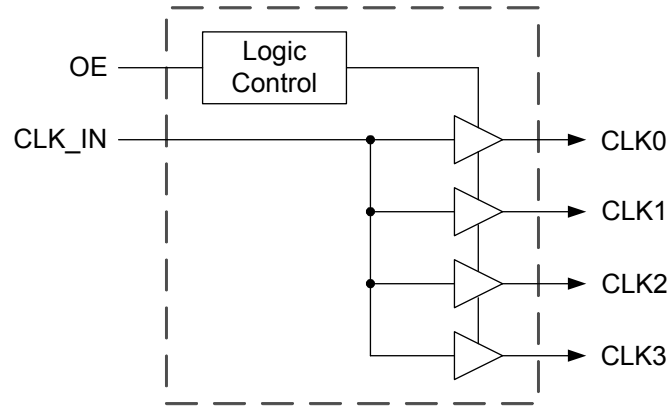
The 2304NZL is a high-performance, low skew, low jitter 1:4 LVCMOS clock buffer. The 2304NZL is ideal for PCI/PCI-X or networking applications.

The 2304NZL supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs.

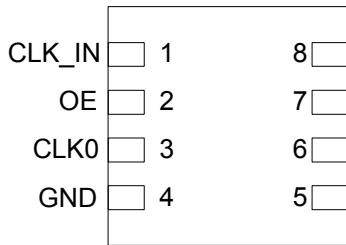
Features

- Low input to output propagation delay (1.8ns, 3.3V)
- Low output skew: 40ps max
- Glitch-free Output Enable Function
- 1.8V to 3.3V power supply
- Packaged in small 8-pin 2mm x 2mm DFN package, as well as standard TSSOP and SOIC packages
- Industrial temperature range (-40°C to +85°C)

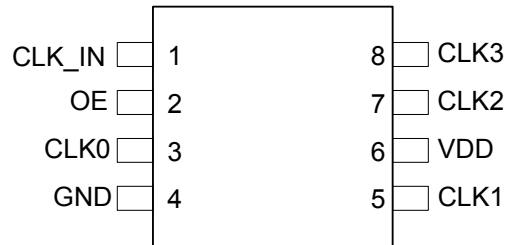
Block Diagram



Pin Assignment



8-pin DFN



8-pin TSSOP/SOIC

Functionality Table

Inputs		Outputs
CLK_IN	OE	CLK(3:0)
0	0	Low
0	1	0
1	0	Low
1	1	1

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK_IN	Input	Clock input.
2	OE	Input	Output Enable for the clock outputs. Outputs are enabled when forced HIGH. Outputs are forced to logic LOW when OE is forced LOW.
3	CLK0	Output	Clock output 0.
4	GND	Power	Power supply ground.
5	CLK1	Output	Clock output 1.
6	VDD	Power	Connect +1.8V, +2.5V or +3.3V power supply.
7	CLK2	Output	Clock output 2.
8	CLK3	Output	Clock output 3.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 6 and GND on pin 4, as close to the device as possible. A termination resistor should be used on each clock output if the trace is longer than 1 inch. See the Test Loads section for recommended values.

To achieve the low output skew that the 2304NZZL is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 2304NZL. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD	Power supply			4.6	V
Output Enable and All Outputs	VIO	With respect to GND	-0.5		VDD+0.5	V
ICLK	VIN	Input Voltage	-0.5		4.6	V
Ambient Operating Temperature	TAMB	Industrial Temperature	-40		85	°C
Storage Temperature	TSTORE	Storage Temperature	-65		150	°C
Junction Temperature	TJ	Junction Temperature			125	°C
Soldering Temperature	TSOLDER	Soldering Temperature			260	°C
ESD	ESD	Human Body Model	2000			V

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Temperature	TAMB	Ambient	-40	25	85	°C
Power Supply Voltage	VDD	With respect to GND	1.7		3.465	V

DC Electrical Characteristics

VDD=1.8 V \pm 5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71	1.8	1.89	V
Input High Voltage(CLK_IN, OE)	VIH	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	VIL	Note 1			0.2xVDD	V
Output High Voltage	VOH	IOH = -2 mA	0.9xVDD			V
Output Low Voltage	VOL	IOH = 2 mA			0.1xVDD	V
Operating Supply Current	IDD	No load, 50MHz		8		mA
Nominal Output Impedance	ZO			20		Ω
Input Capacitance	CIN	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD=2.5 V \pm 5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375	2.5	2.625	V
Input High Voltage(CLK_IN, OE)	VIH	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	VIL	Note 1			0.2xVDD	V
Output High Voltage	VOH	IOH = -2 mA	0.9xVDD			V
Output Low Voltage	VOL	IOH = 2 mA			0.1xVDD	V
Operating Supply Current	IDD	No load, 50MHz		10		mA
Nominal Output Impedance	ZO			21		Ω
Input Capacitance	CIN	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

VDD=3.3 V \pm 5%, Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Input High Voltage(CLK_IN, OE)	VIH	Note 1	0.8xVDD		3.45	V
Input Low Voltage(CLK_IN, OE)	VIL	Note 1			0.2xVDD	V
Output High Voltage	VOH	IOH = -2 mA	0.9xVDD			V
Output Low Voltage	VOL	IOH = 2 mA			0.1xVDD	V
Operating Supply Current	IDD	No load, 50MHz		12		mA
Nominal Output Impedance	ZO			25		Ω
Input Capacitance	CIN	CLK_IN, OE pin		5		pF

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

VDD=1.8V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	Fin		0		170	MHz
Output Rise Time	tOR	20% to 80% of VDD, CL=5 pF	0.7	1.1	1.5	ns
Output Fall Time	tOF	80% to 20% of VDD, CL=5 pF	0.7	1.1	1.5	ns
Propagation Delay	Note 1		2.2	2.5	3.2	ns
Additive Phase Jitter, RMS		125MHz		100		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD=2.5V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	Fin		0		200	MHz
Output Rise Time	tOR	20% to 80% of VDD, CL=5 pF	0.6	1	1.5	ns
Output Fall Time	tOF	80% to 20% of VDD, CL=5 pF	0.6	1	1.5	ns
Propagation Delay	Note 1		1.4	1.9	2.4	ns
Additive Phase Jitter, RMS		125MHz		50		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

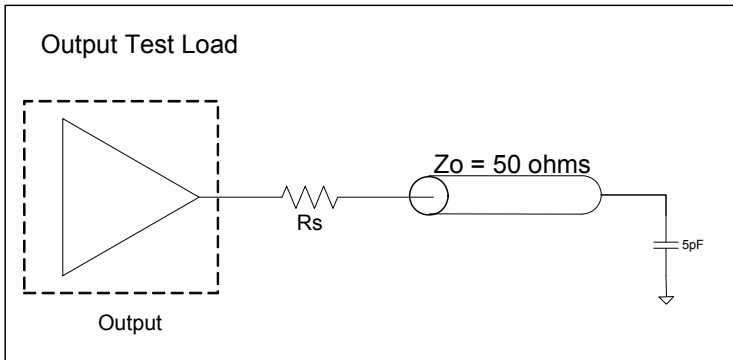
VDD=3.3 V ±5%, Ambient Temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	Fin		0		200	MHz
Output Rise Time	tOR	20% to 80% of VDD, CL=5 pF	0.5	1	1.5	ns
Output Fall Time	tOF	80% to 20% of VDD, CL=5 pF	0.5	1	1.5	ns
Propagation Delay	Note 1		1.1	1.7	2.1	ns
Additive Phase Jitter, RMS		125MHz		30		fs
Duty Cycle		50% input duty cycle	45		55	%
Output to Output Skew	Note 2	Rising edges at VDD/2		15	40	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Phase noise spec taken with Wenzel oscillator as reference input.

Test Load and Circuit



VDD	Rs (Ω)
1.8V	25
2.5V	29
3.3V	30

Thermal Characteristics (8DFN)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		81		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	1 m/s air flow		73		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	3 m/s air flow		70		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	θ_{JC}			10.6		$^{\circ}\text{C}/\text{W}$

Thermal Characteristics (8TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	1 m/s air flow		100		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	3 m/s air flow		80		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	θ_{JC}			35		$^{\circ}\text{C}/\text{W}$

Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	1 m/s air flow		100		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	3 m/s air flow		80		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	θ_{JC}			35		$^{\circ}\text{C}/\text{W}$

Package Outline and Dimensions (NTG8). Use EPAD P1 and LEAD Z1 options

TOP VIEW

BOTTOM VIEW

SIDE VIEW

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	Initial Release	3/5/15	J1HUA
01	Add Epad Option	8/5/15	J1HUA

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.035	0.05
A2	---	0.55	---
A3	0.203 REF		
b	0.20	0.25	0.30
D	2.00		
E	2.00		
e	0.50 BSC		
J	Please refer to table		
K	Please refer to table		
L	Please refer to table		

TOLERANCE OF FORM & POSITION

ddd	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.10

EPAD OPTION:

	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
J	0.80	0.90	1.00	0.70	0.80	0.90
K	1.50	1.60	1.70	1.10	1.20	1.30

LEAD OPTION:

	Z1			Z2		
	MIN	NOM	MAX	MIN	NOM	MAX
L	0.30	0.40	0.50	0.25	0.30	0.35

NOTES:

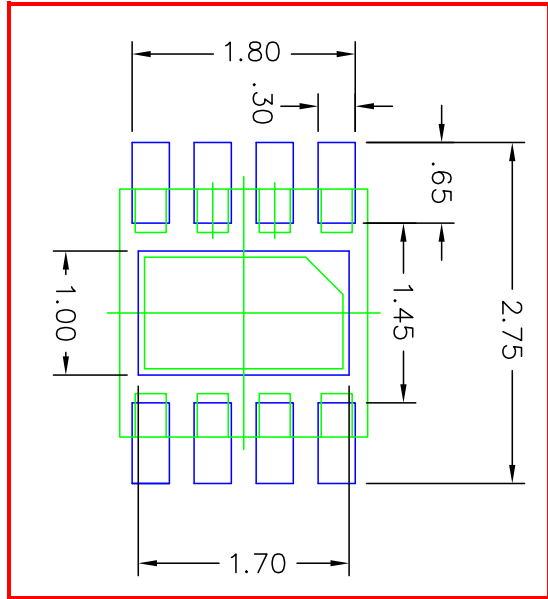
1. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
2. TOTAL THICKNESS NOT INCLUDE SAW BURR.

<p>TOLERANCES UNLESS SPECIFIED IN DECIMAL ANGULAR ±°</p> <p>XXX .05</p> <p>XXXX .030</p> <p>APPROVALS DATE</p> <p>DRAWN 02 3/5/15</p> <p>CHECKED</p>	<p>6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572</p> <p>WWW.IDT.COM</p> <p>6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572</p> <p>6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572</p>
<p>SIZE C</p> <p>DRAWING No. PSC-4604</p>	<p>REV 01</p>

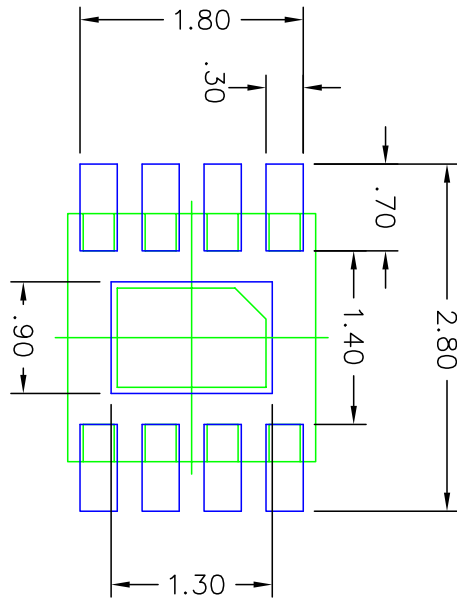
DO NOT SCALE DRAWING

SHEET 1 OF 2

Package Outline and Dimensions (NTG8), cont.



RECOMMENDED LAND PATTERN DIMENSION

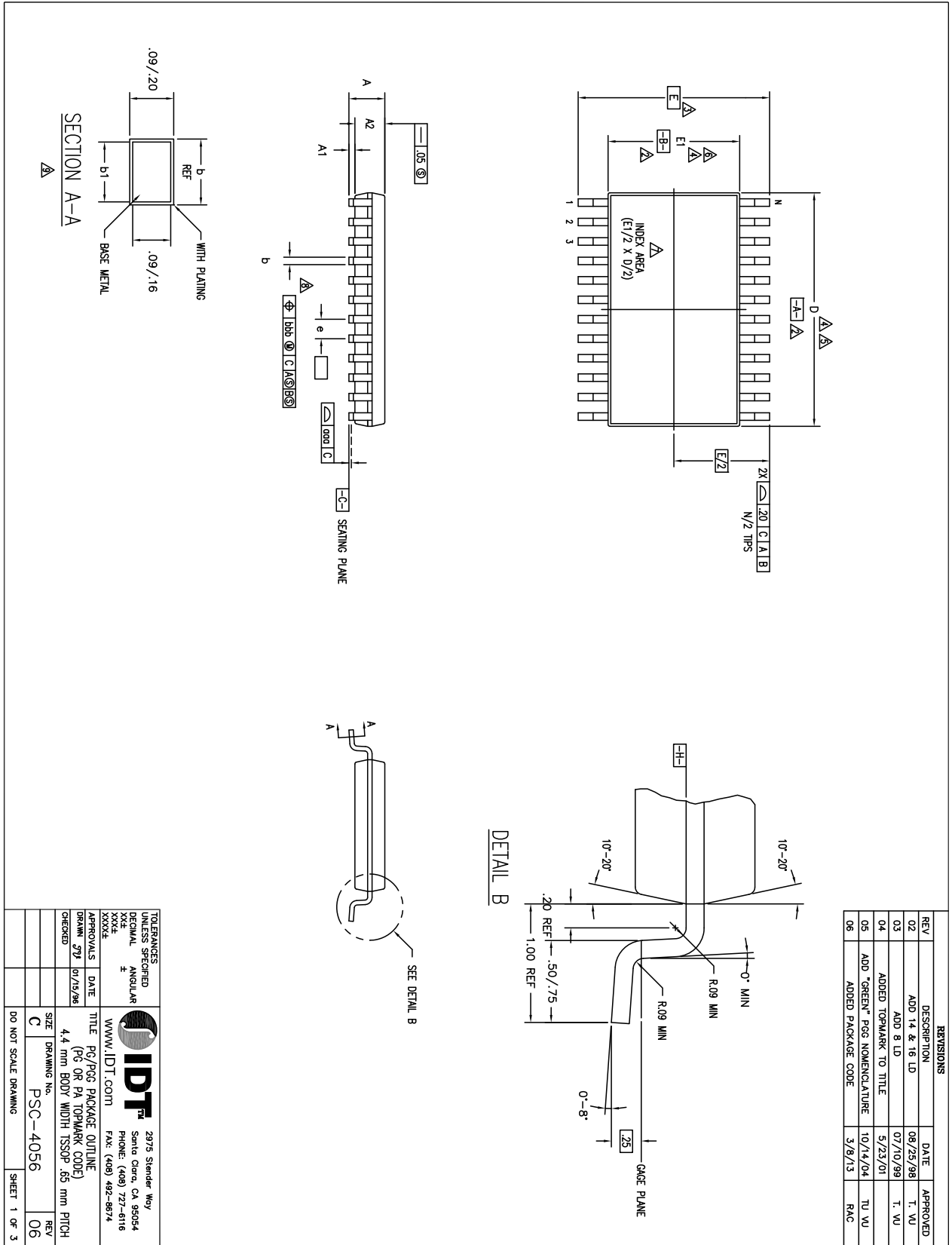


- NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW, AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE, NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	Initial Release	3/5/15	JHUA
01	Add Epod Option	8/5/15	JHUA

TOLERANCES UNLESS SPECIFIED	<p>6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572</p>
DECIMAL .1	
ANGULAR 1°	
XXX .05	
DATE 3/5/15	TITLE NTG8 PACKAGE OUTLINE
APPROVALS	2.0 x 2.0 mm BODY
CHECKED	0.5 mm PITCH TOPFN
SIZE C	DRAWING No. PSC-4604
DO NOT SCALE DRAWING	REV 01
SHEET 2 OF 2	

Package Outline and Dimensions (PGG8)



Package Outline and Dimensions (PGG8), cont.

SYMBOL	PGG8				PGG14				PGG16				PGG20				PGG24				PGG28			
	MIN	NOM	MAX	REF	MIN	NOM	MAX	REF	MIN	NOM	MAX	REF	MIN	NOM	MAX	REF	MIN	NOM	MAX	REF	MIN	NOM	MAX	REF
A	-.05	-.15	-.20	E	.05	-.15	-.20	E	.05	-.15	-.20	E	.05	-.15	-.20	E	.05	-.15	-.20	E	.05	-.15	-.20	E
A1	.80	1.00	1.05	E	.80	1.00	1.05	E	.80	1.00	1.05	E	.80	1.00	1.05	E	.80	1.00	1.05	E	.80	1.00	1.05	E
A2	2.90	3.00	3.10	4.5	4.90	5.00	5.10	4.5	4.90	5.00	5.10	4.5	6.40	6.50	6.60	4.5	7.70	7.80	7.90	4.5	9.60	9.70	9.80	4.5
D	6.40	BSC	3		6.40	BSC	3		6.40	BSC	3		6.40	BSC	3		6.40	BSC	3		6.40	BSC	3	
E1	4.30	4.40	4.50	4.6	4.30	4.40	4.50	4.6	4.30	4.40	4.50	4.6	4.30	4.40	4.50	4.6	4.30	4.40	4.50	4.6	4.30	4.40	4.50	4.6
e	.65	BSC			.65	BSC			.65	BSC			.65	BSC			.65	BSC			.65	BSC		
b	.19	-.30			.19	-.30			.19	-.30			.19	-.30			.19	-.30			.19	-.30		
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
ooo	-.10				-.10				-.10				-.10				-.10				-.10			
bbb	-.10				-.10				-.10				-.10				-.10				-.10			
N	8				14				16				20				24				28			

REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	TU VU
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC

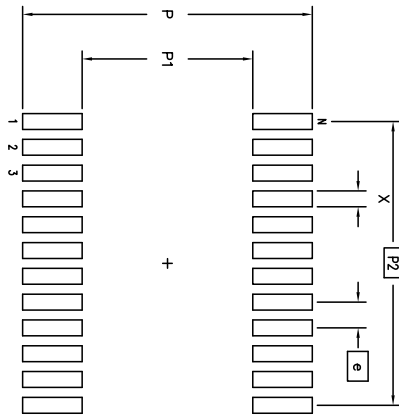
NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2 DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- 3 DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- 4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- 5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- 6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- 7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- 8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OR THE FOOT
- 9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED		2975 Stender Way	
DIMENSIONAL ANGULAR		Santa Clara, CA 95054	
XXX	F	Phone: (408) 727-6116	
XXXX		Fax: (408) 492-8574	
WWW.IDT.COM			
APPROVALS	DATE	TITLE	
DRAWN 797	07/15/98	PG/PGG PACKAGE OUTLINE	
CHECKED		(PG OR PA TOPMARK CODE)	
		4.4 mm BODY WIDTH TSSOP .65 mm PITCH	
		SIZE	REV
		C	06
		PSC-4056	
		DO NOT SCALE DRAWING	
		SHEET 2 OF 3	

Package Outline and Dimensions (PGG8), cont.

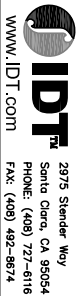
LAND PATTERN DIMENSIONS



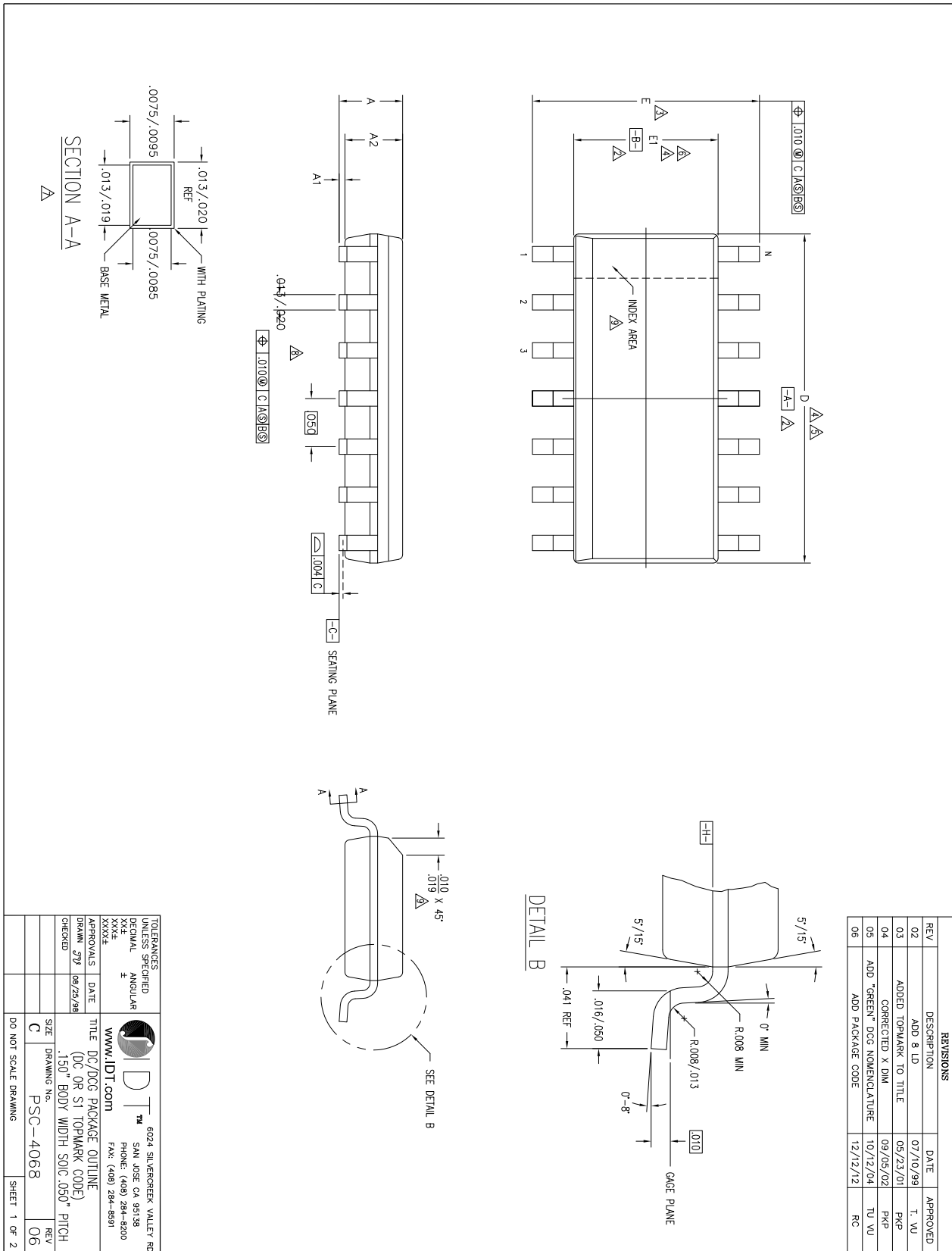
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20		24		28	

REVISIONS		
REV	DESCRIPTION	DATE
02	ADD 14 & 16 LD	08/25/98
03	ADD 8 LD	07/10/99
04	ADDED TOPMARK TO TITLE	5/23/01
05	ADD "GREEN" PFG NOMENCLATURE	10/14/04
06	ADDED PACKAGE CODE	3/8/13

TOLERANCES	
UNLESS SPECIFIED	
DECIMAL	ANGULAR
XXX±	±
XXXX	
APPROVALS	DATE
DRAWN 37J	07/15/98
CHECKED	
SIZE	DRAWING No.
C	PSC-4056
DO NOT SCALE DRAWING	SHEET 3 OF 3



Package Outline and Dimensions (DCG8)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD B LD	07/10/99	T. VU
03	ADDED TOPMARK TO TITLE	05/23/01	PKP
04	CORRECTED X DIM	09/05/02	PKP
05	ADD "GREEN" DCG NOMENCLATURE	10/12/04	TU VU
06	ADD PACKAGE CODE	12/12/12	RC

TOLERANCES UNLESS SPECIFIED DECIMAL ± ANGULAR ± XXXX XXXXX		6024 SILVERCREAK VALLEY RD SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8991	
APPROVALS DRAWN: 279 CHECKED:	DATE: 08/25/98	TITLE: DC/DCG PACKAGE OUTLINE (DC OR S1 TOPMARK CODE) .150" BODY WIDTH SOIC .050" PITCH	SIZE: C DRAWING No.: PSC-4068 REV: 06
DO NOT SCALE DRAWING		SHEET 1 OF 2	

Package Outline and Dimensions (DCG8), cont.

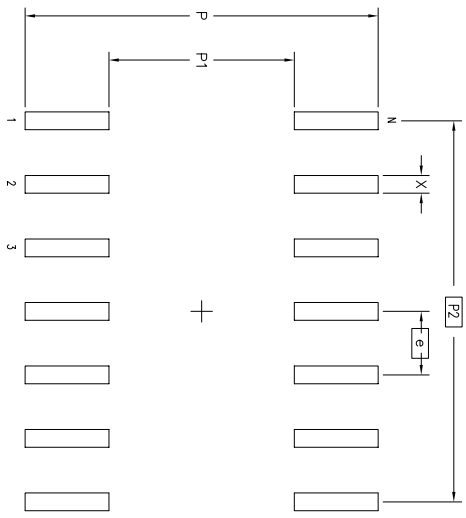
DC/DCG8					DC/DCG14					DC/DCG16					
S M B D	JEDEC VARIATION			N D T E	S M B D	JEDEC VARIATION			N D T E	S M B D	JEDEC VARIATION			N D T E	
	AA	NOM	MAX			AB	NOM	MAX			AC	NOM	MAX		
A	.053	.064	.068			.053	.064	.068			.053	.064	.068		
A1	.004	.006	.010			.004	.006	.010			.004	.006	.010		
A2	.055	.058	.061	11		.055	.058	.061	11		.055	.058	.061	11	
D	.189	.194	.197	4.5		.337	.342	.344	4.5		.386	.391	.393	4.5	
E	.230	.236	.244	3		.230	.236	.244	3		.230	.236	.244	3	
E1	.150	.155	.157	4.6		.150	.155	.157	4.6		.150	.155	.157	4.6	
N	8					14					16				

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-012, VARIATION AA, AB & AC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 8 LD	07/10/99	T. WU
03	ADDED TOPMARK TO TITLE	05/23/01	PKP
04	CORRECTED X DIM	09/05/02	PKP
05	ADD "GREEN" DCG NOMENCLATURE	10/12/04	TU WU
06	ADD PACKAGE CODE	12/12/12	RC

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150
P2	.150 BSC	.300 BSC	.150 BSC	.350 BSC	.150 BSC	.350 BSC
X	.015	.024	.015	.024	.015	.024
e	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC	.050 BSC
N	8		14		16	

TOLERANCES UNLESS SPECIFIED
 DECIMAL ±
 ANGULAR ±

APPROVALS
 DATE: 08/25/98
 DRAWN: JTY
 CHECKED:

APPROVALS
 DATE:

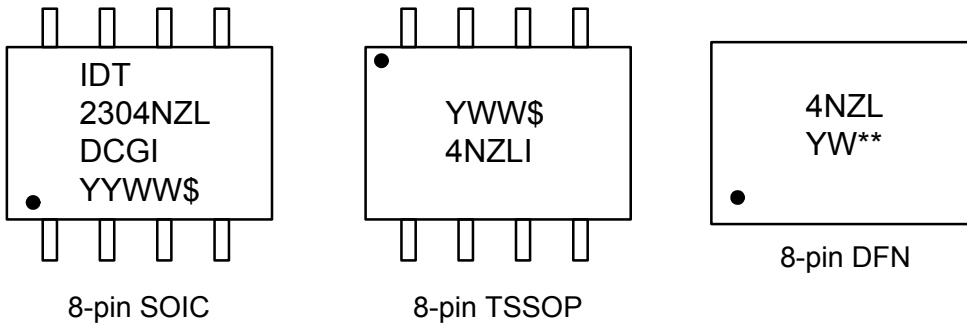
SIZE C
DRAWING No. PSC-4068
REV 06

DO NOT SCALE DRAWING SHEET 2 OF 2

IDT
 6024 SILVERCREST VALLEY RD
 SAN JOSE CA 95138
 PHONE: (408) 284-8200
 FAX: (408) 284-8591
 www.IDT.com

TITLE DC/DCG PACKAGE OUTLINE
 (DC OR ST TOPMARK CODE)
 .150" BODY WIDTH SOIC .050" PITCH

Marking Diagrams



Notes:

1. "***" is the lot number (DFN only).
2. "YYWW" or "YWW" or "YW" is the digits of the year and week that the part was assembled.
3. "\$" is the mark code.
4. "G" denotes RoHS compliant package.
5. "I" denotes industrial temperature range.
6. Bottom markings: lot number and country of origin for TSSOP; lot number for SOIC.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
2304NZLDCGI	Tubes	8-pin SOIC	-40 to +85°
2304NZLDCGI8	Tape and Reel	8-pin SOIC	-40 to +85°
2304NZLPGGI	Tubes	8-pin TSSOP	-40 to +85°
2304NZLPGGI8	Tape and Reel	8-pin TSSOP	-40 to +85°
2304NZLNTGI	Tubes	8-pin DFN	-40 to +85°
2304NZLNTGI8	Tape and Reel	8-pin DFN	-40 to +85°

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	06/21/16	H.G.	1. Added marking diagrams. 2. Moved to final.
B	01/31/17	Y.G.	1. Updates to operating supply current and output impedance values in DC electrical tables. 2. Added Rs values to test loads.



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