

2N3821, 2N3822 N-Channel JFET

Features

- InterFET [N0032H Geometry](#)
- Typical Noise: 7 nV/VHz
- Low Ciss: 6.0pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- VHF Amplifiers
- Small Signal Amplifier

Description

The -50V InterFET 2N3821 and 2N3822 are targeted for sensitive amplifier stages for VHF designs. Gate leakages are typically less than 10pA at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

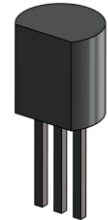
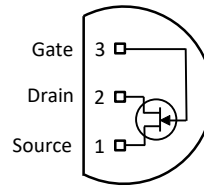
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	2N3821 Min	2N3822 Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-50	-50	V
I_{DSS} Drain to Source Saturation Current	0.5	2	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage			V
G_{FS} Forward Transconductance	1500	3000	μS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N3821; 2N3822	Through-Hole	TO-72	Bulk
PN3821; PN3822	Through-Hole	TO-92	Bulk
SMP3821; SMP3822	Surface Mount	SOT23	Bulk
SMP3821TR; SMP3822TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N3821COT; 2N3822COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N3821CFT; 2N3822CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-50	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	300	mW
P Power Derating	2	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N3821		2N3822		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-50		-50		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -30V, V_{DS} = 0V, T_A = 25^\circ\text{C}$ $V_{GS} = -30V, V_{DS} = 0V, T_A = 150^\circ\text{C}$		-0.1		-0.1	nA
			-0.1		-0.1	μA
V_{GS} Gate to Source Voltage	$V_{DS} = 15V, I_D = ()$	-0.5 (50)	-2 (50)	-1 (200)	-4 (200)	V μA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.5\text{nA}$		-4		-6	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	0.5	2.5	2	10	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N3821		2N3822		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{kHz}$	1500	4500	3000	6500	μS
G_{OS} Output Conductance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{kHz}$		10		20	μS
$ Y_{fs} $ Forward Transmittance	$V_{DS} = 15V, V_{GS} = 0V, f = 100\text{MHz}$	1500		3000		μS
C_{iss} Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{MHz}$		6		6	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1\text{MHz}$		2		2	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 15V, V_{GS} = 0V, f = 10\text{Hz}$		200		200	nV/ $\sqrt{\text{Hz}}$
NF Noise Figure	$V_{DS} = 15V, V_{GS} = 0V, f = 10\text{Hz}$ $R_G = 1\text{M}\Omega$		5		5	dB

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.