

2N4391, 2N4392, 2N4393 N-Channel JFET

Features

- InterFET [N0132S Geometry](#)
- Low Noise: 1.2 nV/√Hz Typical
- Fast Switching
- Low Cutoff Voltage: 2N4393 < 3.0V
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

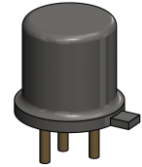
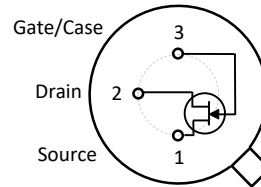
Applications

- Low On Resistance Analog Switches
- Choppers
- Commutators

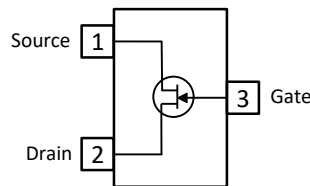
Description

The -40V InterFET 2N4391, 2N4392 and 2N4393 are targeted for switch, chopper and commutator designs. Gate leakages are typically less than 50pA at room temperatures. The 2N4393 has a cutoff voltage of less than 3.0V ideal for low-level power supplies. The TO-18 package is hermetically sealed and suitable for military applications.

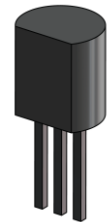
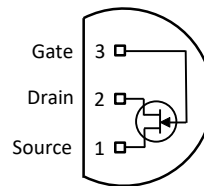
TO-18 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	2N4391 Min	2N4392 Min	2N4393 Min	Unit
BV _{GSS} Gate to Source Breakdown Voltage	-40	-40	-40	V
I _{DSS} Drain to Source Saturation Current	50	25	5	mA
V _{GS(off)} Gate to Source Cutoff Voltage	-4	-2	-0.5	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4391; 2N4392; 2N4393	Through-Hole	TO-18	Bulk
PN4391; PN4392; PN4393	Through-Hole	TO-92	Bulk
SMP4391; SMP4392; SMP4393	Surface Mount	SOT23	Bulk
SMP4391TR; SMP4392TR SMP4393TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4391COT; 2N4392COT 2N4393COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4391CFT; 2N4392CFT 2N4393CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation	1800	mW
P Power Derating	12	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N4391		2N4392		2N4393		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-40		-40		-40		V
I_{GSS} Gate to Source Reverse Current	$V_{DS} = -20V, V_{GS} = 0V, T_A = 25^\circ\text{C}$ $V_{DS} = -20V, V_{GS} = 0V, T_A = 150^\circ\text{C}$		-100 -200		-100 -200		-100 -200	pA nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1\text{nA}$	-4	-10	-2	-5	-0.5	-3	V
$V_{GS(F)}$ Gate to Source Forward Voltage	$V_{DS} = 0V, I_G = 1\text{mA}$		1		1		1	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 20V$ (Pulsed)	50	150	25	75	5	30	mA
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = 20V, V_{GS} = -5V, T_A = 25^\circ\text{C}$						100	pA
	$V_{DS} = 20V, V_{GS} = -5V, T_A = 150^\circ\text{C}$						200	nA
	$V_{DS} = 20V, V_{GS} = -7V, T_A = 25^\circ\text{C}$				100			pA
	$V_{DS} = 20V, V_{GS} = -7V, T_A = 150^\circ\text{C}$				200			nA
	$V_{DS} = 20V, V_{GS} = -12V, T_A = 25^\circ\text{C}$ $V_{DS} = 20V, V_{GS} = -12V, T_A = 150^\circ\text{C}$		100 200					pA nA
$V_{DS(ON)}$ Drain to Source ON Voltage	$V_{GS} = 0V, I_D = 3\text{mA}$						0.4	V
	$V_{GS} = 0V, I_D = 6\text{mA}$				0.4			
	$V_{GS} = 0V, I_D = 12\text{mA}$		0.4					
$R_{DS(ON)}$ Static Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 1\text{mA}$		30		60		100	Ω

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	2N4391		2N4392		2N4393		Unit
		Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{GS} = 0V, I_D = 0A, f = 1\text{kHz}$		30		60		100	Ω
C_{iss} Input Capacitance	$V_{DS} = 20V, V_{GS} = 0V, f = 1\text{MHz}$		14		14		14	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 0V, V_{GS} = -5V, f = 1\text{MHz}$						3.5	pF
	$V_{DS} = 0V, V_{GS} = -7V, f = 1\text{MHz}$				3.5			
	$V_{DS} = 0V, V_{GS} = -12V, f = 1\text{MHz}$		3.5					
t_d Turn-On Delay Time	$V_{DD} = 10V, V_{GS(ON)} = 0V$		15		15		15	ns
t_r Rise Time	$V_{DD} = 10V, V_{GS(ON)} = 0V$		5		5		5	ns
$t_{D(OFF)}$ Turn-Off Delay Time	$V_{DD} = 10V, V_{GS(ON)} = 0V$		20		35		50	ns
t_f Fall Time	$V_{DD} = 10V, V_{GS(ON)} = 0V$		15		20		30	ns

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

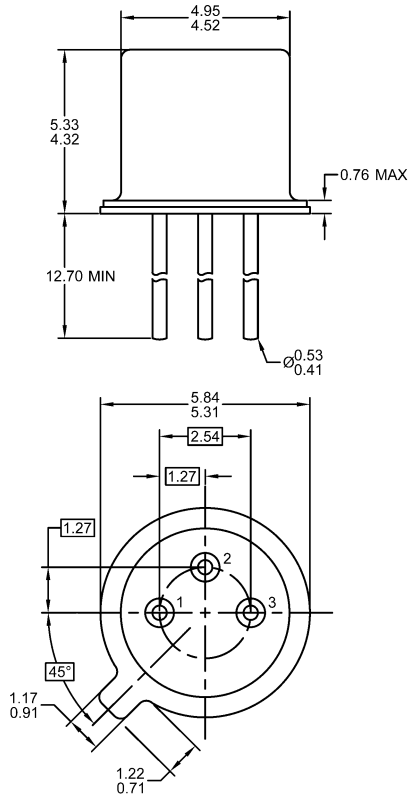
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

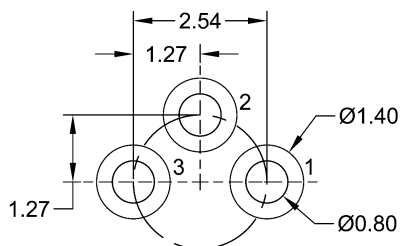
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.