2N5020, 2N5021 P-Channel JFET

Features

- InterFET P0032F Geometry
- Typical Noise: 10 nV/√Hz
- Low Ciss: 3.2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

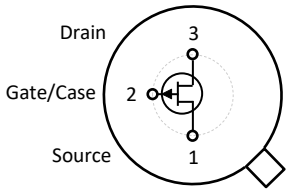
Applications

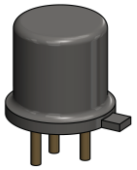
- Analog Switches
- Choppers

Description

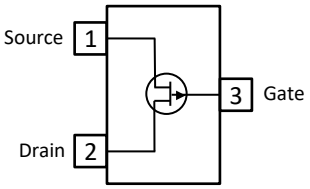
The 25V InterFET 2N5020 and 2N5021 are targeted for data switches and low-level chopper designs. Gate leakages are typically less than 1nA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

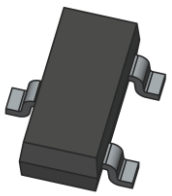
TO-18 Bottom View



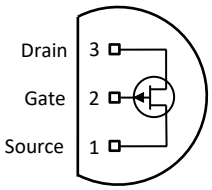


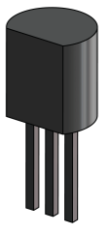
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		2N5020 Min	2N5021 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	25	25	V
I_{DSS}	Drain to Source Saturation Current	-0.3	-1	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	0.3	0.5	V
G_{FS}	Forward Transconductance	1000	1500	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N5020; 2N5021	Through-Hole	TO-18	Bulk
PN5020; PN5021	Through-Hole	TO-92	Bulk
SMP5020; SMP5021	Surface Mount	SOT23	Bulk
SMP5020TR; SMP5021TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N5020COT; 2N5021COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N5020CFT; 2N5021CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	25	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	500	mW
P	Power Derating	4	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

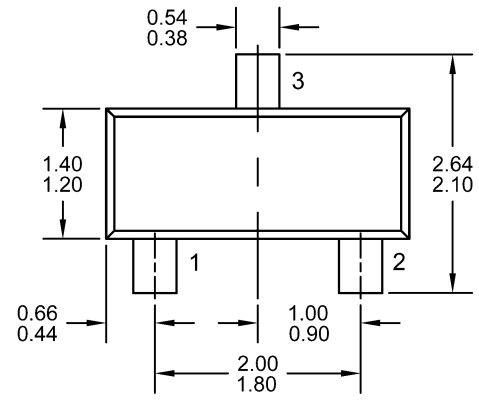
Parameters		Conditions	2N5020		2N5021		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 1µA	25		25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = 15V, V_{DS} = 0V		1		1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = 1nA	0.3	1.5	0.5	2.5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -15V (Pulsed)	-0.3	-1.2	-1	-3.5	mA

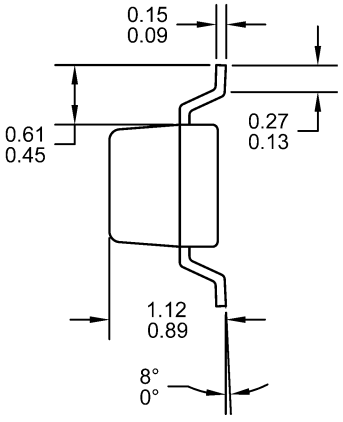
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

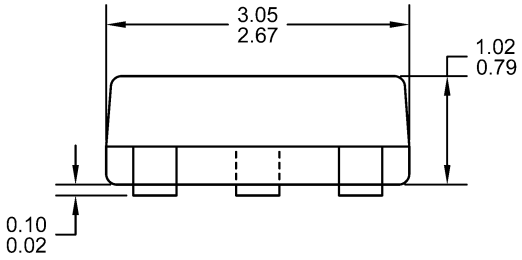
Parameters		Conditions	2N5020		2N5021		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz	1000	3500	1500	6000	µS
G_{OS}	Output Conductance	V_{DS} = -15V, V_{GS} = 0V, f = 1kHz		20		20	µS
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		25		25	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		7		7	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

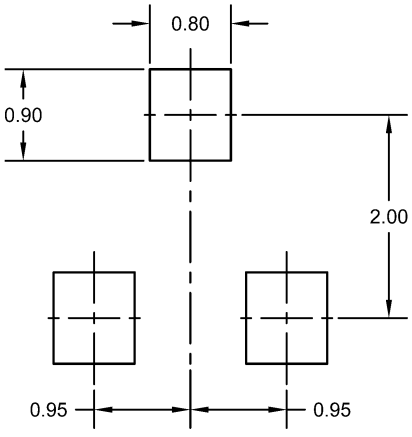






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

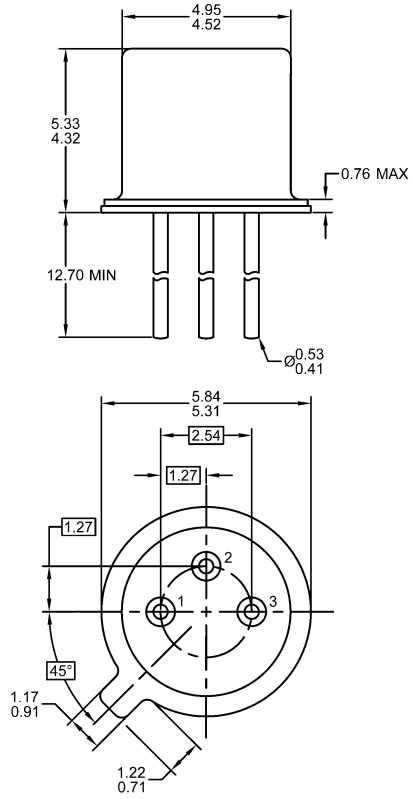
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

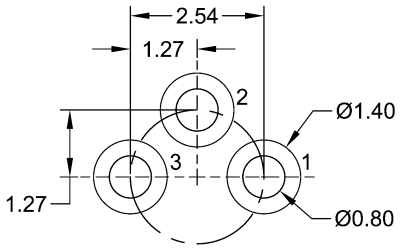
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.