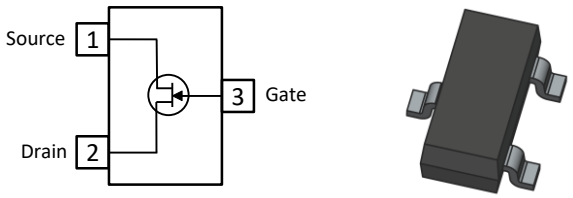
2N5484, 2N5485, 2N5486 N-Channel JFET

Features

- InterFET N0026S Geometry
- Low Noise: 4 nV/√Hz Typical
- Low Ciss: 4.3pF Typical
- Low Leakage: 10pA Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

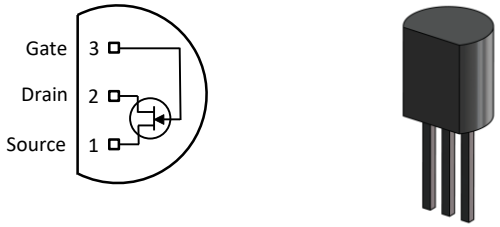
SOT23 Top View



Applications

- VHF/UHF Amplifiers

TO-92 Bottom View



Description

The -25V InterFET 2N5484, 2N5485, and 2N5486 are targeted for low noise low leakage VHF/UHF amplifier designs. Gate leakages are typically less than 10pA at room temperatures.

Product Summary

Parameters		2N5484 Min	2N5485 Min	2N5486 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-25	-25	-25	V
I_{DSS}	Drain to Source Saturation Current	1	4	8	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3	-0.5	-2	V
G_{FS}	Forward Transconductance	2500	3000	3500	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N5484; 2N5485; 2N5486	Through-Hole	TO-92	Bulk
SMP5484; SMP5485; SMP5486	Surface Mount	SOT23	Bulk
SMP5484TR; SMP5485TR; SMP5486TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N5484COT; 2N5485COT; 2N5486COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N5484CFT; 2N5485CFT; 2N5486CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-25	V
I_{FG}	Continuous Forward Gate Current	-25	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	3.27	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

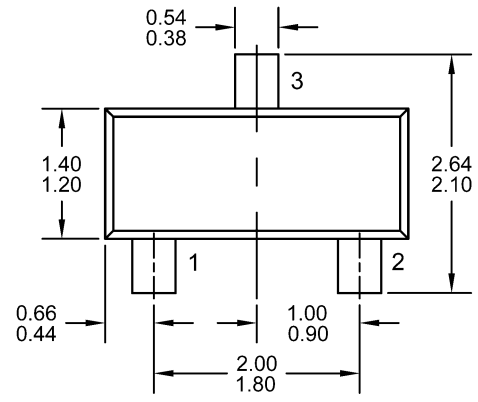
Parameters		Conditions	2N5484		2N5485		2N5486		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 1µA	-25		-25		-25		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V, T_A = 25°C		-1		-1		-1	nA
		V_{GS} = -20V, V_{DS} = 0V, T_A = 100°C		-0.2		-0.2		-0.2	µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 10nA	-0.3	-3	-0.5	-4	-2	-6	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 15V, V_{GS} = 0V (Pulsed)	1	5	4	10	8	20	mA

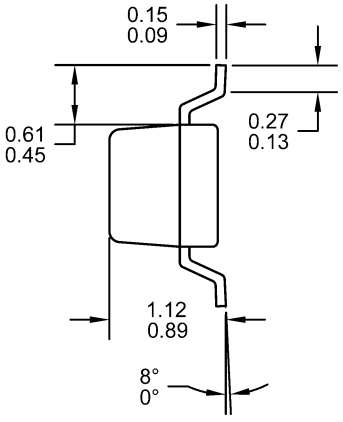
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

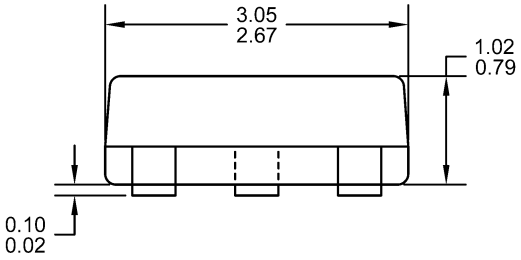
Parameters		Conditions	2N5484		2N5485		2N5486		Unit
			Min	Max	Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 15V, V_{GS} = 0V, f = 100MHz	2500						µS
		V_{DS} = 15V, V_{GS} = 0V, f = 400MHz			3000		3500		
G_{OS}	Output Conductance	V_{DS} = 15V, V_{GS} = 0V, f = 100MHz		75					µS
		V_{DS} = 15V, V_{GS} = 0V, f = 400MHz				100		100	
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		5		5		5	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		1		1		1	pF
C_{oss}	Output Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		2		2		2	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

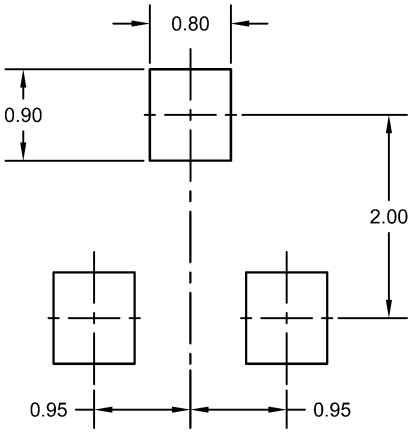






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.