2SC0650P2Ax-17 Preliminary Data Sheet

Dual-Channel High-Power High-Frequency SCALE-2 Driver Core

Short Description

The SCALE-2 dual driver core 2SC0650P2Ax-17 combines highest power density with broad applicability. The driver is designed for both high-power and high-frequency applications requiring maximum reliability. It is suitable for IGBTs with reverse voltages up to 1700V and also features a dedicated MOSFET mode. The embedded paralleling capability allows easy inverter design covering higher power ratings. Multi-level topologies are also supported.

CONCEPT's patented planar-transformer technology assures efficient and high-voltage isolation with long-term reliability and sets new milestones in compactness, interference immunity and performance. Its outstanding EMC with a dv/dt strength of more than 100V/ns allows safe and reliable operation in even the toughest industrial applications.

Thanks to its ultra-flat design with an insertion height of max. 6.5mm and a footprint of 61.7mm x 57.2, the 2SC0650P2Ax-17 can efficiently utilize even the most constrained insertion spaces. Compared with conventional drivers, the highly integrated SCALE-2 chipset allows about 85% of components to be dispensed with. This advantage is impressively reflected in increased reliability at simultaneously minimized cost.

Equipped with the latest SCALE-2 technology, the driver core opens up the possibility of working with clock frequencies of up to 150kHz – at best-in-class efficiency. The 2SC0650P2Ax-17 combines a complete two-channel driver core with all components required for driving, such as an isolated DC/DC converter, short-circuit protection, advanced active clamping as well as supply voltage monitoring. Each of the two output channels is electrically isolated from the primary side and the other secondary channel.

Product Highlights

- ✓ Ultra-flat dual channel driver
- ✓ Highly integrated SCALE-2 chipset
- ✓ Planar transformer technology
- ✓ Blocking voltages up to 1700V
- ✓ Switching frequency up to 150kHz
- ✓ Short delay and extremely small jitter
- ✓ Gate current ±50A, 6W output power per channel
- ✓ +15V/-10V gate driving
- ✓ Safe isolation to EN 50178
- ✓ UL compliant

Applications

- ✓ Wind power converters
- ✓ Industrial drives
- ✓ Traction applications
- ✓ Electro/hybrid drive commercial vehicles
- ✓ Driving parallel-connected large IGBTs
- ✓ High gate-current driving applications
- ✓ Induction heating
- ✓ Switched mode power supplies (SMPS)
- ✓ Laser and medical (MRT, CT, X-Ray)
- ✓ Laser technology

Preliminary Data Sheet

Safety Notice!

The data contained in this data sheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory!

Any handling of electronic devices is subject to the general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

Important Product Documentation

This data sheet contains only product-specific data. For a detailed description, must-read application notes and important information that apply to this product, please refer to "2SC0650P Description & Application Manual" on www.IGBT-Driver.com/go/2SC0650P

Absolute Maximum Ratings

Parameter	Remarks	Min	Max	Unit
Supply voltage V_{DC}	VDC to GND	0	16	V
Supply voltage V_{CC}	VCC to GND	0	16	V
Logic input and output voltages	Primary side, to GND	-0.5	VCC+0.5	V
SOx current	Failure condition, total current		20	mA
Gate peak current I_{out}	Note 1	-50	+50	A
External gate resistance	Turn-on and turn-off	0.5		Ω
Average supply current I_{DC}	Notes 2, 3		1300	mA
Output power	Ambient temperature <70°C (Notes 4, 5)		6.5	W
	Ambient temperature 85°C (Note 4)		6	W
Switching frequency F			150	kHz
Test voltage (50Hz/1min.)	Primary to secondary (Note 15)		5000	$V_{AC(eff)}$
	Secondary to secondary (Note 15)		4000	$V_{AC(eff)}$
|dV/dt|	Rate of change of input to output voltage (Note 11)		100	kV/µs
Operating voltage	Primary/secondary, secondary/secondary		1700	V_{peak}
Operating temperature	Note 5	-40	+85	°C
Storage temperature		-40	+90	°C

Recommended Operating Conditions

Power Supply	Remarks	Min	Typ	Max	Unit
Supply voltage V_{DC}	VDC to GND	14.5	15	15.5	V
Supply voltage V_{CC}	VCC to GND	14.5	15	15.5	V

Electrical Characteristics (IGBT mode)

All data refer to +25°C and V_{CC} = V_{DC} = 15V unless otherwise specified.

Power supply	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Supply current I_{DC}	Without load		40		mA
Supply current I_{CC}	F = 0Hz		21		mA
Supply current I_{CC}	F = 150kHz		35		mA
Coupling capacitance C_{io}	Primary to output, total		28		pF
Power Supply Monitoring	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Supply threshold V_{CC}	Primary side, clear fault	11.9	12.6	13.3	V
	Primary side, set fault (Note 12)	11.3	12.0	12.7	V
Monitoring hysteresis	Primary side, set/clear fault	0.35			V
Supply threshold V_{ISOx}-V_{Ex}	Secondary side, clear fault	12.1	12.6	13.1	V
	Secondary side, set fault (Note 13)	11.5	12.0	12.5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.35			V
Supply threshold V_{Ex}-V_{COMx}	Secondary side, clear fault	5	5.15	5.3	V
	Secondary side, set fault (Note 13)	4.7	4.85	5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.15			V
Logic Inputs and Outputs	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Input bias current	V(INx) > 3V		190		µA
Turn-on threshold	V(INx)		2.6		V
Turn-off threshold	V(INx)		1.3		V
SOx output voltage	Failure condition, I(SOx)<20mA			0.7	V
Short-Circuit Protection	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Current through pin REFx	R(REFx, VEx)<70kΩ		150		µA
Minimum response time	Note 9		1.2		µs
Minimum blocking time	Note 10		9		µs
Timing Characteristics	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Turn-on delay $t_{d(on)}$	Note 6		80		ns
Turn-off delay $t_{d(off)}$	Note 6		75		ns
Jitter of turn-on delay	Note 17		±2		ns
Jitter of turn-off delay	Note 17		±2		ns
Output rise time $t_{r(out)}$	Note 7		25		ns
Output fall time $t_{f(out)}$	Note 7		25		ns
Transmission delay of fault state	Note 14		400		ns

Electrical Isolation	Remarks	Min	Typ	Max	Unit
Test voltage (50Hz/1s)	Primary to secondary side (Note 15)	5000	5050	5100	V_{eff}
Partial discharge extinction volt.	Primary to secondary side (Note 16)	1768			V_{peak}
Creepage distance	Primary to secondary side	15			mm
	Secondary to secondary side	25			mm
Clearance distance	Primary to secondary side	15			mm
	Secondary to secondary side	6.5			mm

Output	Remarks	Min	Typ	Max	Unit
Blocking capacitance	VISOx to VEx (Note 8)		9.4		µF
	VEx to COMx (Note 8)		9.4		µF

Output voltage swing

The output voltage swing consists of two distinct segments. First, there is the turn-on voltage V_{GHx} between pins GHx and VEx. V_{GHx} is regulated and maintained at a constant level for all output power values and frequencies.
The second segment of the output voltage swing is the turn-off voltage V_{GLx}. V_{GLx} is measured between pins GLx and VEx. It is a negative voltage. It changes with the output power to accommodate the inevitable voltage drop across the internal DC/DC converter.

Output Voltage	Remarks	Min	Typ	Max	Unit
Turn-on voltage, V_{GHx}	Any load condition		15.0		V
Turn-off voltage, V_{GLx}	No load		-11.4		V
Turn-off voltage, V_{GLx}	1W output power		-9.3		V
Turn-off voltage, V_{GLx}	6W output power		-8.1		V

Footnotes to the Key Data

1) The maximum peak gate current refers to the highest current level occurring during the product lifetime. It is an absolute value and does also apply for short pulses.
2) The average supply input current is limited for thermal reasons. Higher values than specified by the absolute maximum rating are permissible (e.g. during power supply start up) if the average remains below the given value, provided the average is taken over a time period which is shorter than the thermal time constants of the driver in the application.
3) There is no means of actively controlling or limiting the input current in the driver. In the case of start-up with very high blocking capacitor values, or in case of short circuit at the output, the supply input current has to be limited externally.
4) The maximum output power must not be exceeded at any time during operation. The absolute maximum rating must also be observed for time periods shorter than the thermal time constants of the driver in the application.
5) An extended output power range is specified in the output power section for maximum ambient temperatures of 70°C. In that case, the absolute maximum rating for the operating temperature changes to (–40°C - 70°C) and the absolute maximum output power rating changes to 6.5W.
6) The delay time is measured between 50% of the input signal and 10% voltage swing of the corresponding output. The delay time is independent of the output loading.

7) Output rise and fall times are measured between 10% and 90% of the nominal output swing with an output load of 4.7Ω and 270nF. The values are given for the driver side of the gate resistors. The time constant of the output load in conjunction with the present gate resistors leads to an additional delay at the load side of the gate resistors.
8) External blocking capacitors are to be placed between VISOx and VEx as well as VEx and COMx for gate charges exceeding 3µC. Ceramic capacitors are recommended. A minimum external blocking capacitance of 3µF is recommended for every 1µC of gate charge beyond 3µC. Insufficient external blocking can lead to reduced driver efficiency and thus to thermal overload.
9) The minimum response time given is valid for the circuit given in the description and application manual (Fig. 6) with the values of table 1 (C_{ax}=0pF, R_{thx}=43kΩ).
10) The blocking time sets a minimum time span between the end of any fault state and the start of normal operation (remove fault from pin SOx). The value of the blocking time can be adjusted at pin TB. The specified blocking time is valid if TB is connected to GND.
11) This specification guarantees that the drive information will be transferred reliably even at a high DC-link voltage and with ultra-fast switching operations.
12) Undervoltage monitoring of the primary-side supply voltage (VCC to GND). If the voltage drops below this limit, a fault is transmitted to both SOx outputs and the power semiconductors are switched off.
13) Undervoltage monitoring of the secondary-side supply voltage (VISOx to VEx and VEx to COMx which correspond with the approximate turn-on and turn-off gate-emitter voltages). If the corresponding voltage drops below this limit, the IGBT is switched off and a fault is transmitted to the corresponding SOx output.
14) Transmission delay of fault state from the secondary side to the corresponding primary status output.
15) HiPot testing (= dielectric testing) must generally be restricted to suitable components. This gate driver is suited for HiPot testing. Nevertheless, it is strongly recommended to limit the testing time to 1s slots as stipulated by EN 50178. Excessive HiPot testing at voltages much higher than $1200V_{AC(eff)}$ may lead to insulation degradation. No degradation has been observed over 1min. testing at $5000V_{AC(eff)}$. Every production sample shipped to customers has undergone 100% testing at the given value for 1s.
16) Partial discharge measurement is performed in accordance with IEC 60270 and isolation coordination specified in EN 50178. The partial discharge extinction voltage between primary and either secondary side is coordinated for safe isolation to EN 50178. The minimum value given is designed to include appropriate safety margins for long-term ageing. Accelerated ageing tests show virtually no insulation deterioration. Minimum partial discharge extinction voltages remain >2100V even after 2600 slow thermal cycles between –40°C and 125°C and also after 500 thermal shock cycles between –55°C and 150°C.
17) Jitter measurements are performed with input signals INx switching between 0V and 5V referred to GND, with a corresponding rise time and fall time of 15ns.

Legal Disclaimer

This data sheet specifies devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given – either expressly or implicitly – regarding delivery, performance or suitability.

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