2SP0320x2Ax-12
Preliminary Data Sheet

Compact, high-performance, plug-and-play dual-channel IGBT driver based on SCALE™-2 technology for individual and parallel-connected modules in 2-level, 3-level and multilevel converter topologies

Abstract

The SCALE™-2 plug-and-play driver 2SP0320x2Ax-12 is a compact dual-channel intelligent gate driver designed for 1200V IGBT modules from Danfoss, Fuji or Infineon. The driver features an electrical interface (2SP0320T) or a fiber-optic interface (2SP0320V and 2SP0320S) with a built-in DC/DC power supply.

The turn-on and turn-off gate resistors of both channels are not assembled in order to provide maximum flexibility. They must be assembled by the user before start of operation. Please refer to the paragraph on “Gate Resistor Assembly” for the recommended gate resistors.

For drivers adapted to other types of high-power and high-voltage IGBT modules, refer to

www.IGBT-Driver.com/go/plug-and-play

Features

- ✓ Plug-and-play solution
- ✓ Allows parallel connection of IGBT modules
- ✓ For 2-level, 3-level and multilevel topologies
- ✓ Shortens application development time
- ✓ Extremely reliable; long service life
- ✓ Built-in DC/DC power supply
- ✓ 20-pin flat cable interface (2SP0320T)
- ✓ Fiber-optic links (2SP0320V & 2SP0320S)
- ✓ Duty cycle 0... 100%
- ✓ Active clamping of V_{ce} at turn-off
- ✓ IGBT short-circuit protection
- ✓ Monitoring of supply voltage
- ✓ Safe isolation to EN 50178
- ✓ UL compliant
- ✓ Suitable for 1200V IGBT modules
- ✓ Gate resistors not assembled

Applications

- ✓ Wind-power converters
- ✓ Industrial drives
- ✓ UPS
- ✓ Power-factor correctors
- ✓ Traction
- ✓ Railroad power supplies
- ✓ Welding
- ✓ SMPS
- ✓ Radiology and laser technology
- ✓ Research
- ✓ and many others

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Safety Notice!

The data contained in this data sheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory!

Any handling of electronic devices is subject to the general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

Important Product Documentation

This data sheet contains only product-specific data. For a detailed description, must-read application notes and common data that apply to the whole series, please refer to “Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers” (electrical interface) or “Description & Application Manual for 2SP0320V and 2SP0320S SCALE-2 IGBT Drivers” (fiber-optic interface) on www.IGBT-Driver.com/go/2SP0320.

The gate resistors on this gate driver are not assembled in order to provide maximum flexibility. For the gate resistors required for specific IGBT modules, refer to the paragraph on “Gate Resistor Assembly”. Use of gate resistors other than those specified may result in failure.

Mechanical Dimensions

Dimensions: See the relevant “Description and Application Manual”

Mounting principle: Connected to IGBT module with screws

Fiber-Optic Interfaces

Interface	Remarks	Part type #
Drive signal input	2SP0320V, fiber-optic receiver (Notes 21, 22)	HFBR-2522Z
Drive signal input	2SP0320S, fiber-optic receiver (Notes 21, 22)	HFBR-2412Z
Status output	2SP0320V, fiber-optic transmitter (Notes 21, 23)	HFBR-1522Z
Status output	2SP0320S, fiber-optic transmitter (Notes 21, 23)	HFBR-1412Z

Absolute Maximum Ratings

Parameter	Remarks	Min	Max	Unit
Supply voltage V_{DC}	VDC to GND	0	16	V
Supply voltage V_{CC}	VCC to GND (Note 1)	0	16	V
Logic input and output voltages	To GND	-0.5	VCC+0.5	V
SO_x current	Fault condition, total current		20	mA
Gate peak current I_{out}	Note 2	-20	+20	A
Average supply current I_{DC}	2SP0320T (Note 24)		600	mA
Average supply current I_{DC}	2SP0320V and 2SP0320S (Note 24)		690	mA
Output power per gate	Ambient temperature <70°C (Note 3)		3	W
	Ambient temperature 85°C (Note 3)		2	W
Turn-on gate resistance	Note 17	0.3		Ω
Turn-off gate resistance	Note 17	1		Ω
Switching frequency F	Note 29		n.d.	kHz
Test voltage (50Hz/1min.)	Primary to secondary (Note 19)		3800	$V_{AC(eff)}$
	Secondary to secondary (Note 19)		3800	$V_{AC(eff)}$
DC-link voltage	Note 4		800	V
|dV/dt|	Rate of change of input to output voltage (Note 20)		50	kV/µs
Operating voltage	Primary/secondary, secondary/secondary		1200	V_{peak}
Operating temperature		-40	+85	°C
Storage temperature		-40	+90	°C

Recommended Operating Conditions

Power Supply	Remarks	Min	Typ	Max	Unit
Supply voltage V_{DC}	To GND (Note 1)	14.5	15	15.5	V
Supply voltage V_{CC}	To GND (Note 1)	14.5	15	15.5	V
Resistance from TB to GND	2SP0320T, blocking time≠0, ext. value	128		∞	kΩ
SO_x current	Fault condition, 3.3V logic			4	mA

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Electrical Characteristics

Power Supply	Remarks	Min	Typ	Max	Unit
Supply current I_{DC}	2SP0320T, without load		37		mA
	2SP0320V and 2SP0320S, without load		145		mA
Efficiency η	Internal DC/DC converter		85		%
Supply current I_{CC}	Without load		19		mA
Coupling capacitance C_{io}	Primary side to secondary side, total, per channel				
	2SP0320T		20		pF
	2SP0320V and 2SP0320S		15		pF
Power Supply Monitoring	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Supply threshold V_{CC}	Primary side, clear fault	11.9	12.6	13.3	V
	Primary side, set fault (Note 5)	11.3	12.0	12.7	V
Monitoring hysteresis	Primary side, set/clear fault	0.35			V
Supply threshold V_{isox}-V_{eex}	Secondary side, clear fault	12.1	12.6	13.1	V
	Secondary side, set fault (Note 26)	11.5	12.0	12.5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.35			V
Supply threshold V_{eex}-V_{COMx}	Secondary side, clear fault	5	5.15	5.3	V
	Secondary side, set fault (Note 26)	4.7	4.85	5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.15			V
Logic Inputs and Outputs	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Input impedance	2SP0320T, V(INx) > 3V (Note 6)	3.5	4.1	4.6	kΩ
Turn-on threshold	2SP0320T, V(INx) (Note 7)		2.6		V
Turn-off threshold	2SP0320T, V(INx) (Note 7)		1.3		V
SOx output voltage	Fault condition, I(SOx)<8mA			0.7	V
Short-circuit Protection	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Vce-monitoring threshold	Between auxiliary terminals		10.2		V
Response time	DC-link voltage > 550V (Note 8)		6.9		µs
Delay to IGBT turn-off	After the response time (Note 9)		1.4		µs
Blocking time	2SP0320T, after fault (Note 10)		90		ms

Timing Characteristics	Remarks	Min	Typ	Max	Unit
Turn-on delay $t_{d(on)}$	2SP0320T (Note 11)		90		ns
Turn-off delay $t_{d(off)}$	2SP0320T (Note 11)		90		ns
Jitter of turn-on delay	2SP0320T (Note 28)		±2		ns
Jitter of turn-off delay	2SP0320T (Note 28)		±2		ns
Turn-on delay $t_{d(on)}$	2SP0320V and 2SP0320S (Note 12)		120		ns
Turn-off delay $t_{d(off)}$	2SP0320V and 2SP0320S (Note 12)		100		ns
Output rise time $t_{r(out)}$	G_x to E_x (Note 13)		7		ns
Output fall time $t_{f(out)}$	G_x to E_x (Note 13)		25		ns
Dead time between outputs	2SP0320T, half-bridge mode		3		µs
Jitter of dead time	2SP0320T, half-bridge mode		±100		ns
Transmission delay of fault state	2SP0320T (Note 14)		450		ns
Transmission delay of fault state	2SP0320V and 2SP0320S (Note 25)		90		ns
Delay to clear fault state	2SP0320V and 2SP0320S (Note 15)		11		µs
Acknowledge delay time	2SP0320V and 2SP0320S (Note 16)		220		ns
Acknowledge pulse width	2SP0320V and 2SP0320S (on host side)		700	1050	ns

Outputs	Remarks	Min	Typ	Max	Unit
Turn-on gate resistor $R_{g(on)}$	Note 17		not assembled		Ω
Turn-off gate resistor $R_{g(off)}$	Note 17		not assembled		Ω
Gate voltage at turn-on			15		V
Gate-voltage at turn-off	2SP0320T / (2SP0320V & 2SP0320S)				
	P = 0W		-10.4/-9.9		V
	P = 0.3W		-10.2/-9.8		V
	P = 2.1W		-9.7/-9.5		V
	P = 3W		-9.6/-9.4		V
Gate resistance to COMx			4.7		kΩ

dV/dt Feedback	Remarks	Implementation
dV/dt feedback	Note 18	No

Electrical Isolation	Remarks	Min	Typ	Max	Unit
Test voltage (50Hz/1s)	Primary to secondary side (Note 19)	3800	3850	3900	V_{eff}
	Secondary to secondary side (Note 19)	3800	3850	3900	V_{eff}
Partial discharge extinction volt.	Primary to secondary side (Note 27)	1220			V_{peak}
	Secondary to secondary side (Note 27)	1200			V_{peak}
Creepage distance	Primary to secondary side	20			mm
	Secondary to secondary side	17			mm

All data refer to +25°C and V_{CC} = V_{DC} = 15V unless otherwise specified

Footnotes to the Key Data

1) Both supply voltages V_{DC} and V_{CC} should be applied in parallel.
2) The gate current is limited by the gate resistors located on the driver.
3) If the specified value is exceeded, this indicates a driver overload. It should be noted that the driver is not protected against overload. From 70°C to 85°C, the maximum permissible output power can be linearly interpolated from the given data.
4) This limit is due to active clamping. Refer to “Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers” (electrical interface) or “Description & Application Manual for 2SP0320V and 2SP0320S SCALE-2 IGBT Drivers” (fiber-optic interface).
5) Undervoltage monitoring of the primary-side supply voltage (VCC to GND). If the voltage drops below this limit, a fault is transmitted to the corresponding output(s) (2SP0320T/2SP0320V/2SP0320S) and the IGBTs are switched off (only 2SP0320T).
6) The input impedance can be modified to values < 18 kΩ (customer-specific solution).
7) Turn-on and turn-off threshold values can be increased (customer-specific solution).
8) The resulting pulse width of the direct output of the gate drive unit for short-circuit type I (excluding the delay of the gate resistors) is the sum of response time plus delay to IGBT turn-off.
9) The turn-off event of the IGBT is delayed by the specified time after the response time.
10) Factory set value. The blocking time can be reduced with an external resistor. Refer to “Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers”.
11) Measured from the transition of the turn-on or turn-off command at the driver input to direct output of the gate drive unit (excluding the delay of the gate resistors).
12) Including the delay of the external fiber-optic links. Measured from the transition of the turn-on or turn-off command at the optical transmitter on the host controller side to the direct output of the gate drive unit (excluding the delay of the gate resistors).
13) Refers to the direct output of the gate drive unit (excluding the delay of the gate resistors).
14) Transmission delay of the fault state from the secondary side to the primary status outputs.
15) Measured on the host side. The fault status on the secondary side is automatically reset after the specified time.
16) Including the delay of the external fiber-optic links. Measured from the transition of the turn-on or turn-off command at the optical transmitter on the host controller side to the transition of the acknowledge signal at the optical receiver on the host controller side.
17) The gate resistors are not assembled on this IGBT gate driver. They must be assembled by the user according to the paragraph on “Gate Resistor Assembly”.
18) A dV/dt feedback can optionally be implemented in order to reduce the rate of rise of the collector emitter voltage of the IGBTs at turn-off (customer-specific solution).
19) HiPot testing (= dielectric testing) must generally be restricted to suitable components. This gate driver is suited for HiPot testing. Nevertheless, it is strongly recommended to limit the testing time to 1s slots as stipulated by EN 50178. Excessive HiPot testing at voltages much higher than $850V_{AC(eff)}$ may lead to insulation degradation. No degradation has been observed over 1min. testing at $3800V_{AC(eff)}$. Every production sample shipped to customers has undergone 100% testing at the given value or higher ($<5100V_{eff}$) for 1s.
20) This specification guarantees that the drive information will be transferred reliably even at a high DC-link voltage and with ultra-fast switching operations.
21) The transceivers required on the host controller side are not supplied with the gate driver. It is recommended to use the same types as used in the gate driver. For product information refer to www.IGBT-Driver.com/go/fiberoptics
22) The recommended transmitter current at the host controller is 20mA. A higher current may increase jitter or delay at turn-off.
23) The typical transmitter current at the gate driver is 18mA. In case of supply undervoltage, the minimum transmitter current at the gate driver is 12mA: this is suitable for adequate plastic optical fibers with a length of more than 10 meters.
24) If the specified value is exceeded, this indicates a driver overload. It should be noted that the driver is not protected against overload.

25) Delay of external fiber-optic links. Measured from the driver secondary side (ASIC output) to the optical receiver on the host controller.
26) Undervoltage monitoring of the secondary-side supply voltage (Visox to Veex and Veex to COMx which correspond with the approximate turn-on and turn-off gate-emitter voltages). If the corresponding voltage drops below this limit, the IGBT is switched off and a fault is transmitted to the corresponding output.
27) Partial discharge measurement is performed in accordance with IEC 60270 and isolation coordination specified in EN 50178. The partial discharge extinction voltage between primary and either secondary side is coordinated for safe isolation to EN 50178.
28) Jitter measurements are performed with input signals INx switching between 0V and 15V referred to GND, with a corresponding rise time and fall time of 8ns.
29) The maximum switching frequency is not defined, as it depends on the IGBT module used. Please consult the corresponding driver data sheet for more information.

Gate Resistor Assembly

The turn-on and turn-off gate resistors of 2SP0320x2Ax drivers are adapted to their respective IGBT modules. Recommended gate resistors are: PR02 / 2W / 5% from Vishay.

The following versions exist:

1200V IGBT Type	R120/R121/ R220/R221	R122/R123 / R222/R223	Resulting Rg,on	Resulting Rg,off
FF450R12IE4	5.1Ω	6.8Ω	2.55Ω	3.4Ω
FF600R12IE4	3.6Ω	6.8Ω	1.8Ω	3.4Ω
2MBI900VXA-120E-50	3.3Ω	5.1Ω	1.65Ω	2.55Ω
2MBI900VXA-120P-50	4.3Ω	3.3Ω	2.15Ω	1.65Ω
FF900R12IE4	2.7Ω	6.8Ω	1.35Ω	3.4Ω
FF900R12IP4	3.3Ω	6.8Ω	1.65Ω	3.4Ω
2MBI1400VXB-120E-50	2Ω	3Ω	1Ω	1.5Ω
2MBI1400VXB-120P-50	3.3Ω	3.3Ω	1.65Ω	1.65Ω
DP1400B1200T103714	2Ω	4.7Ω	1Ω	2.35Ω
FF1400R12IP4	2Ω	6.8Ω	1Ω	3.4Ω

For the component position, refer to Fig. 1.

Assembly Drawing

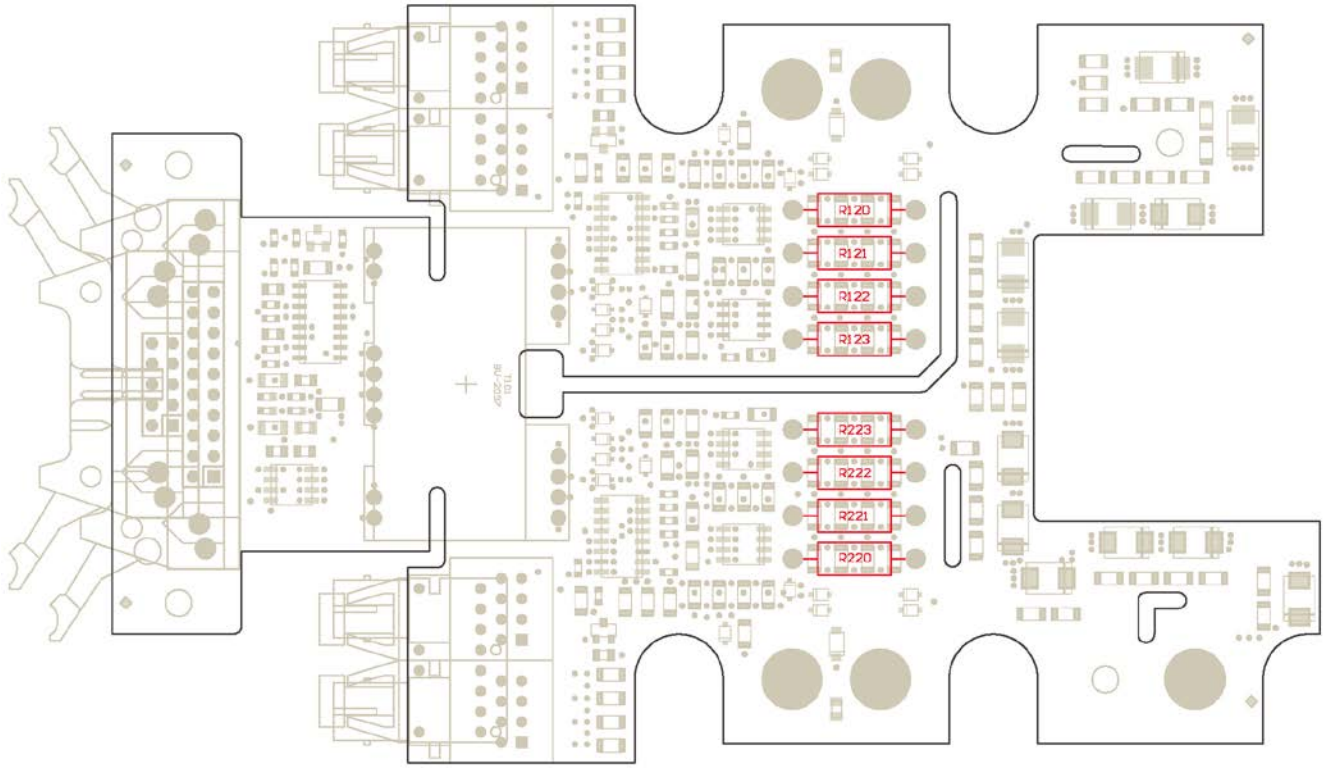

Fig. 1: Assembly drawing of 2SP0320 with highlighted gate resistors

Note that the wires of the gate resistors should not project more than 1.6mm after soldering (excess length at bottom side). Furthermore, a minimum distance of 1mm must be maintained between the gate resistor body and the PCB.

Legal Disclaimer

This data sheet specifies devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given – either expressly or implicitly – regarding delivery, performance or suitability.

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