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JTAG-HS2™ Programming Cable for Xilinx® FPGAs

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This manual applies to the HTAG-HS2 rev. A

Overview

The Joint Test Action Group (JTAG)-HS2 programming cable is a high-speed programming solution for Xilinx field-programmable gate arrays (FPGAs). The cable is fully compatible will all Xilinx tools and can be seamlessly driven from iMPACT, Chipscope™, and EDK. The HS2 attaches to target boards using Digilent's 6-pin, 100-mil spaced programming header or Xilinx's 2×7, 2mm connector and the included adaptor.

The PC powers the JTAG-HS2 through the USB port and will recognize it as a Digilent programming cable when connected to a PC, even if the cable is not attached to the target board. The HS2 has a separate Vdd pin to supply the JTAG signal buffers. The high speed 24mA three-state buffers allow target boards to drive the HS2 with signal voltages from 1.8V to 5V and bus speeds of up to 30MBit/sec. To function correctly, the HS2's Vdd pin must be tied to the same voltage supply that drives the JTAG port on the FPGA (see Fig. 1).

The JTAG bus can be shared with other devices as systems hold JTAG signals at high-impedance except when actively driven during programming. The HS2 comes with a standard Type-A to Micro-USB cable that attaches to the end of the module opposite the system board connector. The system board connector should hold the small and light HS2 firmly in place (see Fig. 2).

The JTAG-HS2.

Features include:

- Small, complete, all-in-one JTAG programming solution for Xilinx FPGAs
- Compatible with all Xilinx tools
- Compatible with IEEE 1149.7-2009 Class T0 - Class T4 (includes 2-Wire JTAG)
- Separate Vref drives JTAG/SPI signal voltages; Vref can be any voltage between 1.8V and 5V.
- High-Speed USB2 port that can drive JTAG/SPI bus at up to 30Mbit/sec
- JTAG/SPI frequency settable by user
- Uses micro-AB USB2 connector
- SPI programming solution (modes 0 and 2 up to 30Mbit/sec, modes 1 and 3 up to 2Mbit/sec)
- Fully supported by the Adept SDK, allowing custom JTAG/SPI applications to be created

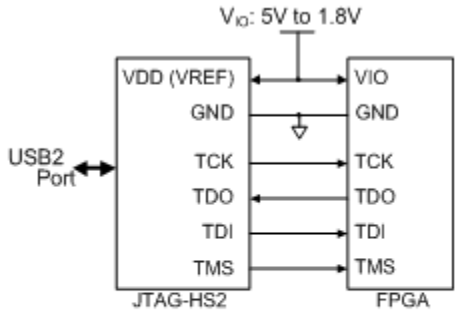

Figure 1. Diagram of signal voltages and connections.

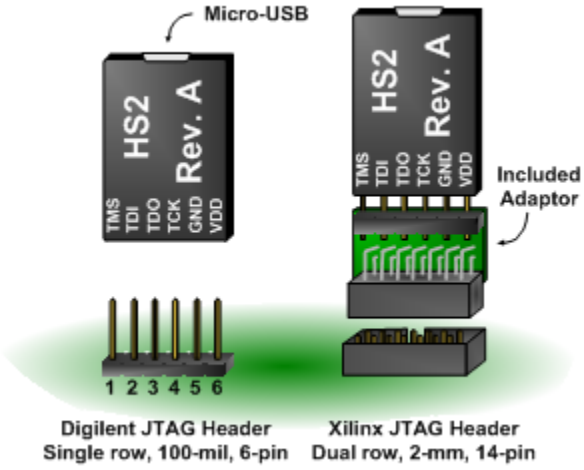

Figure 2. Xilinx JTAG headers.

In addition to supporting JTAG, the JTAG-HS2 also features two highly configurable serial peripheral interface (SPI) ports that allow communication with virtually any SPI peripheral. Both SPI ports share the same pins and only one port may be enabled at any given time (see Fig. 3). Table 1 summarizes the features supported by each port. The HS2 supports SPI modes 0, 1, 2, and 3.

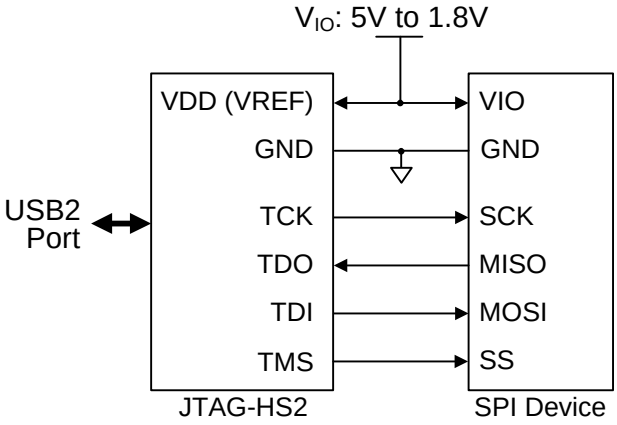

Figure 3. JTAG-HS2 SPI Device Connections.

Port Number	SPI Mode	Shift LSB First	Shift MSB First	Selectable SCK Frequency	Max SCK Frequency	Min SCK Frequency	Inter-byte Delay
0	0	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
	2	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
1	0	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
	1	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
	2	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
	3	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS

Table 1. Features supported by each port.

1 Software Support

In addition to working seamlessly with all Xilinx tools, Digilent's Adept software and the Adept software development kit (SDK) support the HS2 cable. For added convenience, customers may freely downloaded the SDK from Digilent's website. This Adept software includes a full-featured programming environment and a set of public application programming interfaces (API) that allow user applications to directly drive the JTAG chain.

With the Adept SDK, users can create custom applications that will drive JTAG ports on virtually any device. Users may utilize the APIs provided by the SDK to create applications that can drive any SPI device supporting those modes. Please see the Adept SDK reference manual for more information.

Digilent's AVR programmer also supports the HS2 and the cable can be used to program any AVR device.

2 IEEE 1149.7-2009 Compatibility

The JTAG-HS2 supports several scan formats including; the JScan0-JScan3, MScan, and OScan0 - OScan7. It is capable of communicating in 4-wire and 2-wire scan chains that consist of Class T0 – T4 JTAG Target Systems (TS). (See Figs. 4 & 5).

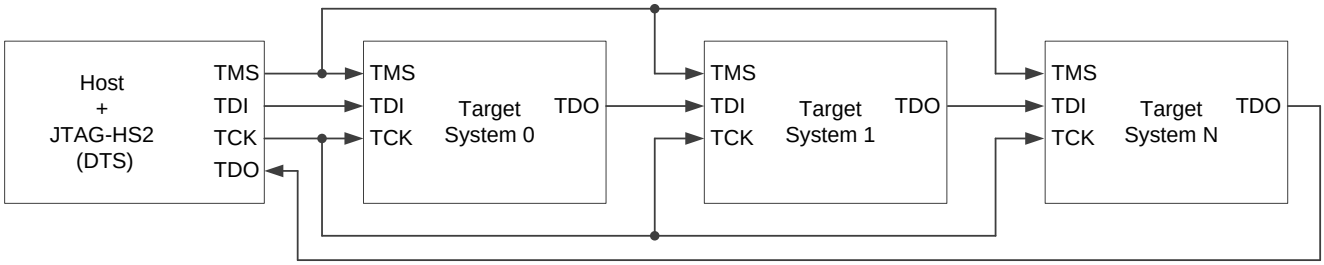

Figure 4. 4-wire series topology.

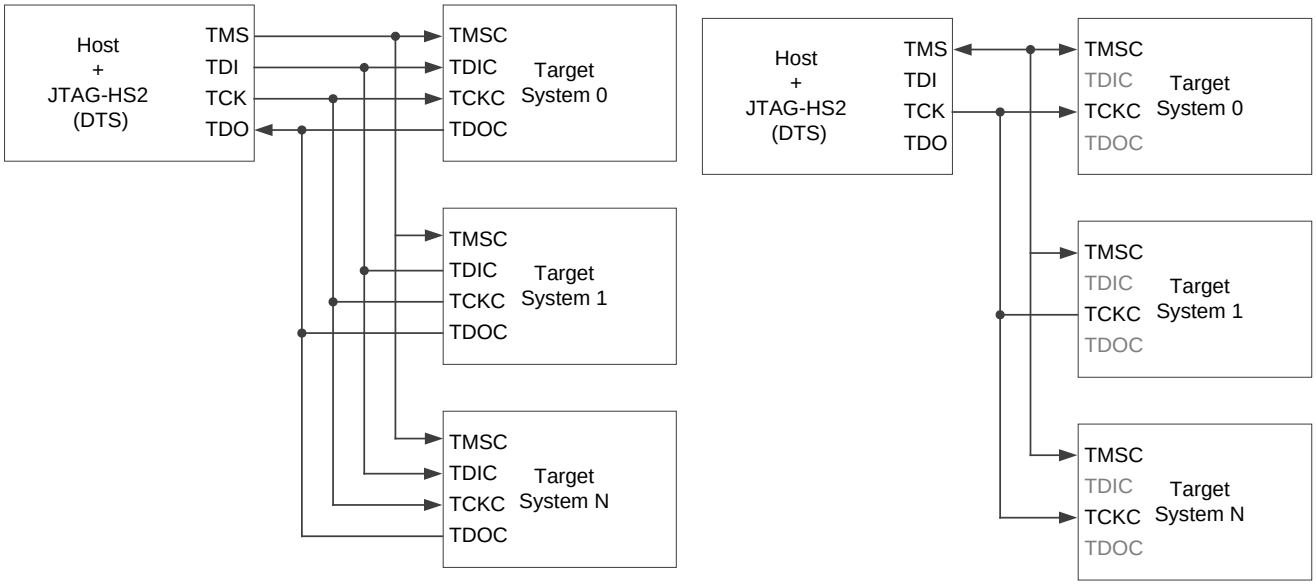

Figure 5. 4-Wire star topology (left), 2-Wire star topology (right).

The Adept SKD provides an example application that demonstrates how to communicate with a class T4 TAP controller using the MScan, OScan0, and OScan1 scan formats.

3 Design Notes

The JTAG-HS2 uses high speed three-state buffers to drive the TMS, TDI, and TCK signals. These buffers are capable of sourcing or sinking a maximum of 50 mA of current. The HS2 has 100 ohm resistors between the output of the buffers and the I/O pins to ensure the cable does not exceed the maximum limit. To further limit short circuit current, additional resistance may be placed in series with the I/O pins of the HS2 and the target board. However, Digilent recommends limiting the amount of additional resistance to 100 ohms or less as higher resistance may result in degraded operation.

When the JTAG-HS2 first receives power, the three-state buffers attached to the TMS, TDI, and TCK signals move into a high-impedance state. They remain in the high-impedance state until an application enables the HS2's JTAG or SPI port. Once these ports activate, the buffers actively drive the TMS, TDI, and TCK signals until the port is disabled.

The IEEE 1149.7-2009 specification requires any device that functions as a debug and test system (DTS) to provide a pull-up bias on the TMS and TDO pins. In order to meet this requirement, the JTAG-HS2 features weak pull-ups (100K ohm) on the TMS, TDI, TDO, and TCK signals. While not strictly required, the pull-ups on the TDI and TCK signals ensure that neither signal floats while another source is not actively driving them.

The JTAG-HS2 can interface scan chains that consist of one or more IEEE 1149-7 compatible Target Systems (TS). The devices in these chains communicate using the TMS, TDI, TDO, and TCK signals or they may communicate using only the TMS and TCK signals. Communication using only the TMS and TCK signals requires both the HS2 and TS to drive the TMS pin. The current scan format, bit period, and the level of the TCK pin determine which device is allowed to drive the TMS pin.

A drive conflict may occur when the HS2 and TS disagree on the current scan format setting or bit period. In the event that a drive conflict occurs, the 100 ohm resistor between the TMS buffer and output pin will limit the maximum current to 50 mA to prevent any damage from occurring to the JTAG-HS2. The drive conflict may be resolved by having the JTAG-HS2 perform a reset escape, which will reset the scan format of the TS to JScan0/JScan1. If the TMS pin of the TS is not capable of sourcing or sinking VDD (VREF) ÷ 100 amps of current then an additional resistor should be placed in series with the TMS pin of the TS to further limit current flow.

In most cases a drive conflict can be avoided by having applications that use the HS2 communicate with the TS in two-wire mode. Use the applications to reconfigure the TS to use the JScan0, JScan1, JScan2, or JScan3 scan format prior to disabling the HS2's JTAG port.

4 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
VDD (VREF)	I/O reference/supply voltage		-0.5	6	V
VIO	Signal Voltage		-0.5	6	V
I_{IK},I_{OK}	TMS, TCK, TDI, TDO DC Input/Output Diode Current	VIO < -0.5V		-50	mA
		VIO > 6V		+20	
I_{OUT}	DC Output Current			±50	mA
T_{STG}	Storage Temperature		-20	+120	ºC
ESD	Human Body Model JESD22-A114			4000	V
	Charge Device Model JESD22-C101			2000	V

5 DC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDD (VREF)	I/O reference/supply voltage	1.65	2.5/3.3	5.5	Volts
TDO	Input High Voltage (V_{IH})	1.62		5.5	Volts
	Input Low Voltage (V_{IL})	0		0.65	Volts
TMS, TCK, TDI	Output High (V_{OH})	0.85 x Vdd	0.95 x Vdd	Vdd	Volts
	Output Low (V_{OL})	0	0.05 x Vdd	0.15 x Vdd	Volts

6 AC Operating Characteristics

The JTAG-HS2 JTAG signals and SPI operate according to the timing diagram in Fig. 6. The HS2 supports TCK frequencies from 30 MHz to 8 KHz at integer divisions of 30 MHz from 1 to 3750. Common frequencies include 30 MHz, 15 MHz, 10 MHz, 7.5 MHz, and 6 MHz (see Table 2).

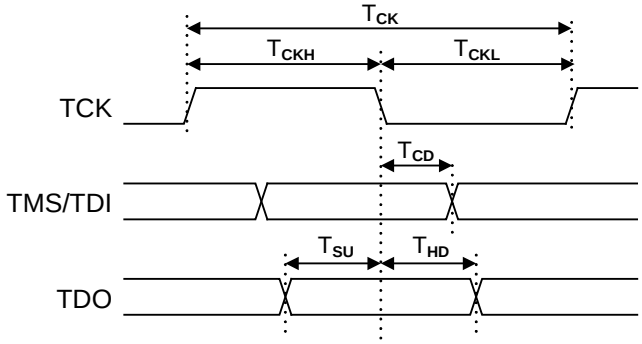

Figure 6. Timing diagram.

Symbol	Parameter	Min	Max
T_{CK}	T_{CK} period	33.3ns	125µs
T_{CKH}, T_{CKL}	T_{CLK} pulse width	16.6ns	62.5µs
T_{CD}	T_{CLK} to TMS, TDI	0	15ns
T_{SU}	TDO Setup time	19ns	
T_{HD}	TDO Hold time	0	

Table 2.Common frequencies.