

551S

Low Skew 1 to 4 Clock Buffer

The 551S is a low cost, high-speed single input to four output clock buffer with best in class additive phase jitter of sub 50fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact Renesas for all of your clocking needs.

Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-SOIC, 8-TSSOP and 8-DFN
- Input/output clock frequency up to 200MHz
- Non-inverting output clock
- Ideal for networking clocks
- Operating voltages: 1.8V to 3.3V
- Output Enable mode tri-states outputs
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)

Block Diagram

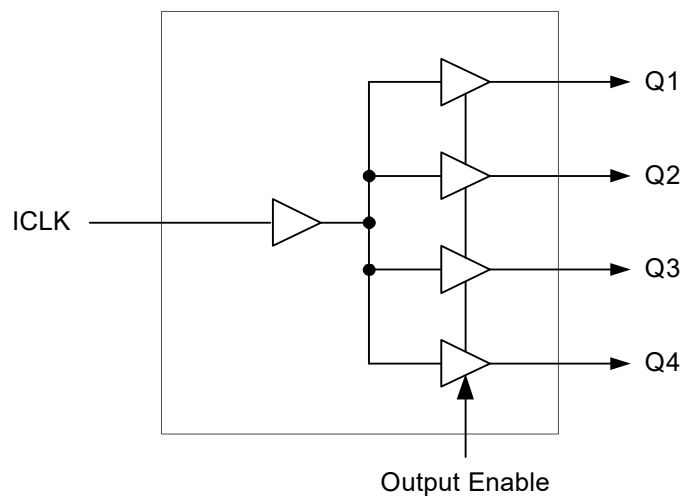


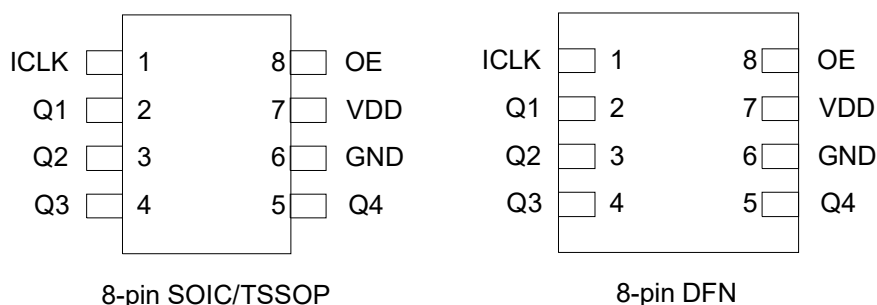
Figure 1. Block Diagram

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1. Pin Information

1.1 Pin Assignments



1.2 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	ICLK	Input	Clock input. Internal pull-up resistor.
2	Q1	Output	Clock output 1.
3	Q2	Output	Clock output 2.
4	Q3	Output	Clock output 3.
5	Q4	Output	Clock output 4.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect +1.8V, +2.5V or +3.3V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.

1.3 External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Rating
Supply Voltage, VDD	3.465V
All Inputs and Outputs	-0.5 V to 3.465V
Ambient Operating Temperature, Extended	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature, extended	-40	+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71	+3.465	V

2.3 Thermal Specifications

Parameter	Symbol	Conditions	Typical	Units
Thermal Resistance Junction to Ambient	Θ_{JA}	Still air	150	°C/W
		1m/s air flow	140	
		3m/s air flow	120	
Thermal Resistance Junction to Board	Θ_{JB}		89	
Thermal Resistance Junction to Case	Θ_{JC}		40	

2.4 Electrical Specifications

2.4.1 DC Electrical Characteristics

VDD = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD		1.89	V
Input Low Voltage, ICLK	V _{IL}	[1]			0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V _{IL}				0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -10mA	1.3			V
Output Low Voltage	V _{OL}	I _{OL} = 10mA			0.35	V
Operating Supply Current	IDD	No load, 135MHz		13		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	OE pin		5		pF

1. Nominal switching threshold is VDD/2.

VDD = 2.5V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD		2.625	V
Input Low Voltage, ICLK	V _{IL}	[1]			0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V _{IL}				0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -16mA	1.8			V
Output Low Voltage	V _{OL}	I _{OL} = 16mA			0.5	V
Operating Supply Current	IDD	No load, 135MHz		18		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	OE pin		5		pF

1. Nominal switching threshold is VDD/2.

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD		3.465	V
Input Low Voltage, ICLK	V _{IL}	[1]			0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD		VDD	V
Input Low Voltage, OE	V _{IL}				0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -25mA	2.2			V
Output Low Voltage	V _{OL}	I _{OL} = 25mA			0.7	V

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Supply Current	IDD	No load, 135MHz		22		mA
Nominal Output Impedance	Z _O			17		Ω
Input Capacitance	C _{IN}	OE pin		5		pF

1. Nominal switching threshold is VDD/2.

2.4.2 AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequency		5pF load [1]			200	MHz
Output Clock Rise Time	t _{OR}	0.36 to 1.44V		0.6	1.0	ns
Output Clock Fall Time	t _{OF}	1.44 to 0.36V		0.6	1.0	ns
Propagation Delay		135MHz [2]	1.5	2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration range: 12kHz–20MHz		0.03	0.05	ps
Output to Output Skew		Rising edges at VDD/2 [3]		50	65	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Output Enable Time	t _{EN}	CL ≤ 5pF			3	cycles
Output Disable Time	t _{DIS}	CL ≤ 5pF			3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

VDD = 2.5V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequency		5pF load [1]			200	MHz
Output Clock Rise Time	t _{OR}	0.36 to 1.44V		0.6	1.0	ns
Output Clock Fall Time	t _{OF}	1.44 to 0.36V		0.6	1.0	ns
Propagation Delay		135MHz [2]	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration range: 12kHz–20MHz		0.035	0.05	ps
Output to Output Skew		Rising edges at VDD/2 [3]		50	65	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Output Enable Time	t _{EN}	CL ≤ 5pF			3	cycles
Output Disable Time	t _{DIS}	CL ≤ 5pF			3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Clock Rise Time	t _{OR}	5pF load [1]			200	MHz
Output Clock Fall Time	t _{OF}	0.66 to 2.64V		0.6	1.0	ns
Propagation Delay		2.64 to 0.66V		0.6	1.0	ns
Buffer Additive Phase Jitter, RMS		135MHz [2]	1.5	2	4	ns
Output to Output Skew		125MHz, Integration range: 12kHz–20MHz		0.037	0.05	ps
Start-up Time	t _{START-UP}	Rising edges at VDD/2 [3]		50	65	ps
Output Enable Time	t _{EN}	Part start-up time for valid outputs after VDD ramp-up			2	ms
Output Disable Time	t _{DIS}	CL ≤ 5pF			3	cycles
Output Clock Rise Time	t _{OR}	CL ≤ 5pF			3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.
4. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

2.5 Phase Noise Plots

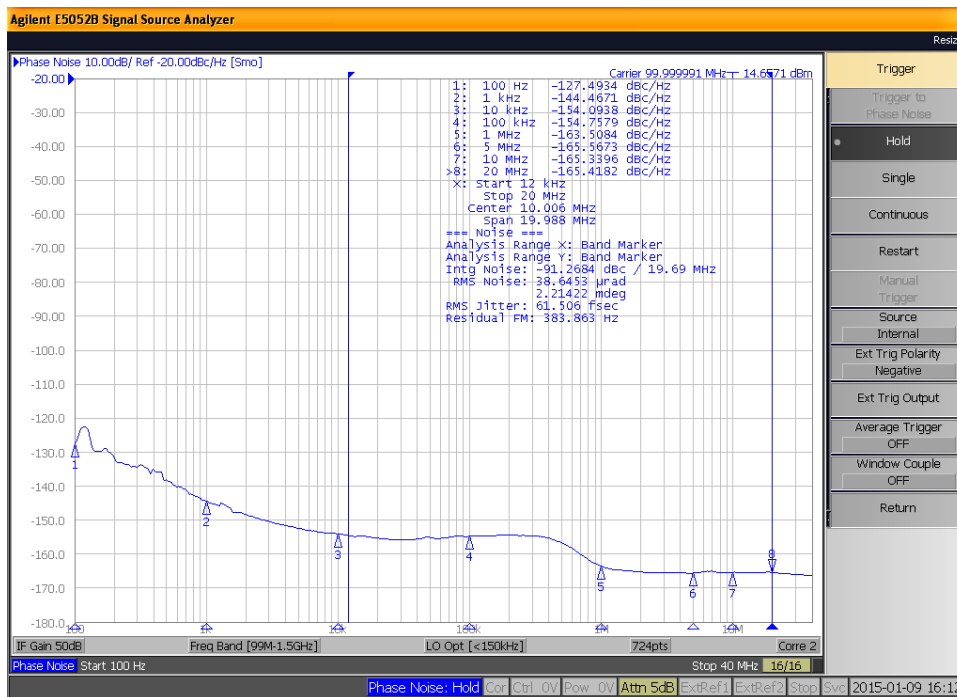


Figure 2. 551S Reference Phase Noise 62fs (12kHz to 20MHz)

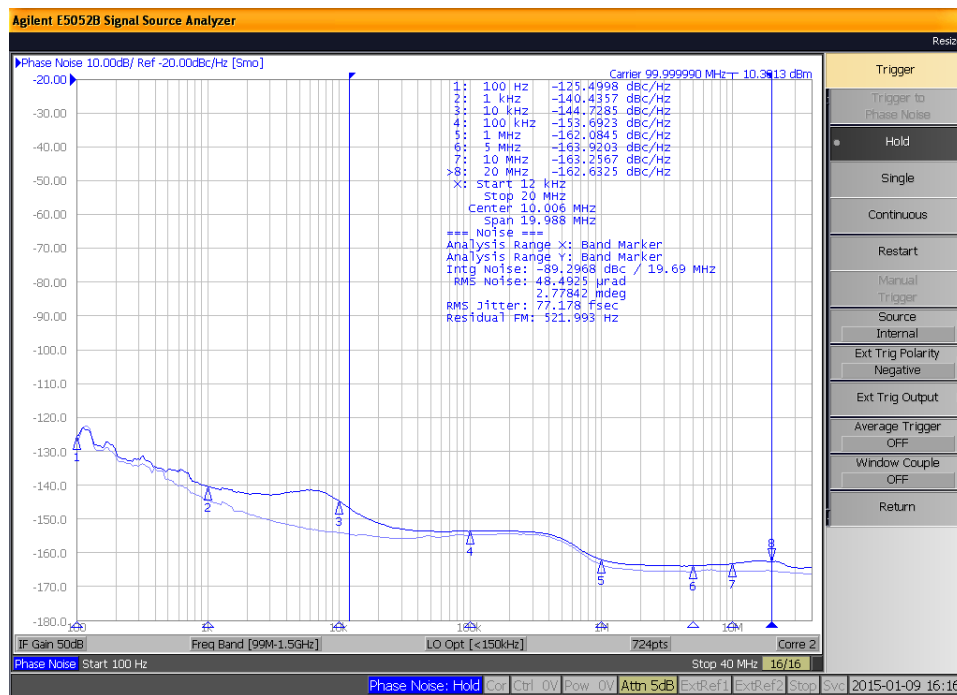
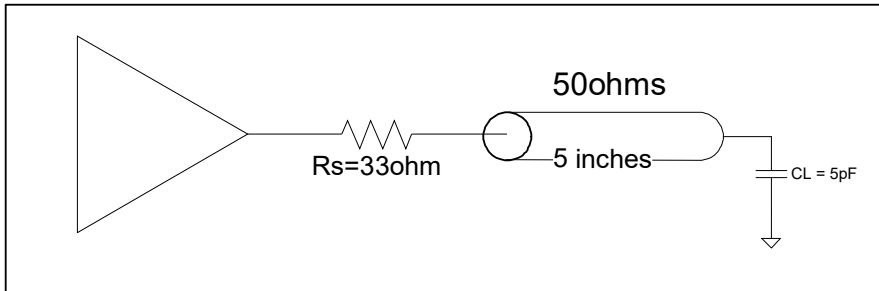


Figure 3. 551S Output Phase Noise 77fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 551S high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 62fs of RMS phase jitter while the output has about 77fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 45fs.

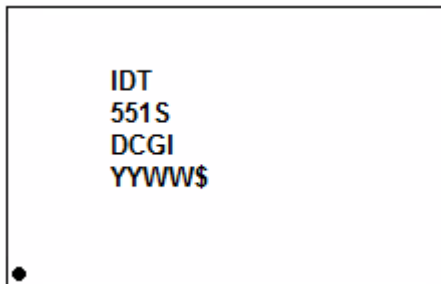
2.6 Test Load and Circuit



3. Package Outline Drawings

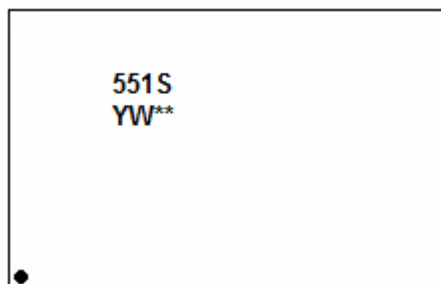
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for package links). The package information is the most current data available and is subject to change without revision of this document.

4. Marking Diagrams



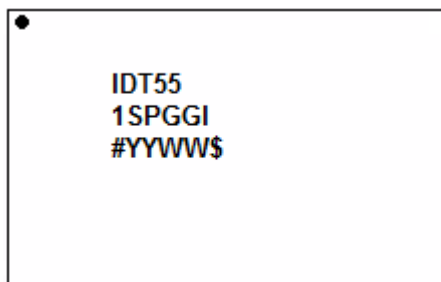
8-SOIC

- Lines 1, 2, and 3: part number.
- Line 4:
 - “YYWW” are the last digits of the year and week that the part was assembled.
 - “\$” denotes the mark code.



8-DFN

- Line 1: truncated part number.
- Line 2:
 - “YW” are the last digit of the year and week that the part was assembled.
 - “**” denotes the lot sequence.



8-TSSOP

- Lines 1 and 2: part number.
- Line 3:
 - “#” denotes the stepping number.
 - “YYWW” are the last digits of the year and week that the part was assembled.
 - “\$” denotes the mark code.

5. Ordering Information

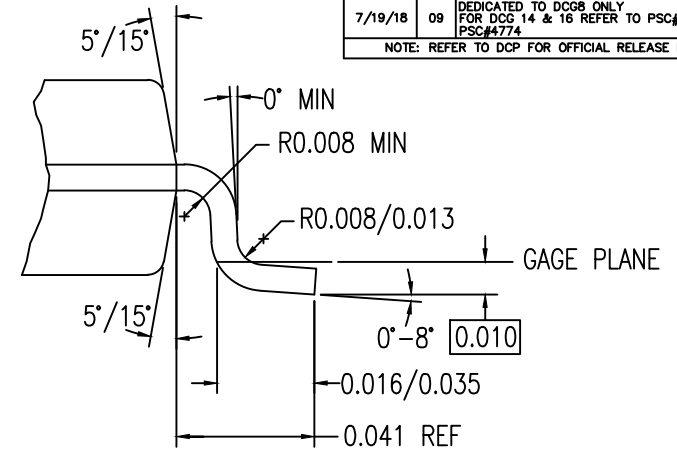
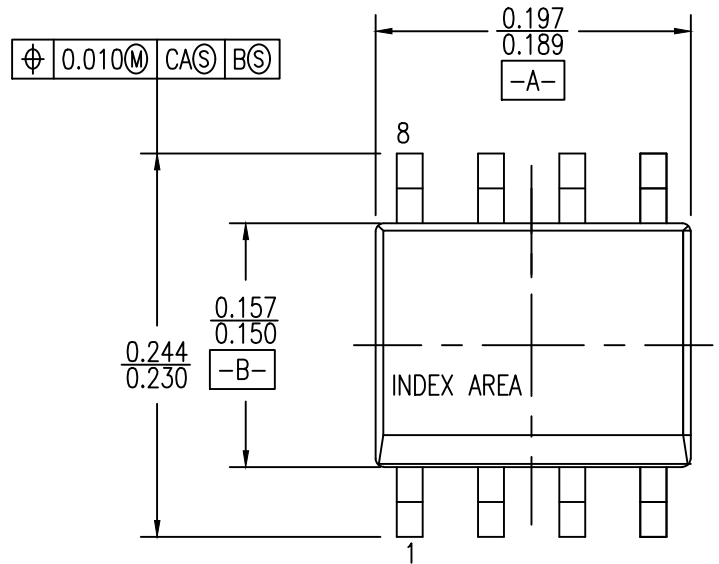
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551SDCGI8		Tape and Reel	
551SCMGI	8-DFN, 2.0 × 2.0 × 0.5 mm	Cut Tape	
551SCMGI8		Tape and Reel	
551SPGGI	8-TSSOP, 4.4 × 3.0 mm	Tubes	
551SPGGI8		Tape and Reel	

6. Revision History

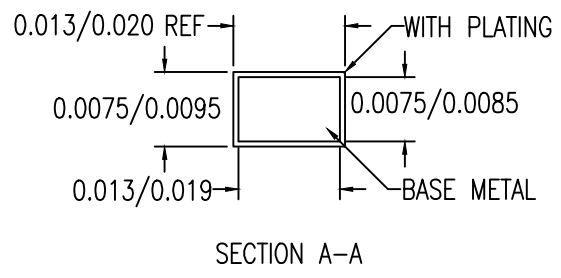
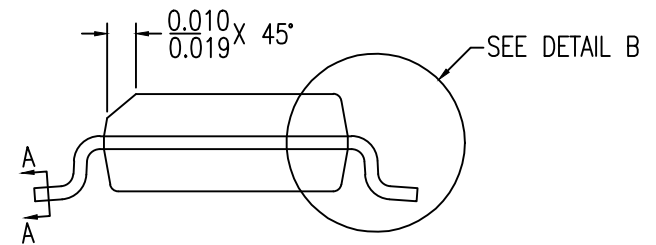
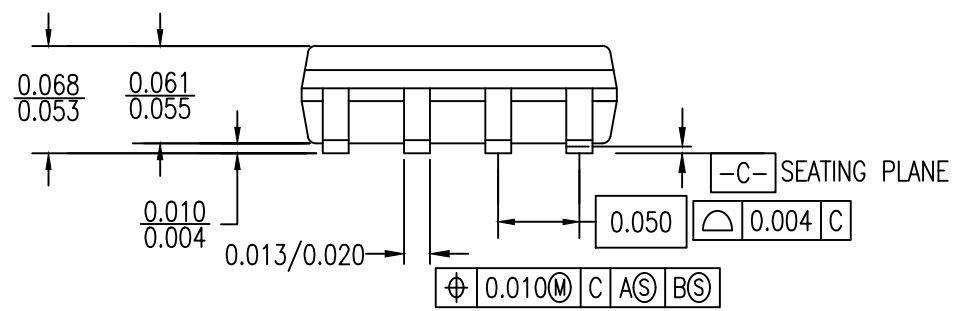
Revision	Date	Description
1.3	Mar 12, 2021	<ul style="list-style-type: none"> ▪ Added 8-TSSOP package information. ▪ Reformatted datasheet to latest template.
1.2	Sep 20, 2018	<ul style="list-style-type: none"> ▪ Added Thermal Resistance Junction to Board to Thermal Characteristics table. ▪ Updated Package Outline Drawings section.
1.0	Mar 18, 2015	Initial release.

DATE		REVISIONS		
CREATED	REV	DESCRIPTION	AUTHOR	
07/10/99	02	ADD 8 LD	T. VU	
05/23/01	03	ADDED TOPMARK TO TITLE	PKP	
09/05/02	04	CORRECTED X DIM	PKP	
10/12/04	05	ADD "GREEN" DCG NOMENCLATURE	TU VU	
12/12/12	06	ADD PACKAGE CODE	RC	
4/8/14	07	MODIFY NOTE "9"	RC	
5/22/14	08	UPDATE "L" TO .016/.035	CM	
7/19/18	09	DEDICATED TO DCG8 ONLY FOR DCG 14 & 16 REFER TO PSC#4773 PSC#4774	RC	

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE



DETAIL B

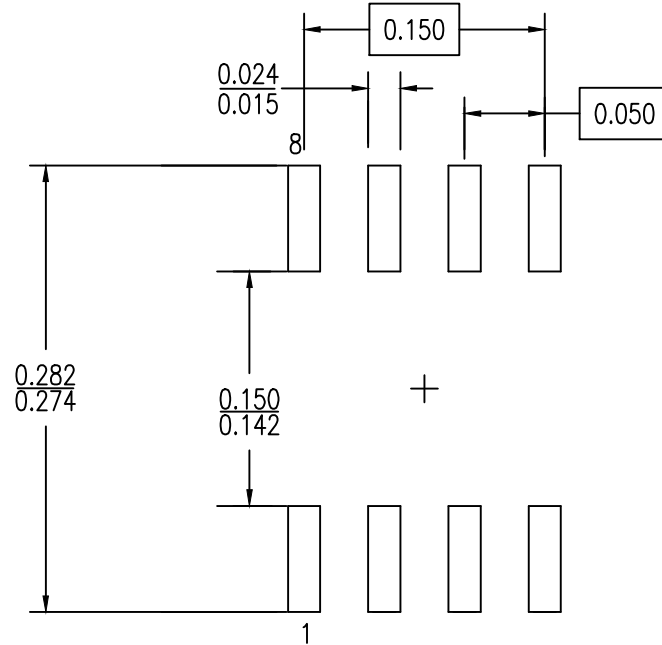


- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
 2. ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± ± XXXX± ±		6024 SILVERCREEK VALLEY RD
		SAN JOSE CA 95138
		PHONE: (408) 284-8200
		FAX: (408) 284-8591
www.IDT.com		
TITLE DCG8 Package Outline Drawing 0.150" Body Width 0.050" Pitch SOIC		
SIZE C	DRAWING No. PSC-4068	REV 09
DO NOT SCALE DRAWING		SHEET 1 OF 2

DATE CREATED		REVISIONS		
REV	DESCRIPTION	AUTHOR		
02	ADD 8 LD	T. VU		
03	ADDED TOPMARK TO TITLE	PKP		
04	CORRECTED X DIM	PKP		
05	ADD "GREEN" DCG NOMENCLATURE	TU VU		
06	ADD PACKAGE CODE	RC		
07	MODIFY NOTE "9"	RC		
08	UPDATE "L" TO .016/.035	CM		
09	DEDICATED TO DCG8 ONLY FOR DCG 14 & 16 REFER TO PSC#4773 PSC#4774	RC		


NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE



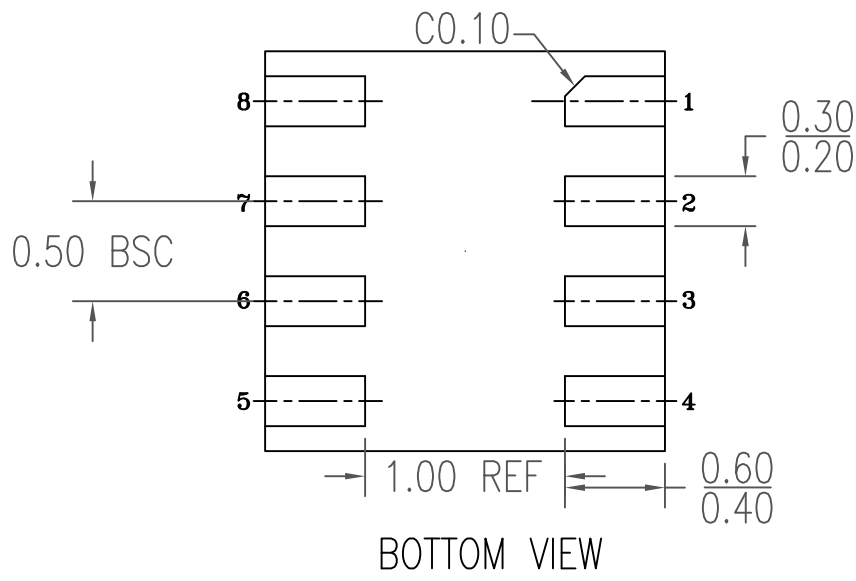
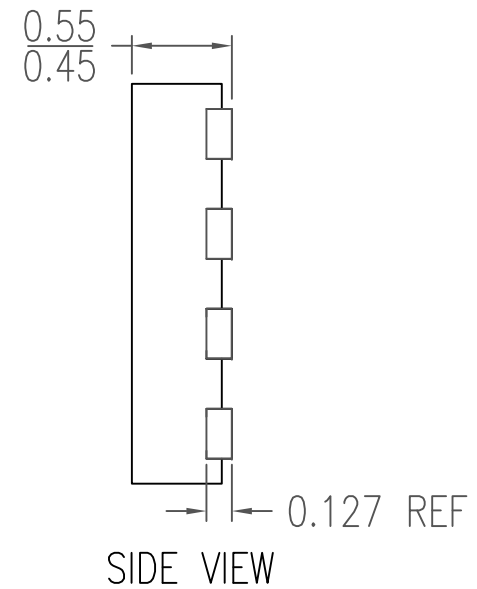
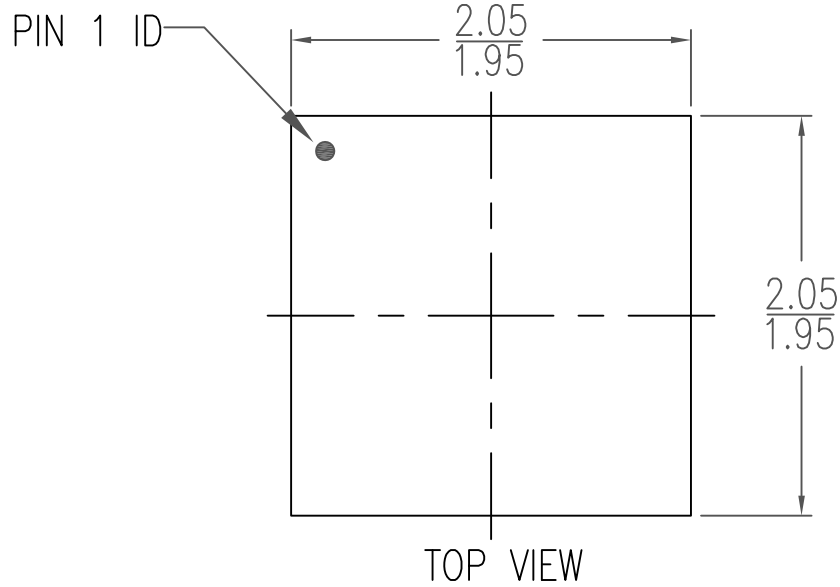
RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS SPECIFIED		 6024 SILVERCREEK VALLEY RD SAN JOSE CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com	
DECIMAL	ANGULAR	TITLE DCG8 Package Outline Drawing 0.150" Body Width 0.050" Pitch SOIC	
XX±	±	SIZE	REV
XXX±		C	09
XXXX±		DO NOT SCALE DRAWING	
		SHEET 2 OF 2	

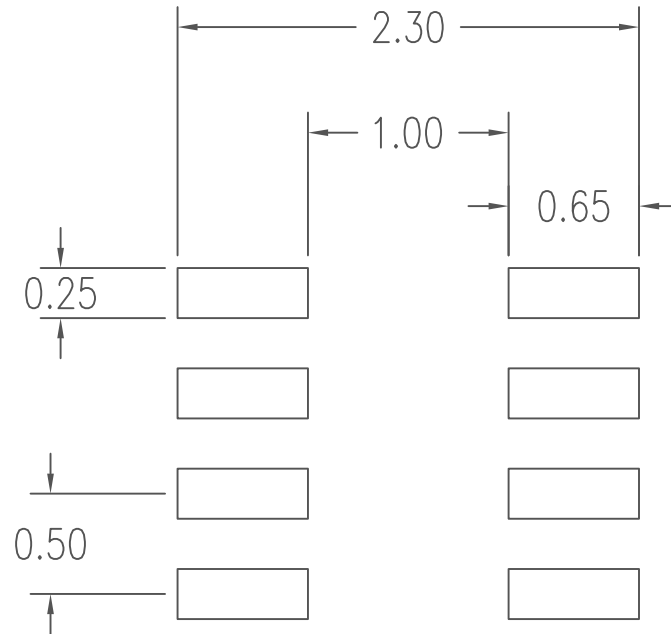
REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
09/18/14	00	INITIAL RELEASE	J.HUA
4/5/18	01	CHANGE VFQFN to DFN	R.C
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
 2. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± ± XXXX± ±	IDT 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674 www.IDT.com	
		TITLE CMC8 Package Outline Drawing 2.0 x 2.0 x 0.5 mm Body 0.5mm Pitch DFN
SIZE C	DRAWING No. PSC-4490	REV 01
DO NOT SCALE DRAWING		SHEET 1 OF 2


REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
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4/5/18	01	CHANGE VQFN to DFN	R.C
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



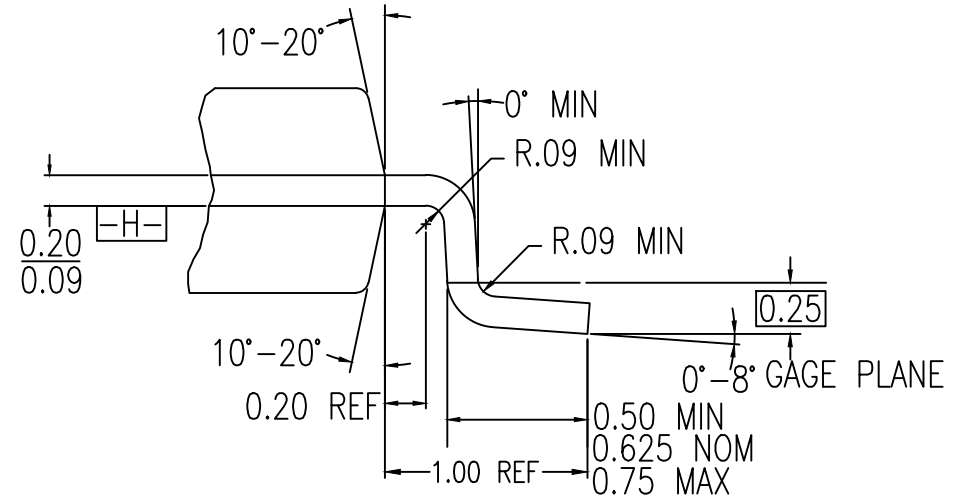
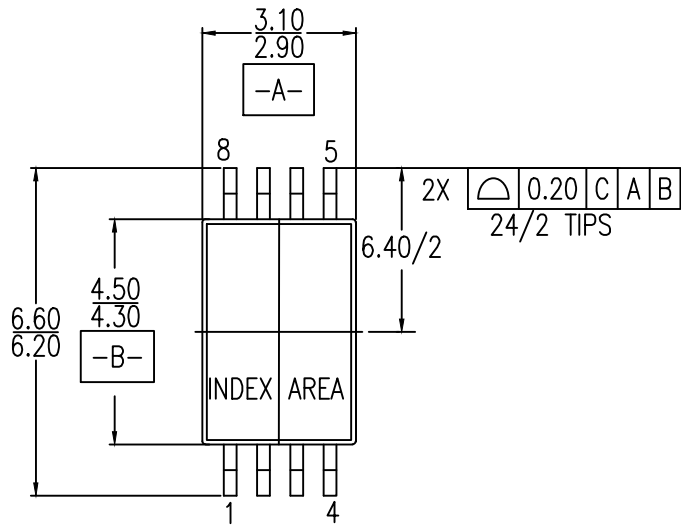
RECOMMENDED LAND PATTERN DIMENSION

NOTES:

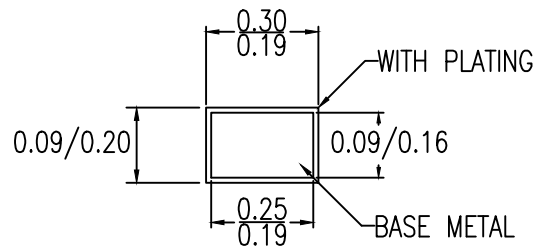
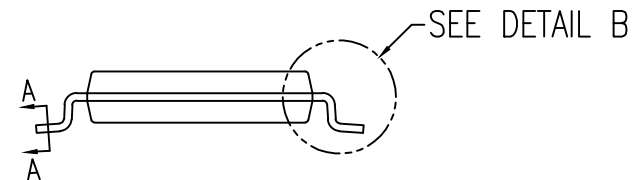
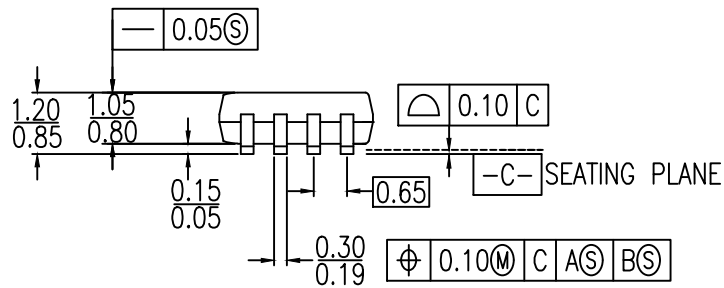
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 IDT 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
TITLE		CMG8 Package Outline Drawing 2.0 x 2.0 x 0.5 mm Body 0.5mm Pitch DFN
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C	PSC-4490	01
DO NOT SCALE DRAWING		SHEET 2 OF 2

DATE CREATED		REVISIONS		
REV	DESCRIPTION	APPROVED		
7/24/18	00	Revised from PSC-4056_09		R.C




DETAIL B



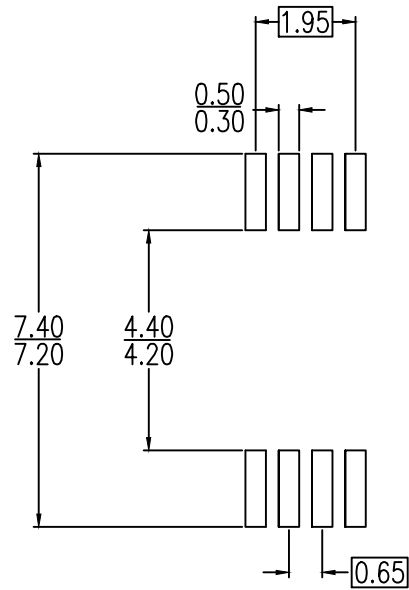
SECTION A-A

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSION ARE IN MM.

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 www.IDT.com	APPROVED	
DECIMAL	ANGULAR			
XX±	±			
XXX±				
		TITLE PGG8 Package Outline Drawing 4.4 mm Body, 0.65mm Pitch TSSOP		
SIZE	DRAWING No.	REV		
C	PSC-4768	00		
DO NOT SCALE DRAWING			SHEET 1 OF 2	


DATE CREATED	REVISIONS		
	REV	DESCRIPTION	APPROVED
7/24/18	00	Revised from PSC-4056_09	R.C



RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED		 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 www.IDT.com
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
TITLE PGG8 Package Outline Drawing 4.4 mm Body, 0.65mm Pitch TSSOP		
SIZE	DRAWING No.	REV
C	PSC-4768	00
DO NOT SCALE DRAWING		SHEET 2 OF 2