HCPL-5120, HCPL-5121 and 5962-04204

2.0 Amp Output Current IGBT Gate Drive
Hermetically Sealed Optocoupler

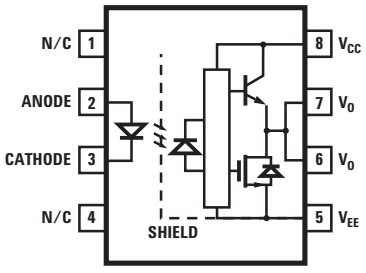
Data Sheet

Description

The HCPL-5120 contains a GaAsP LED optically coupled to an integrated circuit with a power output stage. The device is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200 V/100 A. For IGBTs with higher ratings, the HCPL-5120 can be used to drive a discrete power stage, which drives the IGBT gate.

The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial products, with full MIL-PRF-38534 Class H testing, or from Defense Supply Center Columbus (DLA) Standard Microcircuit Drawing (SMD) 5962-04204. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DLA Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits.

Schematic Diagram



Applications

- Industrial and Military Environments
- High Reliability Systems
- Harsh Industrial Environments
- Transportation, Medical, and Life Critical Systems
- Uninterruptible Power Supplies (UPS)
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- Switch Mode Power Supplies (SMPS)

Features

- Performance Guaranteed over Full Military Temperature Range: -55°C to +125°C
- Manufactured and Tested on a MIL-PRF-38534 Certified Line
- Hermetically Sealed Packages
- Dual Marked with Device Part Number and DLA Drawing Number QML-38534
- HCPL-3120 Function Compatibility
- 2.0 A Minimum Peak Output Current
- 0.5V Maximum Low Level Output Voltage (V_{OL}) : Eliminates Need for Negative Gate Drive
- 10 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000V
- I_{CC} = 5 mA Maximum Supply Current
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- Wide Operating V_{CC} Range: 15 to 30 Volts
- 500 ns Maximum Propagation Delay
- ±0.35µs Maximun Delay Between Devices

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Truth Table

LED	V_{CC} - V_{EE}	V_{CC} - V_{EE}	V_O
	"POSITIVE GOING" (i.e., TURN-ON)	"NEGATIVE GOING" (i.e., TURN-OFF)	
OFF	0 - 30 V	0 - 30 V	LOW
ON	0 - 11 V	0 - 9.5 V	LOW
ON	11 - 13.5 V	9.5 - 12 V	TRANSITION
ON	13.5 - 30 V	12 - 30 V	HIGH

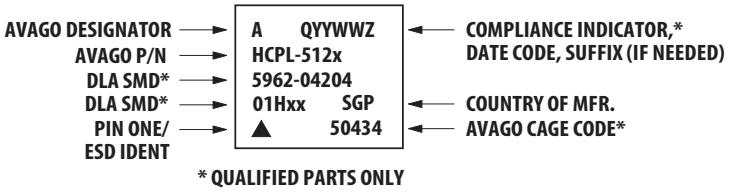
A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

Selection Guide: Lead Configuration Options

Avago Technologies Part Number and Options	
Commercial	HCPL-5120
MIL-PRF-38534, Class H	HCPL-5121
Standard Lead Finish	Gold Plate
Solder Dipped *	Option - 200
Butt Cut/Gold Plate	Option - 100
Gull Wing/Soldered *	Option - 300
SMD Part Number	
Prescript for all below	*5962-*
Gold Plate	0420401HPC
Solder Dipped *	0420401HPA
Butt Cut/Gold Plate	0420401HYC
Butt Cut/Soldered *	0420401HYA
Gull Wing/Soldered *	0420401HXA

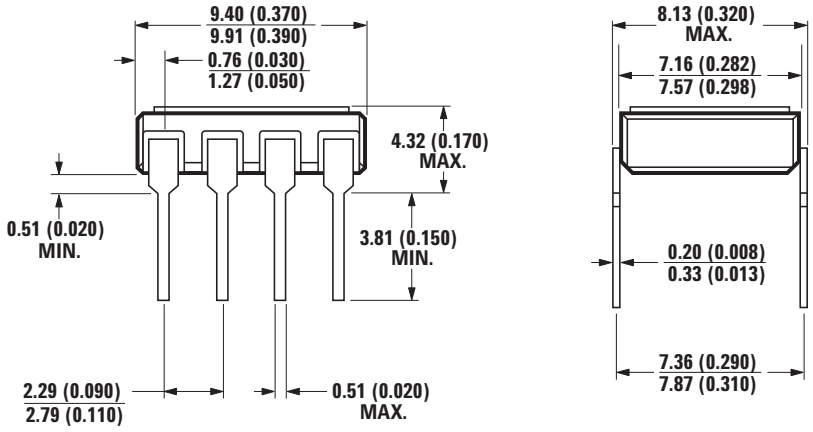
* Solder contains lead

Device Marking



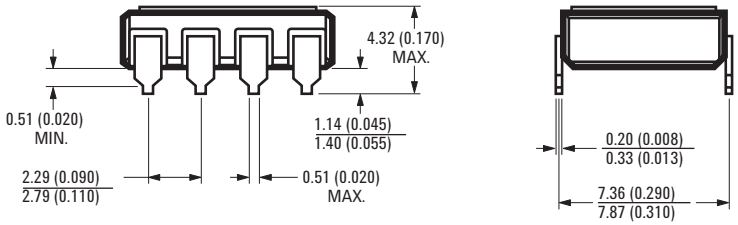
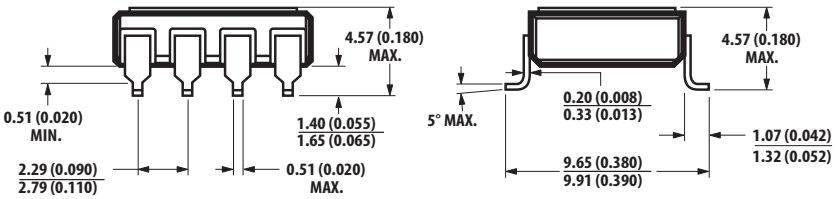
* QUALIFIED PARTS ONLY

Outline Drawing



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DLA Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

* Solder contains lead

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Case Temperature	T_C		+145	°C	
Junction Temperature	T_J		+150	°C	
Lead Solder Temperature			260 for 10s	°C	
Average Input Current	$I_{F\ AVG}$		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300 pps)	$I_{F\ PK}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH\ (PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL\ (PEAK)}$		2.5	A	2
Supply Voltage	$(V_{CC}\text{-}V_{EE})$	0	35	V	
Output Voltage	$V_{O\ (PEAK)}$	0	VCC	V	
Emitter Power Dissipation	P_E		45	mW	1
Output Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4

Notes:
1. No derating required for typical case-to-ambient thermal resistance (θ_{CA}=140°C/W). Refer to Figure 35.
2. Maximum pulse width = 10μs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0A. See Applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 102°C free air temperature at a rate of 6mW/°C for typical case-to-ambient thermal resistance (θ_{CA}=140°C/W). Refer to Figure 36.
4. Derate linearly above 102°C free air temperature at a rate of 6mW/°C for typical case-to-ambient thermal resistance (θ_{CA}=140°C/W). Refer to Figure 35 and 36.

ESD Classification

MIL-STD-883, Method 3015 (▲), Class 1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	Volts
Input Current (ON)	$I_{F\ (ON)}$	10	18	mA
Input Voltage (OFF)	$V_{F\ (OFF)}$	-3.0	0.8	Volts
Operating Temperature	T_A	-55	125	°C

Electrical Specifications (DC)

Over recommended operating conditions (T_A = -55 to +125°C, $I_{F(ON)}$ = 10 to 18 mA, $V_{F(OFF)}$ = -3.0 to 0.8V, V_{CC} = 15 to 30 V, V_{EE} = Ground), unless otherwise specified.

Parameter	Symbol	Test Conditions	Group A Subgroups (13)	Limits			Units	Fig	Note
				Min.	Typ. *	Max.			
High Level Output Current	I_{OH}	$V_O = (V_{CC} - 4\ V)$	1, 2, 3	0.5	1.5		A	2, 3, 17	2
		V_O = (VCC - 15 V)		2.0			A		1
Low Level Output Current	I_{OL}	$V_O = (V_{EE} + 2.5\ V)$	1, 2, 3	0.5	2.0		A	5, 6, 18	2
		$V_O = (V_{EE} + 15\ V)$		2.0			A		1
High Level Output Voltage	V_{OH}	I_O = -100 mA	1, 2, 3	(V_{CC} - 4)	(V_{CC} - 3)		V	1, 3, 19	3, 4
Low Level Output Voltage	V_{OL}	I_O = 100 mA	1, 2, 3		0.1	0.5	V	4, 6, 20	
High Level Supply Current	I_{CCH}	Output Open, I_F = 10 to 18 mA	1, 2, 3		2.5	5.0	mA	7, 8	
Low Level Supply Current	I_{CCL}	Output Open, V_F = -3.0 to +0.8V	1, 2, 3		2.5	5.0	mA		
Threshold Input Current Low to High	I_{FLH}	I_O = 0 mA, V_O > 5 V	1, 2, 3		3.5	9.0	mA	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}		1, 2, 3	0.8			V		
Input Forward Voltage	V_F	I_F = 10 mA	1, 2, 3	1.2	1.5	1.8	V	16	
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	I_F = 10 mA			-1.6		mV/°C		
Input Reverse Breakdown Voltage	BV_R	I_R = 10 µA	1, 2, 3	5			V		
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V			80		pF		
UVLO Threshold	V_{UVLO+}	V_O > 5 V, I_F = 10 mA	1, 2, 3	11.0	12.3	13.5	V	22, 37	
	V_{UVLO-}		1, 2, 3	9.5	10.7	12.0			
UVLO Hysteresis	$UVLO_{HYS}$				1.6				

*All typical values at T_A = 25°C and V_{CC} - V_{EE} = 30 V, unless otherwise noted.

Switching Specifications (AC)

Over recommended operating conditions (T_A = -55 to +125°C, $I_{F(ON)}$ = 10 to 18 mA, $V_{F(OFF)}$ = -3.0 to 0.8V, V_{CC} = 15 to 30 V, V_{EE} = Ground), unless otherwise specified.

Parameter	Symbol	Test Conditions	Group A Subgroups (13)	Limits			Units	Fig	Note
				Min.	Typ. *	Max.			
Propagation Delay Time to High Output Level	t_{PLH}	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%	9, 10, 11	0.10	0.30	0.50	µs	10, 11, 12, 13, 14, 23	11
Propagation Delay Time to Low Output Level	t_{PHL}		9, 10, 11	0.10	0.30	0.50	µs		
Pulse Width Distortion	PWD		9, 10, 11			0.3	µs		12
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})		9, 10, 11	-0.35		0.35	µs	33, 34	7
Rise Time	t_r				0.1		µs	23	
Fall Time	t_f				0.1		µs		
UVLO Turn On Delay	$t_{UVLO\ ON}$	V_O > 5 V, I_F = 10 mA			0.8		µs	22	
UVLO Turn Off Delay	$t_{UVLO\ OFF}$	V_O < 5 V, I_F = 10 mA			0.6				
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	I_F = 10mA, V_{CM} = 1000 V, V_{CC} = 30 V, T_A = 25°C	9	10			kV/µs	24	8, 9, 14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	V_{CM} = 1000 V, V_F = 0 V, V_{CC} = 30 V, T_A = 25°C	9	10			kV/µs		8, 10, 14

*All typical values at T_A = 25°C and $V_{CC} - V_{EE}$ = 30 V, unless otherwise noted.

Package Characteristics

Over recommended operating conditions (T_A = -55 to +125°C) unless otherwise specified.

Parameter	Symbol	Test Conditions	Group A Subgroups (13)	Limits			Units	Fig	Note
				Min.	Typ.*	Max.			
Input-Output Leakage Current	I_{I-O}	V_{I-O} = 1500Vdc, RH ≤ 65%, t = 5 sec., T_A = 25°C	1			1.0	μA		5, 6
Resistance (Input-Output)	R_{I-O}	V_{I-O} = 500 V_{DC}			10^{10}		Ω		6
Capacitance (Input-Output)	C_{I-O}	f = 1 MHz			2.5		pF		6

*All typicals at T_A = 25°C.

Notes:

1. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See Applications section for additional details on limiting I_{OH} peak.
2. Maximum pulse width = 50 μs, maximum duty cycle = 0.5%.
3. In this test V_{OH} is measured with a dc load current. When driving capacitive loads V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
4. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
5. This is a momentary withstand test, not an operating condition.
6. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
7. The difference between t_{PHL} and t_{PLH} between any two HCPL-5120 parts under the same test condition.
8. Pins 1 and 4 need to be connected to LED common.
9. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15.0 V).
10. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V).
11. This load condition approximates the gate load of a 1200 V/75A IGBT.
12. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and Class H parts receive 100% testing at 25, 125, and -55°C (Sub groups 1 and 9, 2 and 10, 3 and 11, respectively).
14. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

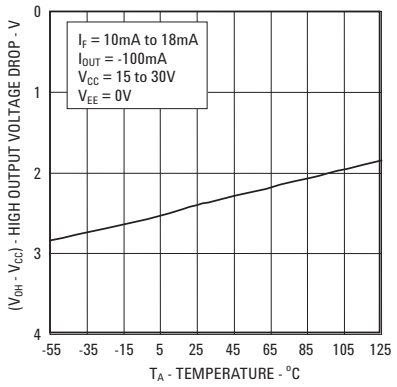


Figure 1. V_{OH} vs. Temperature

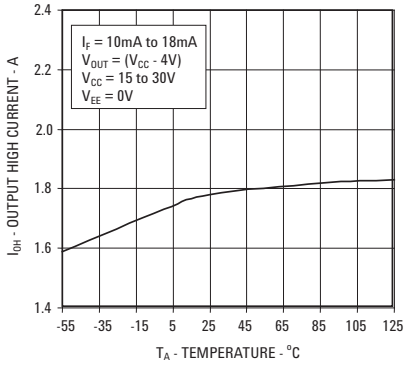


Figure 2. I_{OH} vs. Temperature

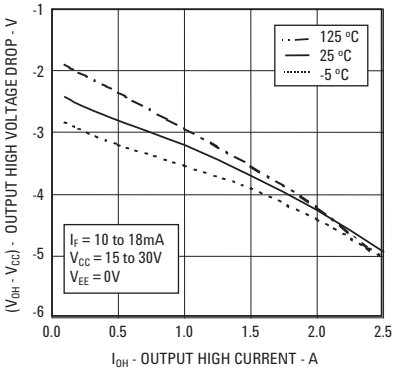


Figure 3. V_{OH} vs. I_{OH}

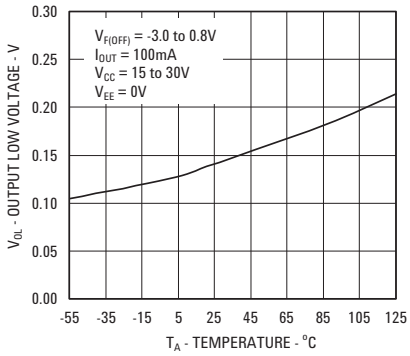


Figure 4. V_{OL} vs. Temperature

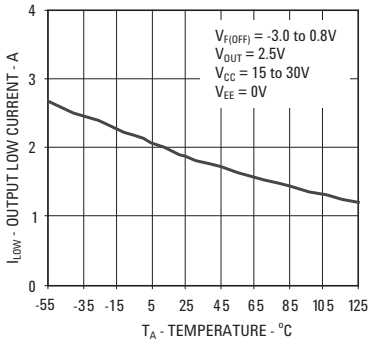


Figure 5. I_{OL} vs. Temperature

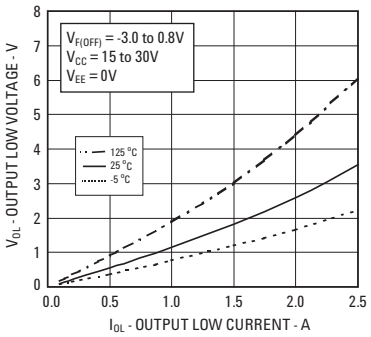


Figure 6. V_{OL} vs. I_{OL}

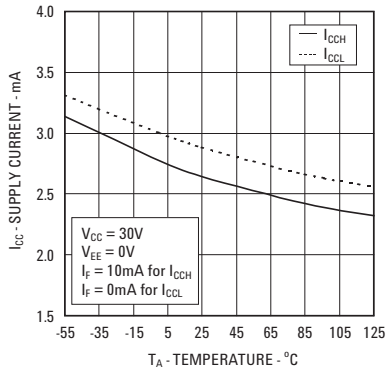


Figure 7. I_{CC} vs. Temperature

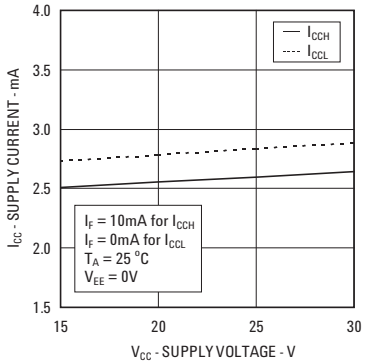


Figure 8. I_{CC} vs. V_{CC}

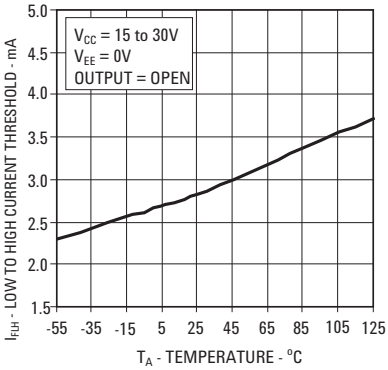


Figure 9. I_{FLH} vs. Temperature

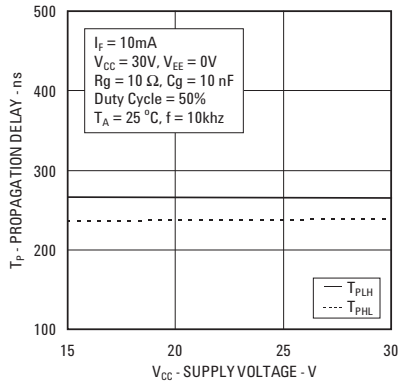


Figure 10. Propagation Delay vs. V_{CC}

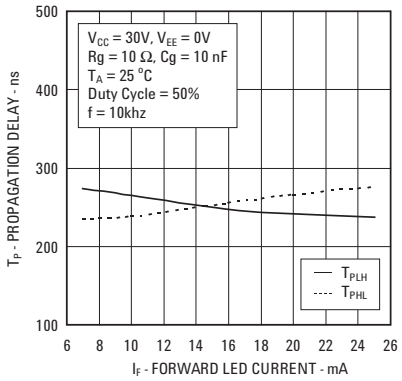


Figure 11. Propagation Delay vs. I_F

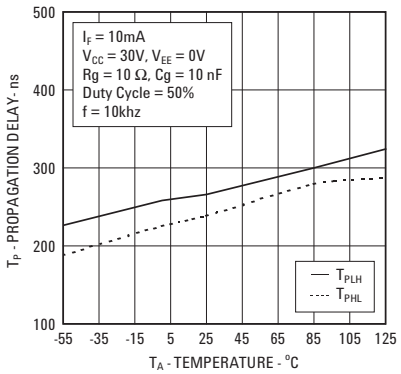


Figure 12. Propagation Delay vs. Temperature

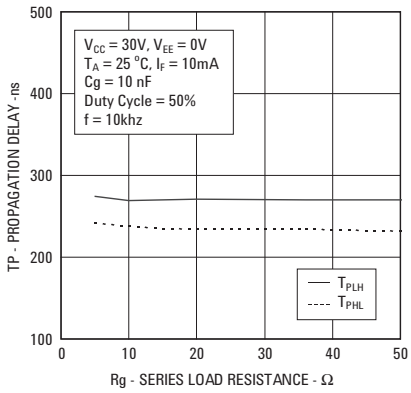


Figure 13. Propagation Delay vs. Rg

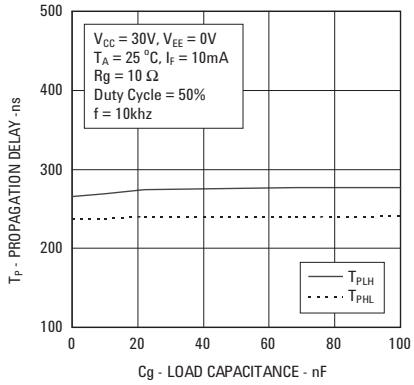


Figure 14. Propagation Delay vs. Cg

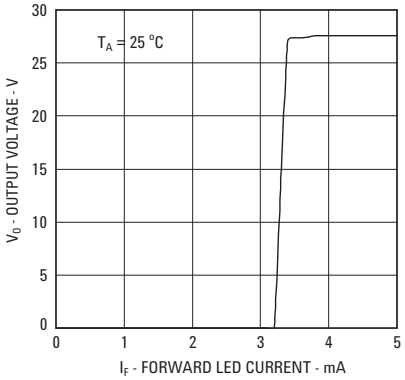


Figure 15. Transfer Characteristics

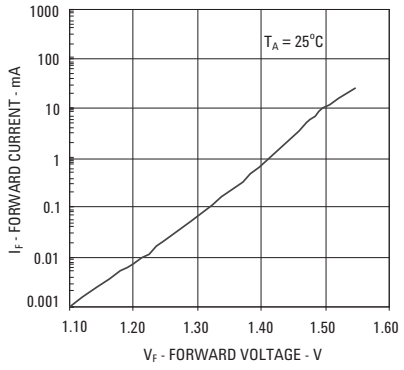


Figure 16. Input Current vs. Forward Voltage

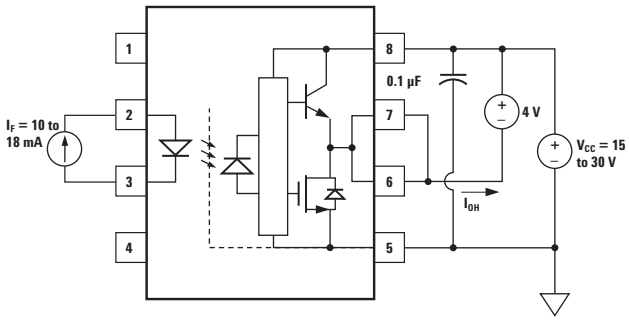


Figure 17. I_{OH} Test Circuit

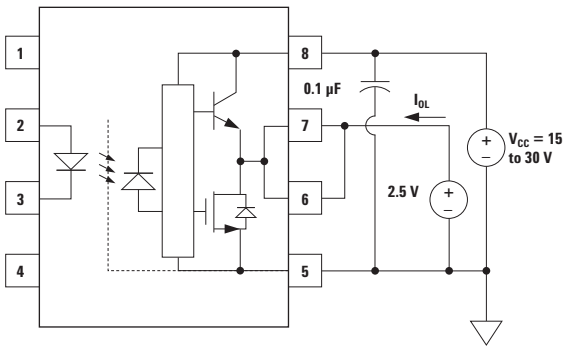


Figure 18. I_{OL} Test Circuit

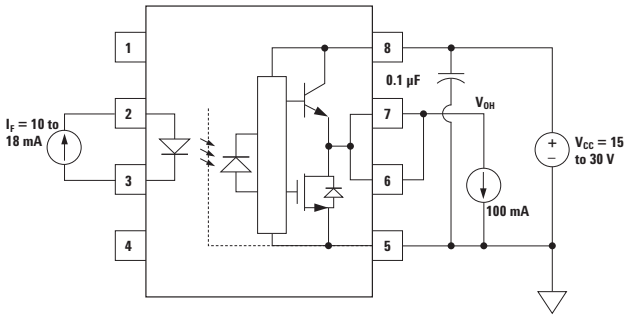


Figure 19. V_{OH} Test Circuit

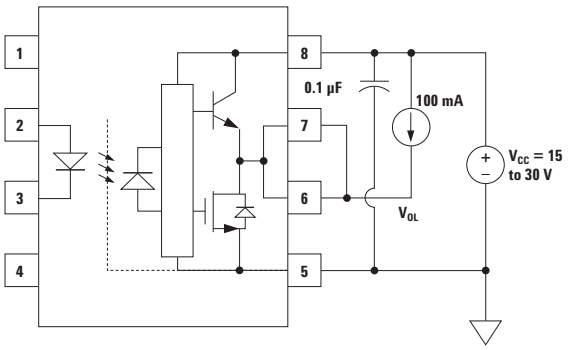


Figure 20. V_{OL} Test Circuit

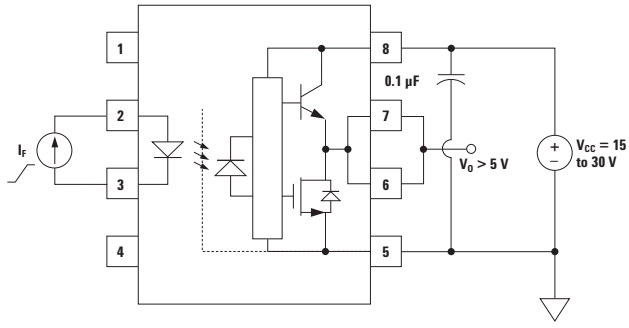


Figure 21. I_{FLH} Test Circuit

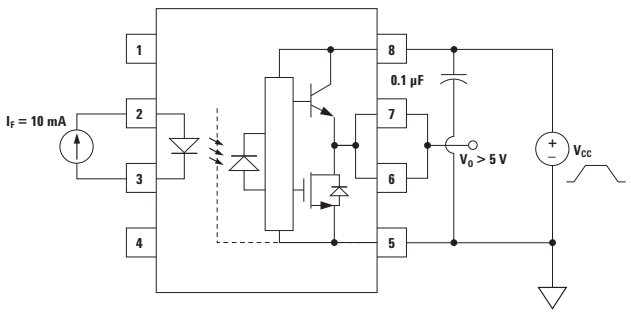


Figure 22. UVLO Test Circuit

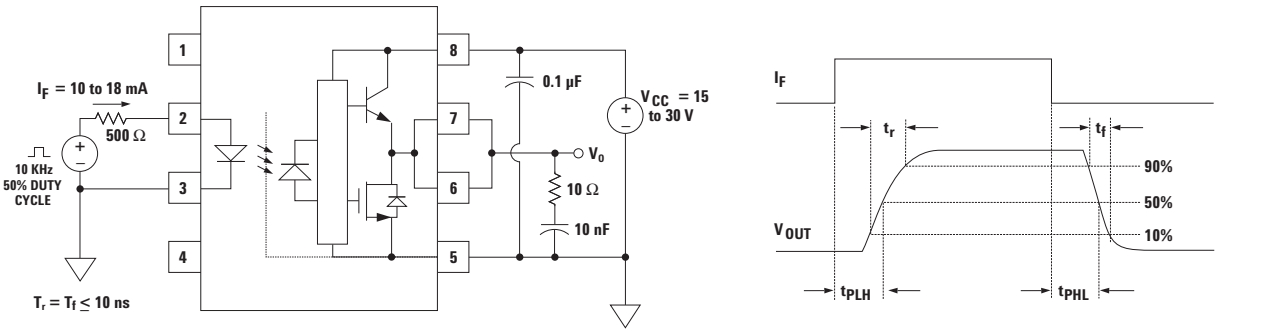


Figure 23. t_{PLH}, t_{PHL}, and t_f Test Circuit and Waveforms

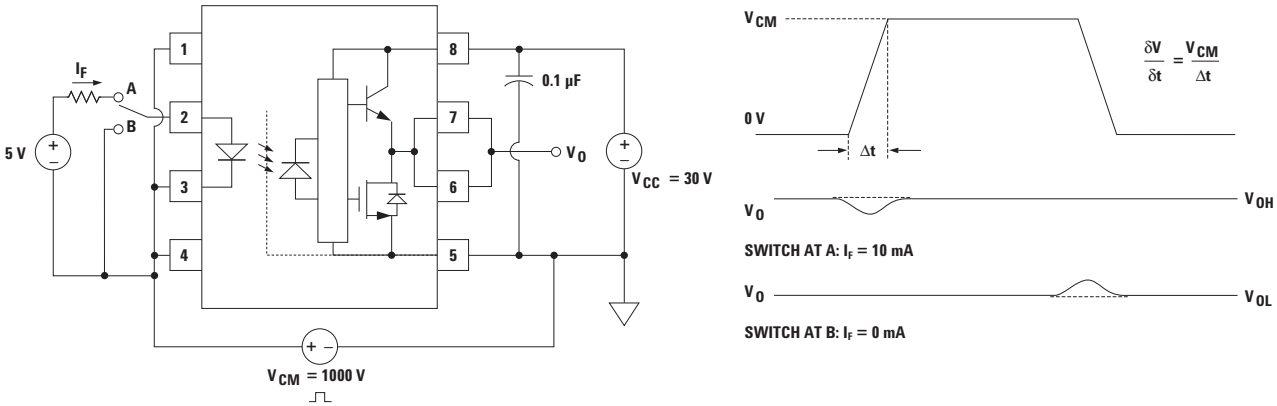


Figure 24. CMR Test Circuit and Waveforms

Applications Information

Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-5120 has a very low maximum V_{OL} specification of 0.5 V. The HCPL-5120 realizes this very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the HCPL-5120 is in the low state, the IGBT gate is shorted to the emitter by R_g + 1 Ω. Minimizing Rg and the lead inductance from the HCPL-5120 to the IGBT gate and emitter (possibly by mounting the HCPL-5120 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-5120 input as this can result in unwanted coupling of transient signals into the HCPL-5120 and degrade performance. (If the IGBT drain must be routed near the HCPL-5120 input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-5120.)

Selecting the Gate Resistor (R_g) to Minimize IGBT Switching Losses.

Step 1: Calculate R_g Minimum from the I_{OL} Peak Specification.

The IGBT and R_g in Figure 26 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-5120.

$$R_g = \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}}$$

$$= \frac{(V_{CC} - V_{EE} - 2V)}{I_{OLPEAK}}$$

$$= \frac{(15\,V + 5\,V - 2V)}{2.5\,A}$$

$$= 7.2\Omega \approx 8\Omega$$

The V_{OL} value of 2 V in the previous equation is a conservative value of V_{OL} at the peak current of 2.5A (see Figure 6). At lower Rg values the voltage supplied by the HCPL-5120 is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used V_{EE} in the previous equation is equal to zero volts

Step 2: Check the HCPL-5120 Power Dissipation and Increase R_g if Necessary.

The HCPL-5120 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O):

$$P_T = P_E + P_O$$

$$P_E = I_F \bullet V_F \bullet Duty\ Cycle$$

$$P_O = P_{O(BIAS)} + P_{O\ (SWITCHING)}$$

$$= I_{CC} \bullet (V_{CC} - V_{EE}) + ESW(R_g, Q_g) \bullet f$$

For the circuit in Figure 26 with I_F (worst case) = 18 mA, R_g = 8 Ω, Max Duty Cycle = 80%, Q_g = 500 nC, f = 20 kHz and T_A max = 125°C:

$$P_E = 18\,mA \bullet 1.8\,V \bullet 0.8 = 26\,mW$$

$$P_O = 4.25\,mA \bullet 20\,V + 1.0\mu J \bullet 20\,kHz$$

$$= 85\,mW + 20\,mW$$

$$= 105\,mW$$

$$< 112\,mW\ (P_{O(MAX)} @ 125°C = 250\,mW - 23°C \bullet 6\,mW/°C)$$

The value of 4.25 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 5 mA (which occurs at -55°C) to I_{CC} max at 125°C.

Since P_O for this case is less than $P_{O(MAX)}$, R_g of 8 Ω is appropriate.

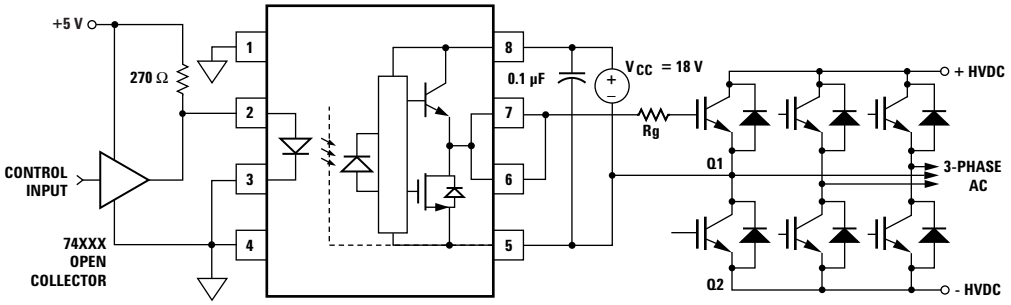


Figure 25. Recommended LED Drive and Application Circuit

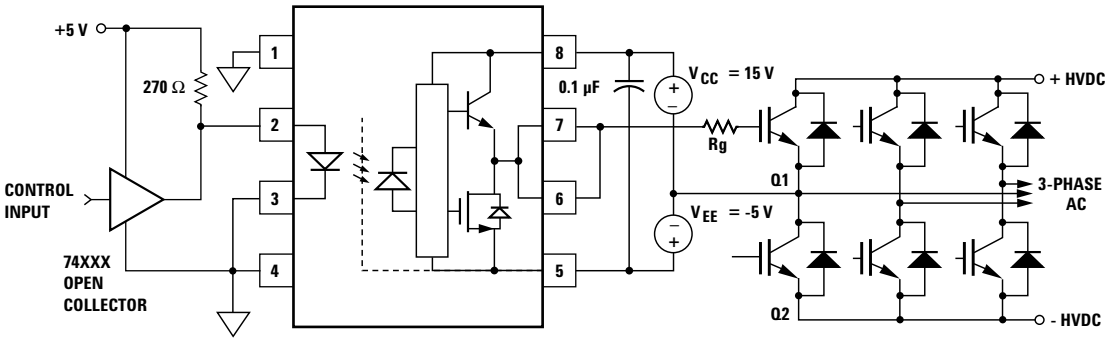


Figure 26. Typical Application Circuit with Negative IGBT Gate Drive

P_E Parameter	Description
I_F	LED Current
V_F	LED On Voltage
Duty Cycle	Maximum LED Duty Cycle
P_O Parameter	**Description**
I_{CC}	Supply Current
V_{CC}	Positive Supply Voltage
V_{EE}	Negative Supply Voltage
E_{SW} (Rg, Qg)	Energy Dissipation in the HCPL-5120 for each IGBT Switching Cycle (See Figure 27)
f	Switching Frequency

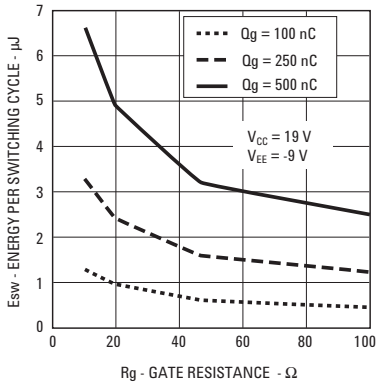


Figure 27. Energy Dissipated in the HCPL-5120 for Each IGBT Switching Cycle

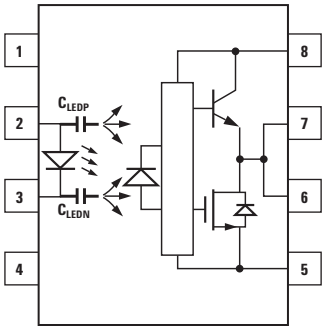


Figure 28. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

LED Drive Circuit Considerations for Ultra High CMR Performance.

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 28. The HCPL-5120 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 29. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 10 kV/µs CMR while minimizing component complexity. Techniques to keep the LED in the proper state are discussed in the next two sections.

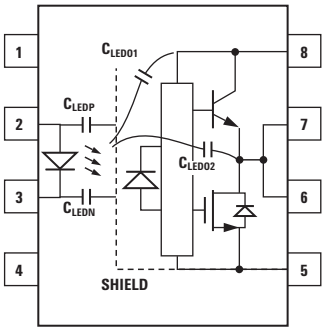


Figure 29. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

CMR with the LED On (CMR_H).

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 7 mA to achieve 10 kV/µs CMR.

CMR with the LED Off (CMR_L).

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a $-dV_{cm}/dt$ transient in Figure 30, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 31, cannot keep the LED off during a $+dV_{cm}/dt$ transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 32 is an alternative drive circuit which, like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

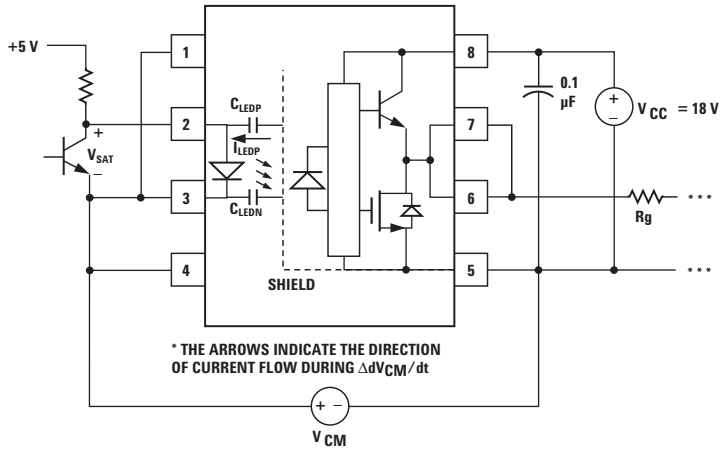


Figure 30. Equivalent Circuit for Figure 25 During Common Mode Transient.

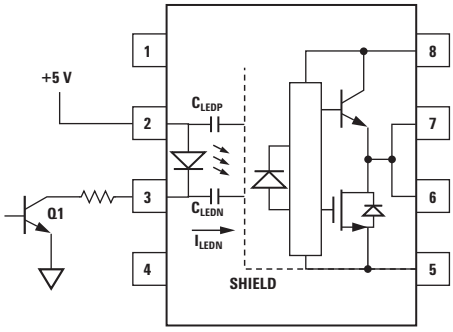


Figure 31. Not Recommended Open Collector Drive Circuit

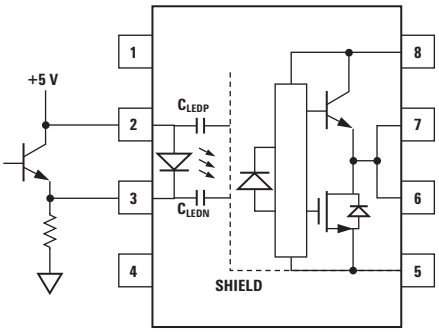


Figure 32. Recommended LED Drive Circuit for Ultra-High CMR

IPM Dead Time and Propagation Delay Specifications.

The HCPL-5120 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 25) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rail.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 33. The amount of delay necessary to achieve this conditions is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 350 ns over the operating temperature range of -55°C to 125°C.

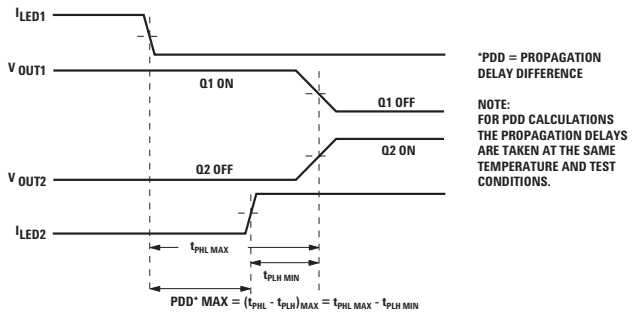


Figure 33. Minimum LED Skew for Zero Dead Time

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 34. The maximum dead time for the HCPL-5120 is 700 ns (= 350 ns - (-350 ns)) over an operating temperature range of -55°C to 125°C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

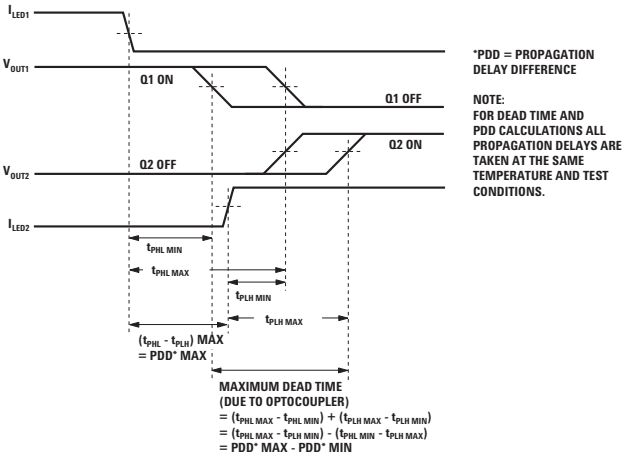


Figure 34. Waveforms for Dead Time Calculations

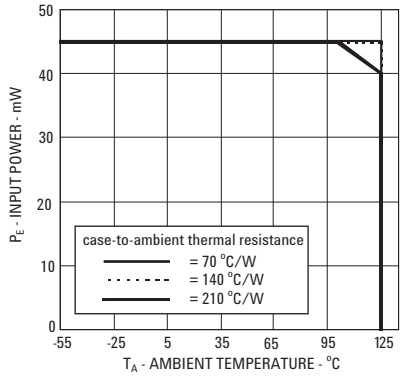


Figure 35. Input Thermal Derating Curve, Dependence of case-to-ambient Thermal Resistance

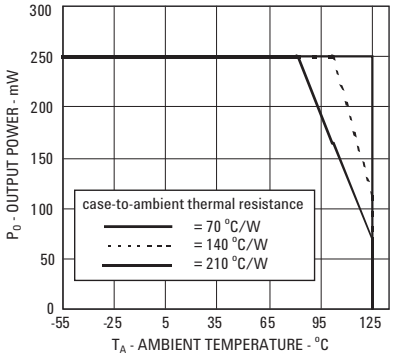


Figure 36. Output Thermal Derating Curve, Dependence of case-to-ambient Thermal Resistance