BROADCOM®

Data Sheet

ACPL-267xL, ACPL-268KL, ACPL-560xL, ACPL-563xL, ACPL-665xL, and 5962-08242[1]

Hermetically Sealed, 3.3V High-Speed, High CMR, Logic Gate Optocouplers

Description

The Broadcom® ACPL-267xL, ACPL-268KL, ACPL-560xL, ACPL-563xL, ACPL-665xL, and 5962-08242 units are single, dual, and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard commercial product or with full MIL-PRF-38534 Class Level H or K testing or from DLA Standard Microcircuit Drawing (SMD) 5962-08242. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Features

- Low power consumption
- 3.3V supply voltages
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Four hermetically sealed package configurations
- Performance guaranteed over full military temperature range: –55°C to +125°C
- High speed: 10 Mbd typical
- CMR: >10,000 V/µs typical
- 1500 Vdc withstand test voltage
- TTL circuit compatibility
- HCPL-260L/060L/263L/063L function compatibility

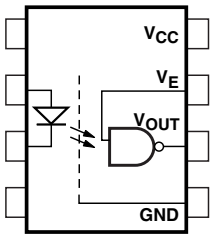
Applications

- Military and aerospace
- High reliability systems
- Transportation, medical, and life critical systems
- Line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Isolation for computer, communication, and test equipment systems

1. See Selection Guide – Package Styles and Lead Configuration Options for available extensions.

Functional Diagram

Multiple channel devices available.



NOTE: An external 0.01-µF to 0.1-µF bypass capacitor must be connected as close as possible between pin V_{CC} and GND.

Truth Tables

(Positive Logic)

Multichannel Devices

Input	Output
On (H)	L
Off (L)	H

Single-Channel DIP

Input	Enable	Output
On (H)	H	L
Off (L)	H	H
On (H)	L	H
Off (L)	L	H

Each channel contains a GaAsP light emitting diode that is optically coupled to an integrated high-speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/µs. Package styles for these parts are 8- and 16-pin DIP through hole (case outlines P and E respectively), and 16-pin surface mount DIP flat pack (case outline F). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide – Package Styles and Lead Configuration Options for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations, and are as noted. Additionally, the same package assembly processes and materials are used in all devices.

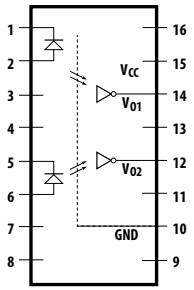
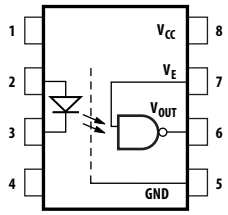
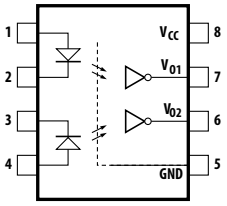
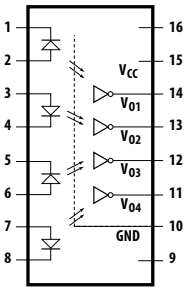
Selection Guide – Package Styles and Lead Configuration Options

Package	16-Pin DIP	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack
Lead Style	Through Hole	Through Hole	Through Hole	Unformed leads
Channels	2	1	2	4
Common Channel Wiring	VCC, GND	None	VCC, GND	VCC, GND
Withstand Test Voltage	1500 Vdc	1500 Vdc	1500 Vdc	1500 Vdc
Part Number and Options				
Standard Commercial	ACPL-2670L	ACPL-5600L	ACPL-5630L	ACPL-6650L
MIL-PRF-38534, Class H	ACPL-2672L	ACPL-5601L	ACPL-5631L	ACPL-6651L
MIL-PRF-38534, Class K	ACPL-268KL	ACPL-560KL	ACPL-563KL	ACPL-665KL
Standard Lead Finish[a]	Gold Plate	Gold Plate	Gold Plate	Gold Plate
Solder Dipped[b]	Option -200	Option -200	Option -200	
Butt Cut/Gold Plate[a]	Option -100	Option -100	Option -100	
Gull Wing/Soldered[b]	Option -300	Option -300	Option -300	
Class H SMD Part Number				
Prescript for all below	5962-	5962-	5962-	5962-
Gold Plate[a]	0824203HEC	0824201HPC	0824202HPC	0824204HZC
Solder Dipped[b]	0824203HEA	0824201HPA	0824202HPA	
Butt Cut/Gold Plate[a]	0824203HUC	0824201HYC	0824202HYC	
Butt Cut/Soldered[b]	0824203HUA	0824201HYA	0824202HYA	
Gull Wing/Soldered[b]	0824203HTA	0824201HXA	0824202HXA	
Class K SMD Part Number				
Prescript for all below	5962-	5962-	5962-	5962-
Gold Plate[a]	0824203KEC	0824201KPC	0824202KPC	0824204KZC
Solder Dipped[b]	0824203KEA	0824201KPA	0824202KPA	
Butt Cut/Gold Plate[a]	0824203KUC	0824201KYC	0824202KYC	
Butt Cut/Soldered[b]	0824203KUA	0824201KYA	0824202KYA	
Gull Wing/Soldered[b]	0824203KTA	0824201KXA	0824202KXA	

a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.

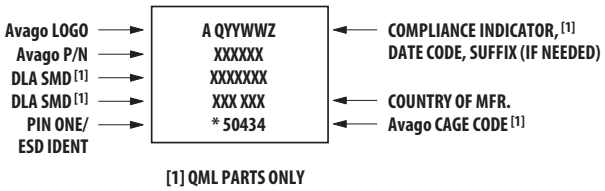
b. Solder lead finish: Sn63/Pb37.

Functional Diagrams

16-Pin DIP	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack
Through Hole	Through Hole	Through Hole	Unformed Leads
2 Channels	1 Channel	2 Channels	4 Channels
			

NOTE: All DIP and flat pack devices have common V_{CC} and ground. Single-channel DIP has an enable pin 7.

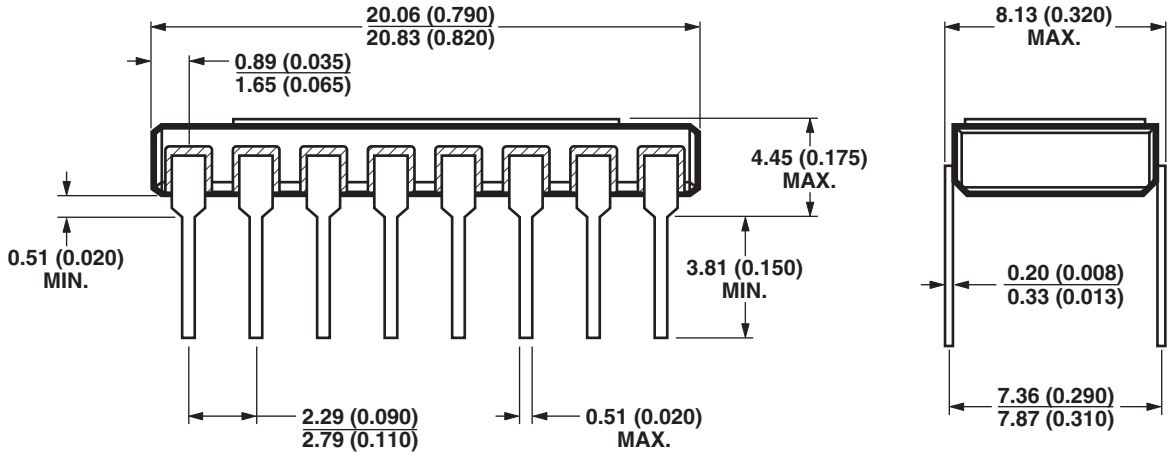
Device Marking



[1] QML PARTS ONLY

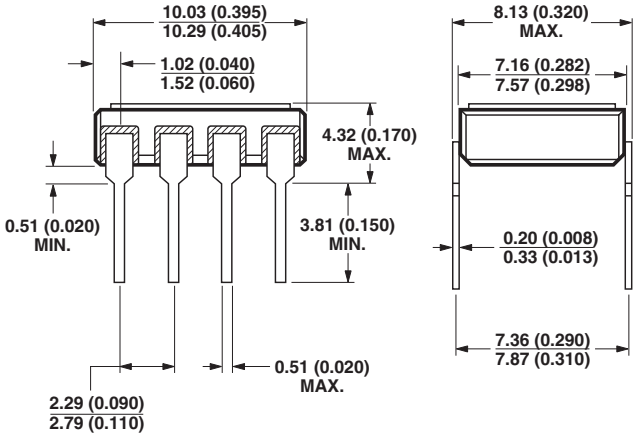
Outline Drawings

16-Pin DIP Through Hole, 2 Channels



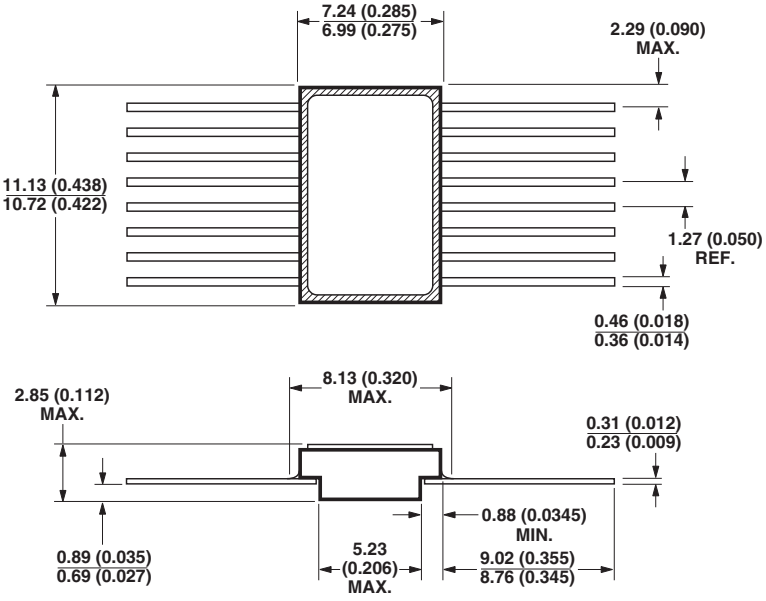
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

8-Pin DIP Through Hole, 1 and 2 Channels



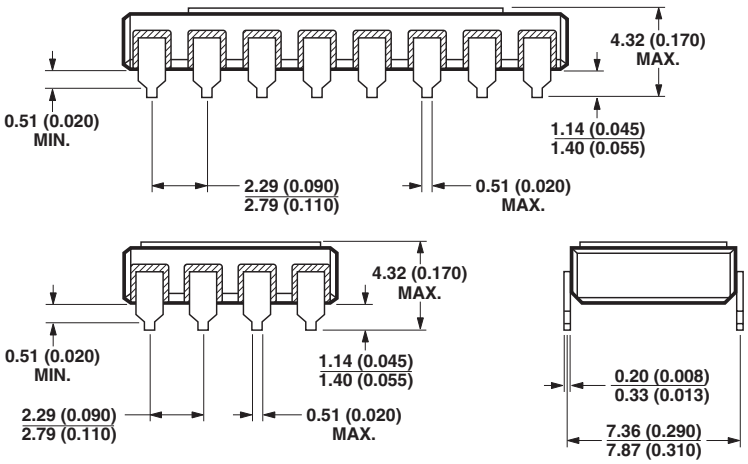
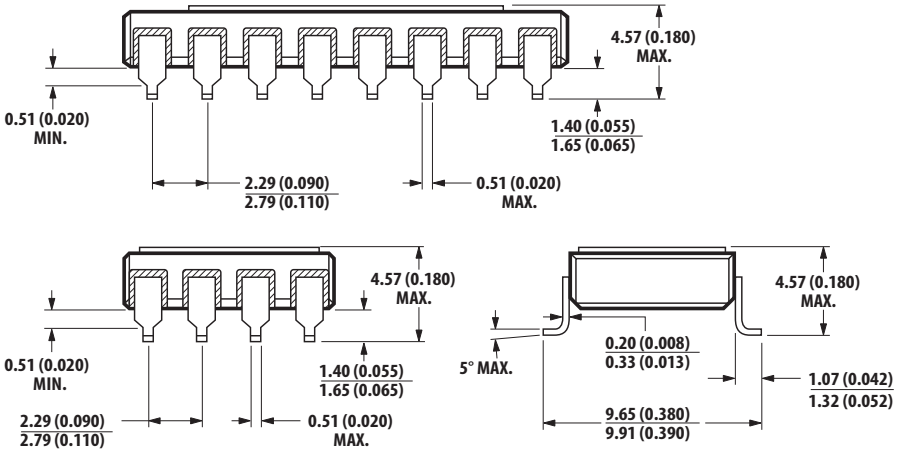
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

16-Pin Flat Pack, 4 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on standard commercial, class H and class K product in 8- and 16-pin DIP.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on standard commercial, class H and class K products in 8- and 16-pin DIP. DLA Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on standard commercial, class H and class K product in 8- and 16-pin DIP. This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

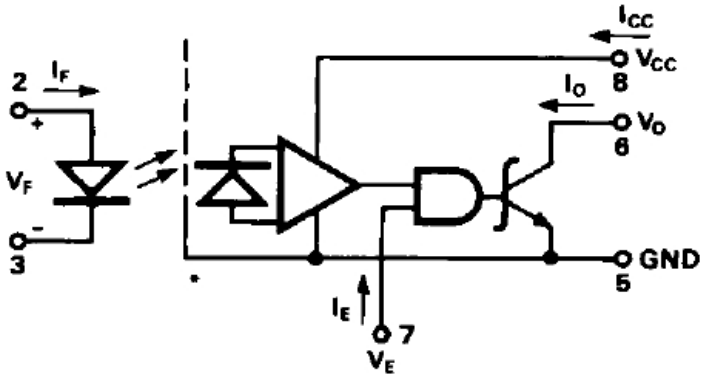
No derating required up to +125°C.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	–65	+150	°C
Operating Temperature	T_A	–55	+125	°C
Case Temperature	T_C	—	+170	°C
Junction Temperature	T_J	—	+175	°C
Lead Solder Temperature		—	260 for 10 sec	°C
Peak Forward Input Current (each channel, ≤1 ms duration)	$I_{F(PEAK)}$	—	40	mA
Average Input Forward Current (each channel)	$I_{F(AVG)}$	—	20	mA
Input Power Dissipation (each channel)		—	35	mW
Reverse Input Voltage (each channel)	V_R	—	5	V
Supply Voltage (1 minute maximum)	V_{CC}	—	7.0	V
Output Current (each channel)	I_O	—	25	mA
Output Voltage (each channel)	V_O	—	7	V
Output Power Dissipation (each channel)	P_O	—	40	mW
Package Power Dissipation (each channel)	P_D	—	200	mW

Single-Channel Product Only

Parameter	Symbol	Min.	Max.	Unit
Enable Input Voltage	V_E	—	3.6	V

8-Pin Ceramic DIP Single-Channel Schematic



NOTE: Note enable pin 7.

ESD Classification

MIL-PRF-38534 and MIL-STD-883, Method 3015

ACPL-5600L/01L/0KL, 5962-0824201	▲B, Class 1B
ACPL-5630L/31L/3KL, ACPL-6650L/51L/5KL, 5962-0824202, 5962-0824204	▲▲▲A, Class 3A
ACPL-2670L/72L/268KL, 5962-0824203	▲▲, Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Input Current, Low Level, Each Channel	I_{FL}	0	250	µA
Input Current, High Level, Each Channel	I_{FH}	10	20	mA
Supply Voltage, Output	V_{CC}	3.0	3.6	V
Fan Out (TTL Load) Each Channel	N	—	6	

Single-Channel Product Only

Parameter	Symbol	Min.	Max.	Unit
High-Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low-Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics

T_A = –55°C to +125°C, unless otherwise specified.

Parameter		Symbol	Test Conditions	Group A[a] Subgroups	Limits			Unit	Fig.	Note
					Min.	Typ.[b]	Max.			
High-Level Output Current		I_{OH}	V_{CC} = 3.3V, V_O = 3.3V, I_F = 250 µA	1, 2, 3	—	6	250	µA	1	c
Low-Level Output Voltage		V_{OL}	V_{CC} = 3.3V, I_F = 10 mA, I_{OL} (Sinking) = 10 mA	1, 2, 3	—	0.3	0.6	V	2	c, d
Current Transfer Ratio		h_F CTR	V_O = 0.6V, I_F = 10 mA, V_{CC} = 3.3V	1, 2, 3	100	—	—	%		c
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 3.3V, I_F = 0 mA	1, 2, 3	—	5	11	mA		c
	Dual Channel		V_{CC} = 3.3V, I_{F1} = I_{F2} = 0 mA		—	10	22	mA		
	Quad Channel		V_{CC} = 3.3V, I_{F1} = I_{F2} = I_{F3} = I_{F4}= 0 mA		—	17	44	mA		

Parameter		Symbol	Test Conditions	Group A[a] Subgroups	Limits			Unit	Fig.	Note
					Min.	Typ.[b]	Max.			
Logic Low Supply Current	Single Channel	I_{CCL}	V_{CC} = 3.3V, I_F = 20 mA	1, 2, 3	—	6	15	mA		c
	Dual Channel		V_{CC} = 3.3V, $I_{F1} = I_{F2}$ = 20 mA		—	12	30	mA		
	Quad Channel		V_{CC} = 3.3 V, $I_{F1} = I_{F2} = I_{F3} = I_{F4}$ = 20 mA		—	22	60	mA		
Input Forward Voltage		V_F	I_F = 20 mA	1, 2	—	1.55	1.75	V	3	c
				3	—	—	1.85			
Input Reverse Breakdown Voltage		BV_R	I_R = 10 µA	1, 2, 3	5	—	—	V		c
Input-Output Leakage Current		I_{I-O}	RH ≤ 65%, T_A = 25°C, t = 5s, V_{I-O} = 1500 Vdc	1	—	—	1.0	µA		e, f
Capacitance Between Input/Output		C_{I-O}	f = 1 MHz, T_C = 25°C	4	—	1.0	4.0	pF		c, g, j
Propagation Delay Time to High Output Level		t_{PLH}	V_{CC} = 3.3V, R_L = 510Ω, C_L = 50 pF, I_F = 13 mA	9	—	43	100	ns	4, 5, 6	c, h
				10, 11	—	—	140			
Propagation Delay Time to Low Output Level		t_{PHL}	—	9	—	54	100	ns		
				10, 11	—	—	120			
Output Rise Time		t_{LH}	R_L = 510Ω, C_L = 50 pF, I_F = 13 mA	9, 10, 11	—	20	90	ns		c
Output Fall Time		t_{HL}			—	8	40			
Common Mode Transient Immunity at High Output Level		$\|CM_H\|$	V_{CM} = 50V (PEAK), V_{CC} = 3.3V, V_O (min.) = 2V, R_L = 510Ω, I_F = 0 mA	9, 10, 11	1000	>10000	—	V/µs	7	c, i, j
Common Mode Transient Immunity at Low Output Level		$\|CM_L\|$	V_{CM} = 50V (PEAK), V_{CC} = 3.3V, V_O (max.) = 0.8V, R_L = 510Ω, I_F = 10 mA	9, 10, 11	1000	>10000	—	V/µs	7	c, i, j

a. Standard commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). Class H and K parts receive 100% testing at 25°C, 125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

b. All typical values are at V_{CC} = 3.3V, T_A = 25°C.

c. Each channel.

d. It is essential that a bypass capacitor (0.01 µF to 0.1 µF, ceramic) be connected as close as possible from pin V_{CC} to ground.

e. All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

f. This is a momentary withstand test, not an operating condition.

g. Measured between each input pair shorted together and all output connections for that channel shorted together.

h. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

i. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).

j. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

Single-Channel Product Only

Parameter	Symbol	Test Conditions	Group A[a] Subgroups	Limits			Unit	Fig.	Note
				Min.	Typ.[b]	Max.			
Low-Level Enable Current	I_{EL}	V_{CC} = 3.3V, V_E = 0.5V	1, 2, 3	–2.0	–0.54	—	mA		
High-Level Enable Voltage	V_{EH}		1, 2, 3	2.0	—	—	V		c
Low-Level Enable Voltage	V_{EL}		1, 2, 3	—	—	0.8	V		

a. Standard commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). Class H and K parts receive 100% testing at 25°C, 125°C, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

b. All typical values are at V_{CC} = 3.3V, T_A = 25°C.

c. No external pull-up is required for a high logic state on the enable input.

Typical Characteristics

T_A = 25°C, V_{CC} = 3.3V.

Parameter	Sym.	Typ.	Unit	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0V, f = 1 MHz		a
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	–1.5	mV/°C	I_F = 20 mA		a
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500V		b

a. Each channel.

b. All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

Single-Channel Product Only

Parameter	Sym.	Typ.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	32	ns	R_L = 510Ω, C_L = 50 pF, I_F = 13 mA, V_{EH} = 3V, V_{EL} = 0V	8, 9	a, b
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	28	ns			a, c

a. Each channel.

b. The t_{ELH} enable propagation delay is measured from the 1.5V point on the trailing edge of the enable input pulse to the 1.5V point on the trailing edge of the output pulse.

c. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the enable input pulse to the 1.5V point on the leading edge of the output pulse.

Dual and Quad Channel Product Only

Parameter	Sym.	Typ.	Unit	Test Conditions	Fig.	Note
Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity ≤ 65%, V_{I-I} = 500V, t = 5s		a
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500V		a
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		a

a. Measured between adjacent input pairs shorted together for each multichannel device.

Figure 1: High-Level Output Current vs. Temperature

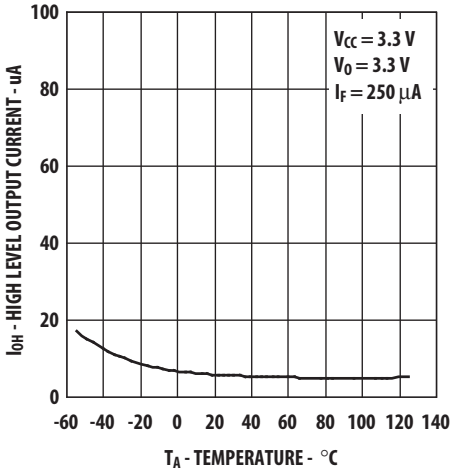


Figure 2: Input-Output Characteristics

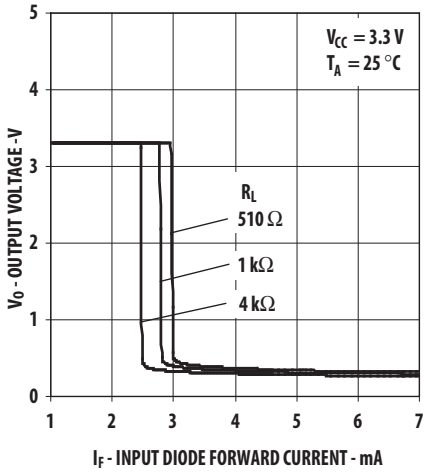


Figure 3: Input Diode Forward Characteristics

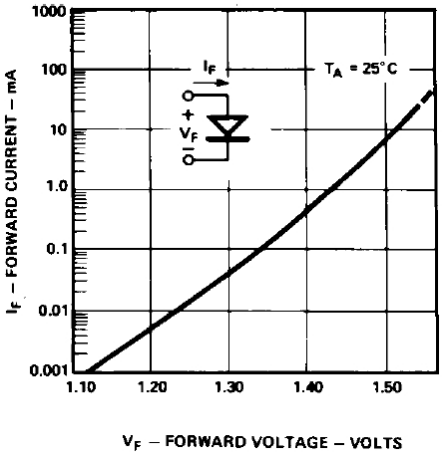
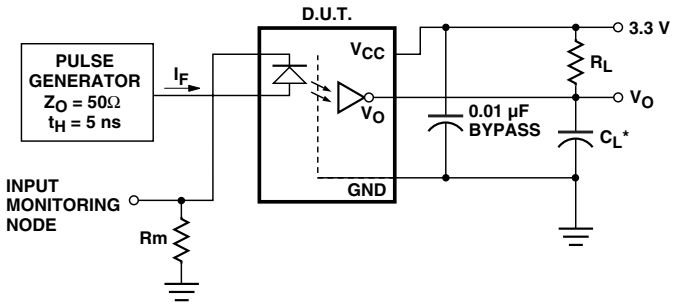


Figure 4: Test Circuit for t_{PHL} and t_{PLH}



* C_L INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

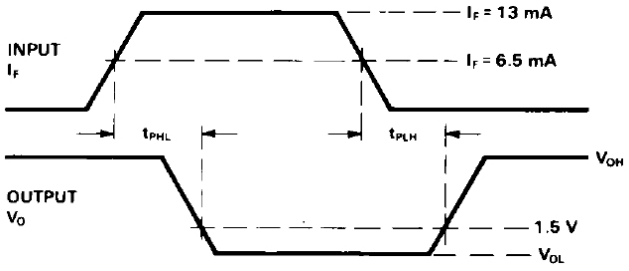


Figure 5: Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

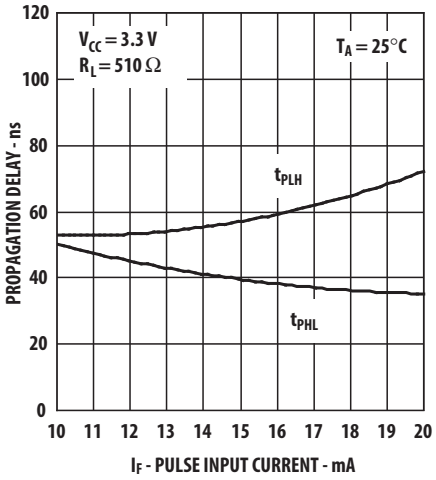


Figure 6: Propagation Delay vs. Temperature

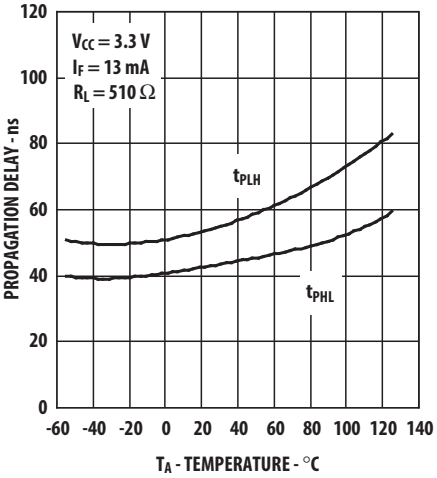


Figure 7: Test Circuit for Common Mode Transient Immunity and Typical Waveforms

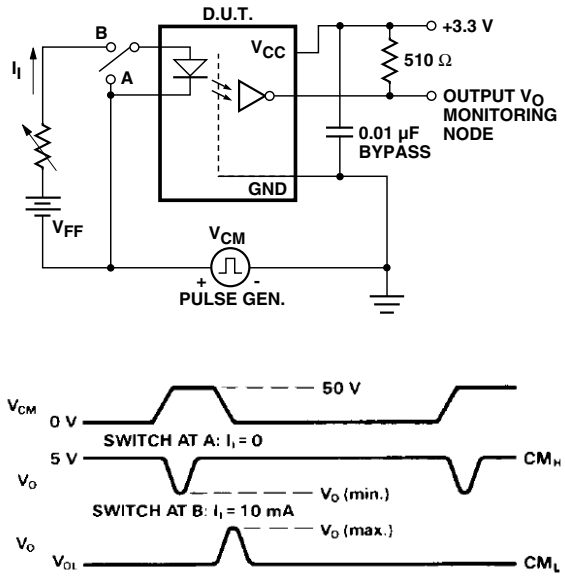


Figure 8: Test Circuit for t_{EHL} and t_{ELH}

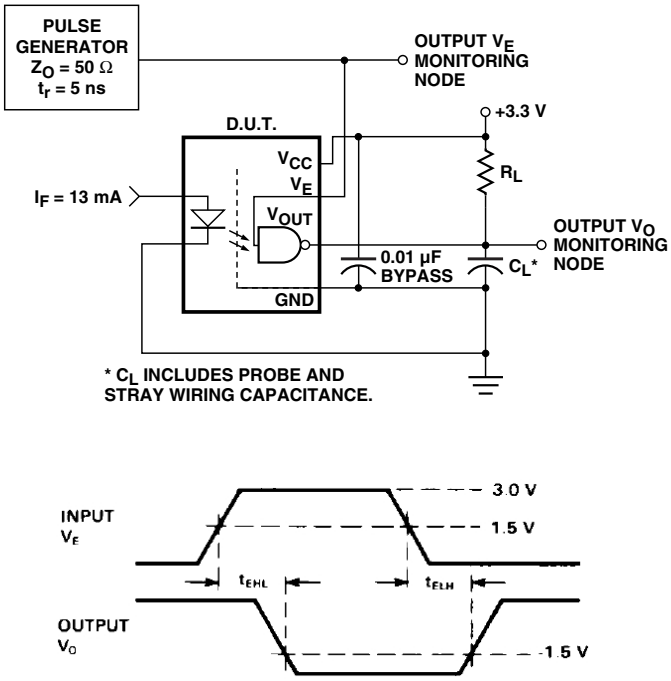


Figure 9: Enable Propagation Delay vs. Temperature

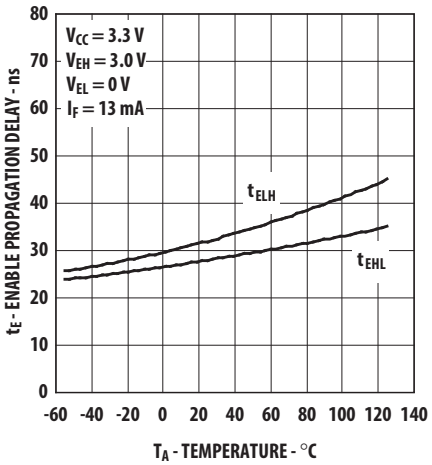
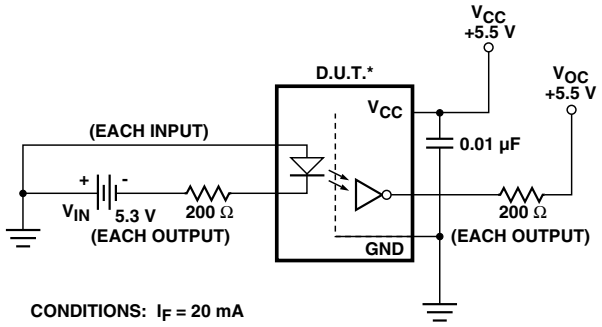


Figure 10: Operating Circuit for Burn-In and Steady State Life Tests



CONDITIONS: I_F = 20 mA
I_O = 25 mA

T_A = +125 °C

*** ALL CHANNELS TESTED SIMULTANEOUSLY.**