

## Description

The 5PB11xx is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50fs RMS.

There are five different fan-out variations available: 1:2 to 1:10.

The 5PB11xx supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8V to 3.3V supply.

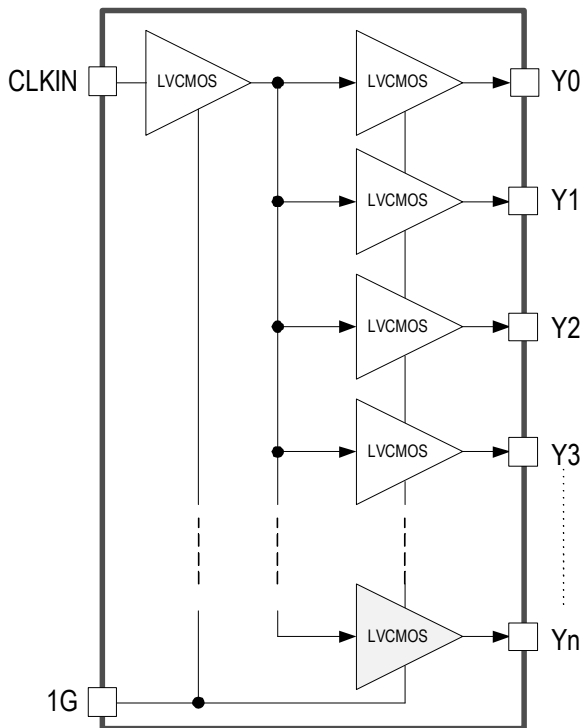
## Typical Applications

- Industrial applications
- Automotive:
  - Radar, Lidar, and other applications

## Features

- High-performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew: < 50ps
- Very low additive jitter: < 50fs
- Supply voltage: 1.8V to 3.3V
- 3.3V tolerant input clock
- $f_{MAX} = 200\text{MHz}$
- Integrated serial termination for 50Ω channel
- Packaged in 8-, 14-, 16-, 20-pin TSSOP and as small as 2 × 2 mm DFN and 3 × 3 mm VFQFPN packages
- Industrial (-40°C to +85°C) and extended (-40°C to +105°C) temperature ranges
- 5PB1104 available in AEC-Q100 qualified, Automotive Grade 1 (-40°C to +125°C)
- 5PB1110 available in AEC-Q100 qualified, Automotive Grade 2 (-40°C to +105°C)

## Block Diagram



## Contents

Description	1
Typical Applications	1
Features	1
Block Diagram	1
Pin Assignments – TSSOP Packages	3
Pin Descriptions – TSSOP Packages	3
Pin Assignments – DFN/VFQFPN Packages	4
Pin Descriptions – DFN/VFQFPN Packages	4
Output Logic Table	5
Absolute Maximum Ratings	5
Recommended Operating Conditions	5
Thermal Characteristics	6
DC Electrical Characteristics	7
AC Electrical Characteristics	13
Phase Noise Plots	19
Test Load and Circuit	20
Package Outline Drawings	20
Marking Diagrams (Industrial)	20
Marking Diagrams (Extended)	21
Marking Diagrams (Automotive)	21
Ordering Information (Industrial)	22
Ordering Information (Extended)	23
Ordering Information (Automotive)	23
Ordering Information (Special Material Request)	24
Revision History	24

## Pin Assignments – TSSOP Packages

Figure 1. Pin Assignments for TSSOP Packages

CLKIN	1	8	Y1	CLKIN	1	14	Y1	CLKIN	1	20	Y1
1G	2	7	NC	1G	2	13	Y3	1G	2	19	Y3
Y0	3	6	VDD	Y0	3	12	VDD	Y0	3	18	VDD
GND	4	5	NC	GND	4	11	Y2	GND	4	17	Y2
				VDD	5	10	GND	VDD	5	16	GND
				Y4	6	9	Y5	Y4	6	15	Y5
				GND	7	8	VDD	GND	7	14	VDD
								Y6	8	13	Y7
CLKIN	1	8	Y1	CLKIN	1	16	Y1	VDD	9	12	Y8
1G	2	7	Y3	1G	2	15	Y3	Y9	10	11	GND
Y0	3	6	VDD	Y0	3	14	VDD				
GND	4	5	Y2	GND	4	13	Y2				
				VDD	5	12	GND				
				Y4	6	11	Y5				
				GND	7	10	VDD				
				Y6	8	9	Y7				

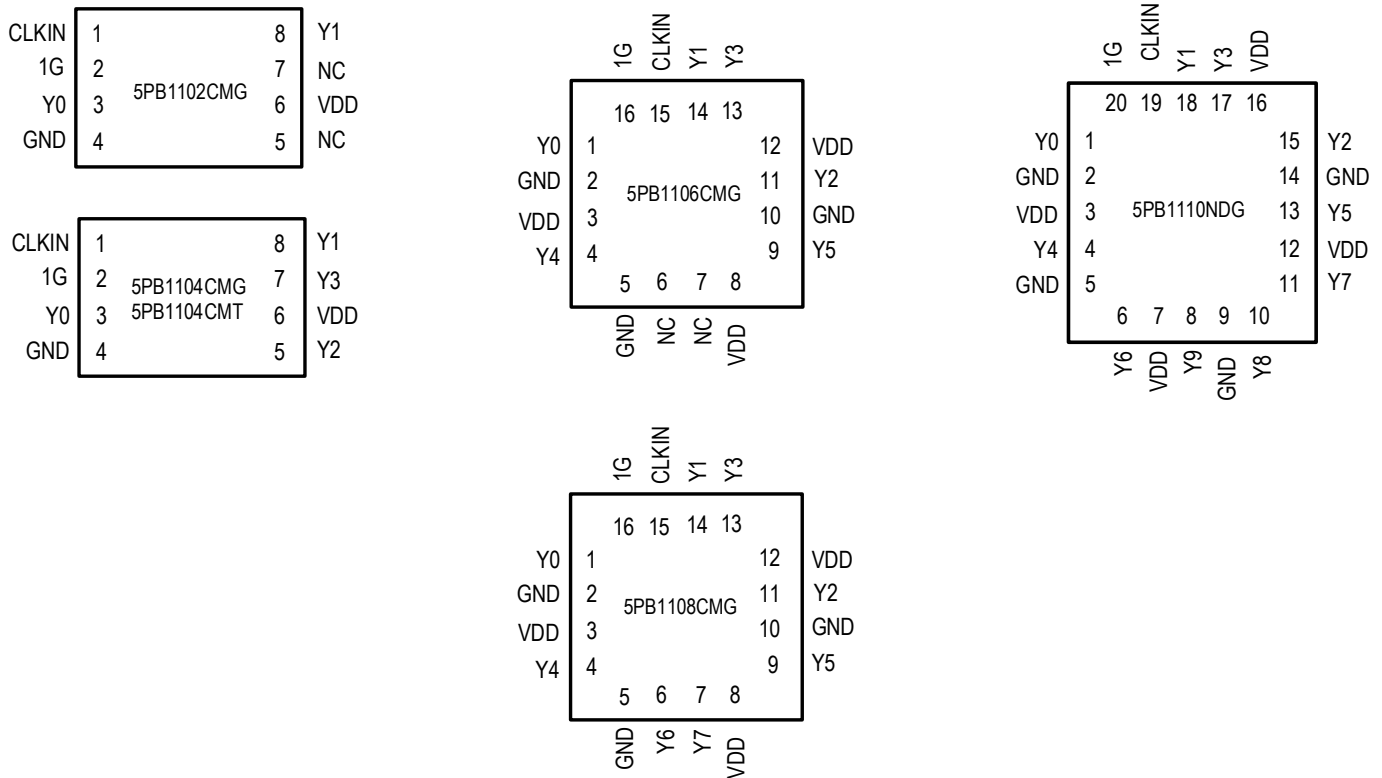
## Pin Descriptions – TSSOP Packages

Table 1. Pin Descriptions for TSSOP Packages

Device Number	LVC MOS Clock Input	Clock Output Enable	LVC MOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, ... Y9	V <sub>DD</sub>	GND
5PB1102PGG	1	2	3, 8	6	4
5PB1104PGG	1	2	3, 8, 5, 7	6	4
5PB1106PGG	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
5PB1108PGG	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12
5PB1110PGG	1	2	3, 20, 17, 19, 6, 15, 8, 13, 12, 10	5, 9, 14, 18	4, 7, 11, 16

## Pin Assignments – DFN/VFQFPN Packages

**Figure 2. Pin Assignments for DFN/QFN Packages**



## Pin Descriptions – DFN/VFQFPN Packages

**Table 2. Pin Descriptions for DFN/VFQFPN Packages**

Device Number	LVC MOS Clock Input	Clock Output Enable	LVC MOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, ... Y9	V <sub>DD</sub>	GND
5PB1102CMG	1	2	3, 8	6	4
5PB1104CMG 5PB1104CMT	1	2	3, 5, 7, 8	6	4
5PB1106CMG	15	16	1, 4, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1108CMG	15	16	1, 4, 6, 7, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1110NDG	19	20	1, 4, 6, 8, 10, 11, 13, 15, 17, 18	3, 7, 12, 16	2, 5, 9, 14

## Output Logic Table

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

After at least three cycles of input clock toggling. Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5PB11xx at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 3. Absolute Maximum Ratings**

Item	Rating
Supply Voltage, $V_{DD}$	3.8V
Output Enable and All Outputs	-0.4 V to $V_{DD} + 0.5$ V
Input Voltage, CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (Industrial)	-40 to +85°C
Ambient Operating Temperature (Extended and Automotive Grade 2)	-40 to +105°C
Ambient Operating Temperature (Automotive Grade 1)	-40 to +125°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

## Recommended Operating Conditions

**Table 4. Recommended Operating Conditions**

Parameter	Minimum	Typical	Maximum	Units
Ambient Operating Temperature (Industrial)	-40		+85	°C
Ambient Operating Temperature (Extended and Automotive Grade 2)	-40		+105	
Ambient Operating Temperature (Automotive Grade 1)	-40		+125	
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

## Thermal Characteristics

**Table 5. Thermal Characteristics**

Package	Applies to	$\theta_{JA}$	$\theta_{JC}$	$\theta_{JB}$	Units
8-TSSOP	5PB1102PGG, 5PB1104PGG	122.0	58.2	139.3	°C/W; still air
14-TSSOP	5PB1106PGG	84.5	44.2	64.5	°C/W; still air
16-TSSOP	5PB1108PGG	80.9	43.3	60.1	°C/W; still air
20-TSSOP	5PB1110PGG	72.5	37.9	49.8	°C/W; still air
8-DFN	5PB1102CMG, 5PB1104CMG 5PB1104CMT	120.2	99.4	63.3	°C/W; still air
16-VFQFPN	5PB1106CMG, 5PB1108CMG	115.6	83.1	61.8	°C/W; still air
20-VFQFPN	5PB1110NDG	49.6	94.7	5.1	°C/W; still air

## DC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, \text{ or } 3.3V$  (see tables below)

**Table 6. DC Electrical Characteristics –  $V_{DD} = 1.8V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units	
$V_{DD}$	Operating Voltage	Industrial and Extended <sup>[2]</sup>		1.71	1.8	1.89	V	
$V_{IH}$	Input High Voltage, CLKIN <sup>[1]</sup>		$0.7 \times V_{DD}$				V	
$V_{IL}$	Input Low Voltage, CLKIN <sup>[1]</sup>					$0.3 \times V_{DD}$	V	
$V_{IH}$	Input High Voltage, 1G		1.6			$V_{DD}$	V	
$V_{IL}$	Input Low Voltage, 1G					0.6	V	
$V_{OH}$	Output High Voltage		$I_{OH} = -5mA.$	1.4			V	
$V_{OL}$	Output Low Voltage		$I_{OL} = 5mA.$			0.4	V	
$Z_O$	Nominal Output Impedance					50	$\Omega$	
$C_{IN}$	Input Capacitance		CLKIN, 1G pin.			5	pF	
$I_{DD}$	Operating Supply Current, 5PB1102		100MHz, no load, 25°C.			6	8	mA
	Operating Supply Current, 5PB1104					12	13	
	Operating Supply Current, 5PB1106					15	18	
	Operating Supply Current, 5PB1108					20	23	
	Operating Supply Current, 5PB1110					23	27	
$I_{IH}$	Input High Leakage	$V_{IN} = V_{DD}$				5	$\mu A$	
$I_{IL}$	Input Low Leakage	$V_{IN} = 0V$				5	$\mu A$	

<sup>[1]</sup> Nominal switching threshold is  $V_{DD}/2$ .

<sup>[2]</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

**Table 7. DC Electrical Characteristics –  $V_{DD} = 1.8V \pm 5\%$ , Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Operating Voltage	Automotive [2][3]		1.71	1.8	1.89	V
$V_{IH}$	Input High Voltage, CLKIN [1]		$0.7 \times V_{DD}$				V
$V_{IL}$	Input Low Voltage, CLKIN [1]					$0.3 \times V_{DD}$	V
$V_{IH}$	Input High Voltage, 1G		1.6			$V_{DD}$	V
$V_{IL}$	Input Low Voltage, 1G					0.6	V
$V_{OH}$	Output High Voltage		$I_{OH} = -5mA.$	1.2			V
$V_{OL}$	Output Low Voltage		$I_{OL} = 5mA.$			0.45	V
$Z_O$	Nominal Output Impedance					50	$\Omega$
$C_{IN}$	Input Capacitance			CLKIN, 1G pin.		5	
$I_{DD}$	Operating Supply Current	5PB1104 [2]	0.001MHz, $C_L = 5pF.$		0.7	1	mA
			0.008MHz, $C_L = 5pF.$		0.7	1	
			40MHz, $C_L = 5pF.$		11	13	
			100MHz, $C_L = 5pF.$		25	30	
			156.25MHz, $C_L = 5pF.$		37	47	
			200MHz, $C_L = 5pF.$		39	57	
$I_{DD}$	Operating Supply Current	5PB1110 [3]	0.001MHz, $C_L = 5pF.$		4.1	6.7	mA
			0.008MHz, $C_L = 5pF.$		4.2	6.7	
			40MHz, $C_L = 5pF.$		30	45	
			100MHz, $C_L = 5pF.$		65	82	
			156.25MHz, $C_L = 5pF.$		91	123	
			200MHz, $C_L = 5pF.$		96	137	
$I_{IH}$	Input High Leakage	Automotive [2][3]	$V_{IN} = V_{DD}$			5	$\mu A$
$I_{IL}$	Input Low Leakage		$V_{IN} = 0V$			5	$\mu A$

[1] Nominal switching threshold is  $V_{DD}/2$ .

[2] 5PB1104CMG1 and 5PB1104CMT1  $T_A = -40^\circ C$  to  $+125^\circ C$  unless stated otherwise.

[3] 5PB1110NDG2  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.



**Table 8. DC Electrical Characteristics –  $V_{DD} = 2.5V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units	
$V_{DD}$	Operating Voltage	Industrial and Extended <sup>[2]</sup>		2.375	2.5	2.625	V	
$V_{IH}$	Input High Voltage, CLKIN <sup>[1]</sup>			$0.7 \times V_{DD}$			V	
$V_{IL}$	Input Low Voltage, CLKIN <sup>[1]</sup>					$0.3 \times V_{DD}$	V	
$V_{IH}$	Input High Voltage, 1G			1.8		$V_{DD}$	V	
$V_{IL}$	Input Low Voltage, 1G					0.7	V	
$V_{OH}$	Output High Voltage		$I_{OH} = -8mA.$	1.9			V	
$V_{OL}$	Output Low Voltage		$I_{OL} = 8mA.$			0.5	V	
$Z_O$	Nominal Output Impedance					50	$\Omega$	
$C_{IN}$	Input Capacitance		CLKIN, 1G pin.			5	pF	
$I_{DD}$	Operating Supply Current, 5PB1102		100MHz, no load, 25°C.			9	11	mA
	Operating Supply Current, 5PB1104					15	18	
	Operating Supply Current, 5PB1106					21	24	
	Operating Supply Current, 5PB1108					27	31	
	Operating Supply Current, 5PB1110					32	37	
$I_{IH}$	Input High Leakage		$V_{IN} = V_{DD}$			5	$\mu A$	
$I_{IL}$	Input Low Leakage		$V_{IN} = 0V$			5	$\mu A$	

<sup>[1]</sup> Nominal switching threshold is  $V_{DD}/2$ .

<sup>[2]</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

**Table 9. DC Electrical Characteristics –  $V_{DD} = 2.5V \pm 5\%$ , Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Operating Voltage	Automotive [2][3]		2.375	2.5	2.625	V
$V_{IH}$	Input High Voltage, CLKIN [1]		$0.7 \times V_{DD}$				V
$V_{IL}$	Input Low Voltage, CLKIN [1]					$0.3 \times V_{DD}$	V
$V_{IH}$	Input High Voltage, 1G		1.8		$V_{DD}$		V
$V_{IL}$	Input Low Voltage, 1G					0.7	V
$V_{OH}$	Output High Voltage		$I_{OH} = -8mA.$	1.6			V
$V_{OL}$	Output Low Voltage		$I_{OL} = 8mA.$			0.625	V
$Z_O$	Nominal Output Impedance					50	$\Omega$
$C_{IN}$	Input Capacitance			CLKIN, 1G pin.		5	
$I_{DD}$	Operating Supply Current	5PB1104 [2]	0.001MHz, $C_L = 5pF.$		0.9	1.3	mA
			0.008MHz, $C_L = 5pF.$		0.9	1.3	
			40MHz, $C_L = 5pF.$		15	17	
			100MHz, $C_L = 5pF.$		35	42	
			156.25MHz, $C_L = 5pF.$		52	67	
			200MHz, $C_L = 5pF.$		56	80	
$I_{DD}$	Operating Supply Current	5PB1110 [3]	0.001MHz, $C_L = 5pF.$		5.4	8.2	mA
			0.008MHz, $C_L = 5pF.$		5.4	8.2	
			40MHz, $C_L = 5pF.$		41	61	
			100MHz, $C_L = 5pF.$		91	116	
			156.25MHz, $C_L = 5pF.$		129	169	
			200MHz, $C_L = 5pF.$		140	195	
$I_{IH}$	Input High Leakage	Automotive [2][3]	$V_{IN} = V_{DD}$			5	$\mu A$
$I_{IL}$	Input Low Leakage		$V_{IN} = 0V$			5	$\mu A$

[1] Nominal switching threshold is  $V_{DD}/2$ .

[2] 5PB1104CMG1 and 5PB1104CMT1  $T_A = -40^\circ C$  to  $+125^\circ C$  unless stated otherwise.

[3] 5PB1110NDG2  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

**Table 10. DC Electrical Characteristics –  $V_{DD} = 3.3V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units	
$V_{DD}$	Operating Voltage	Industrial and Extended <sup>[2]</sup>		3.135	3.3	3.465	V	
$V_{IH}$	Input High Voltage, CLKIN <sup>[1]</sup>			$0.7 \times V_{DD}$			V	
$V_{IL}$	Input Low Voltage, CLKIN <sup>[1]</sup>					$0.3 \times V_{DD}$	V	
$V_{IH}$	Input High Voltage, 1G			2.0		$V_{DD}$	V	
$V_{IL}$	Input Low Voltage, 1G					0.8	V	
$V_{OH}$	Output High Voltage		$I_{OH} = -12mA.$	2.4			V	
$V_{OL}$	Output Low Voltage		$I_{OL} = 12mA.$			0.7	V	
$Z_O$	Nominal Output Impedance					50	$\Omega$	
$C_{IN}$	Input Capacitance		CLKIN, 1G pin.			5	pF	
$I_{DD}$	Operating Supply Current, 5PB1102		100MHz, no load, 25°C.			12	13	mA
	Operating Supply Current, 5PB1104					20	22	
	Operating Supply Current, 5PB1106					25	30	
	Operating Supply Current, 5PB1108					35	38	
	Operating Supply Current, 5PB1110					40	45	
$I_{IH}$	Input High Leakage		$V_{IN} = V_{DD}$			5	$\mu A$	
$I_{IL}$	Input Low Leakage		$V_{IN} = 0V$			5	$\mu A$	

<sup>[1]</sup> Nominal switching threshold is  $V_{DD}/2$ .

<sup>[2]</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

**Table 11. DC Electrical Characteristics –  $V_{DD} = 3.3V \pm 5\%$ , Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Operating Voltage	Automotive [2][3]		3.135	3.3	3.465	V
$V_{IH}$	Input High Voltage, CLKIN [1]		$0.7 \times V_{DD}$				V
$V_{IL}$	Input Low Voltage, CLKIN [1]		$0.3 \times V_{DD}$				V
$V_{IH}$	Input High Voltage, 1G		2.1		$V_{DD}$		V
$V_{IL}$	Input Low Voltage, 1G					08	V
$V_{OH}$	Output High Voltage		$I_{OH} = -12mA.$		2.1		
$V_{OL}$	Output Low Voltage	5PB1104 [2]	$I_{OL} = 12mA.$			0.825	V
		5PB1110 [3]	$I_{OL} = 12mA.$			0.850	V
$Z_O$	Nominal Output Impedance	Automotive [2][3]			50		$\Omega$
$C_{IN}$	Input Capacitance		CLKIN, 1G pin.		5		pF
$I_{DD}$	Operating Supply Current	5PB1104 [2]	0.001MHz, $C_L = 5pF.$		1.2	1.7	mA
			0.008MHz, $C_L = 5pF.$		1.2	1.7	
			40MHz, $C_L = 5pF.$		19	22	
			100MHz, $C_L = 5pF.$		45	54	
			156.25MHz, $C_L = 5pF.$		67	87	
			200MHz, $C_L = 5pF.$		75	107	
$I_{DD}$	Operating Supply Current	5PB1110 [3]	0.001MHz, $C_L = 5pF.$		7.2	10.2	mA
			0.008MHz, $C_L = 5pF.$		7.2	10.2	
			40MHz, $C_L = 5pF.$		52	67	
			100MHz, $C_L = 5pF.$		117	147	
			156.25MHz, $C_L = 5pF.$		168	234	
			200MHz, $C_L = 5pF.$		186	256	
$I_{IH}$	Input High Leakage	Automotive [2][3]	$V_{IN} = V_{DD}$			5	$\mu A$
$I_{IL}$	Input Low Leakage		$V_{IN} = 0V$			5	$\mu A$

[1] Nominal switching threshold is  $V_{DD}/2$ .

[2] 5PB1104CMG1 and 5PB1104CMT1  $T_A = -40^\circ C$  to  $+125^\circ C$  unless stated otherwise.

[3] 5PB1110NDG2  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

## AC Electrical Characteristics

$V_{DD} = 1.8V, 2.5V, \text{ or } 3.3V$  (see tables below).

**Table 12. AC Electrical Characteristics –  $V_{DD} = 1.8V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Industrial and Extended <sup>[1]</sup>		0		200	MHz
$t_{OR}$	Output Rise Time (2pF load)		0.36V to 1.44V, $C_L = 2pF$ .		0.5	0.75	ns
$t_{OF}$	Output Fall Time (2pF load)		1.44V to 0.36V, $C_L = 2pF$ .		0.5	0.75	ns
$t_{OR}$	Output Rise Time (5pF load)		0.36V to 1.44V, $C_L = 5pF$ .		0.8	1.0	ns
$t_{OF}$	Output Fall Time (5pF load)		1.44V to 0.36V, $C_L = 5pF$ .		0.8	1.0	ns
$t_{START-UP}$	Start-up Time		Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3	ms
$t_{PD}$	Propagation Delay <sup>[2]</sup>			1.5		2.5	ns
	Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz–20MHz.			0.05	ps
	Output to Output Skew, 5PB1102/04		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	50	ps
	Output to Output Skew, 5PB1106		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	58	ps
	Output to Output Skew, 5PB1108/10		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		45	65	ps
	Device to Device Skew		Rising edges at $V_{DD}/2$ .			200	ps
$t_{EN}$	Output Enable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DIS}$	Output Disable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DC}$	Duty Cycle <sup>[4]</sup>			50		%	

<sup>1</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when  $V_{IH}$  on CLKIN pin equals  $V_{DD}$  power supply voltage. Consult Renesas for tight duty cycle clock generators.

**Table 13. AC Electrical Characteristics –  $V_{DD} = 1.8V \pm 5\%$ , Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Automotive [1][5]		0		200	MHz
$t_{OR}$	Output Rise Time (5pF load)		0.36V to 1.44V, $C_L = 5pF$ .		0.65	1.2	ns
$t_{OF}$	Output Fall Time (5pF load)	5PB1104[1]	1.44V to 0.36V, $C_L = 5pF$ .		0.65	1.2	ns
		5PB1110[5]	1.44V to 0.36V, $C_L = 5pF$ .		0.65	1.25	ns
$t_{START-UP}$	Start-up Time	5PB1104[1]	Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3	ms
		5PB1110[5]	Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3.2	ms
$t_{PD}$	Propagation Delay [2]	5PB1104[1]		1.0		3.4	ns
		5PB1110[5]		1.0		4.0	ns
	Buffer Additive Phase Jitter, RMS	5PB1104[1]	156.25MHz, Integration Range: 12kHz–20MHz.			0.06	ps
		5PB1110[5]	156.25MHz, Integration Range: 12kHz–20MHz.			0.068	ps
	Output to Output Skew	Automotive [1][5]	Rising edges at $V_{DD}/2$ . [3]		35	87	ps
	Device to Device Skew		Rising edges at $V_{DD}/2$ .			200	ps
$t_{EN}$	Output Enable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DIS}$	Output Disable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DC}$	Duty Cycle [4]					50	%

<sup>1</sup> 5PB1104CMG1 and 5PB1104CMT1  $T_A = -40^\circ C$  to  $+125^\circ C$  unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when  $V_{IH}$  on CLKIN pin equals  $V_{DD}$  power supply voltage. Consult Renesas for tight duty cycle clock generators.

<sup>5</sup> 5PB1110NDG2  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

**Table 14. AC Electrical Characteristics –  $V_{DD} = 2.5V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Industrial and Extended <sup>[1]</sup>		0		200	MHz
$t_{OR}$	Output Rise Time (2pF load)		0.5V to 2.0V, $C_L = 2pF$ .		0.4	0.7	ns
$t_{OF}$	Output Fall Time (2pF load)		2.0V to 0.5V, $C_L = 2pF$ .		0.4	0.7	ns
$t_{OR}$	Output Rise Time (5pF load)		0.5V to 2.0V, $C_L = 5pF$ .		0.75	1.0	ns
$t_{OF}$	Output Fall Time (5pF load)		2.0V to 0.5V, $C_L = 5pF$ .		0.75	1.0	ns
$t_{START-UP}$	Start-up Time		Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3	ms
$t_{PD}$	Propagation Delay, 5PB1102/04 <sup>[2]</sup>			1.9		2.9	ns
	Propagation Delay, 5PB1106/08 <sup>[2]</sup>			2.0		3.3	ns
	Propagation Delay, 5PB1110 <sup>[2]</sup>			2.0		3.0	ns
	Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz–20MHz.			0.05	ps
	Output to Output Skew, 5PB1102/04		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	50	ps
	Output to Output Skew, 5PB1106		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	58	ps
	Output to Output Skew, 5PB1108/10		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		45	65	ps
	Device to Device Skew		Rising edges at $V_{DD}/2$ .			200	ps
$t_{EN}$	Output Enable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DIS}$	Output Disable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DC}$	Duty Cycle <sup>[4]</sup>			50		%	

<sup>1</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when  $V_{IH}$  on CLKIN pin equals  $V_{DD}$  power supply voltage. Consult Renesas for tight duty cycle clock generators.

**Table 15. AC Electrical Characteristics – V<sub>DD</sub> = 2.5V ±5%, Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Automotive <sup>[1][5]</sup>		0		200	MHz
t <sub>OR</sub>	Output Rise Time (5pF load)		0.5V to 2.0V, C <sub>L</sub> = 5pF.		0.63	1.2	ns
t <sub>OF</sub>	Output Fall Time (5pF load)		2.0V to 0.5V, C <sub>L</sub> = 5pF.		0.63	1.2	ns
t <sub>START-UP</sub>	Start-up Time		Part start-up time for valid outputs after V <sub>DD</sub> ramp-up.			3	ms
t <sub>PD</sub>	Propagation Delay <sup>[2]</sup>	5PB1104 <sup>[1]</sup>		1.0		4.5	ns
		5PB1110 <sup>[5]</sup>				4.75	ns
	Buffer Additive Phase Jitter, RMS	5PB1104 <sup>[1]</sup>	156.25MHz, Integration Range: 12kHz–20MHz.			0.06	ps
		5PB1110 <sup>[5]</sup>	156.25MHz, Integration Range: 12kHz–20MHz.			0.065	ps
	Output to Output Skew	Automotive <sup>[1][5]</sup>	Rising edges at V <sub>DD</sub> /2. <sup>[3]</sup>		35	87	ps
	Device to Device Skew		Rising edges at V <sub>DD</sub> /2.			200	ps
t <sub>EN</sub>	Output Enable Time		C <sub>L</sub> ≤ 5pF.			3	cycles
t <sub>DIS</sub>	Output Disable Time		C <sub>L</sub> ≤ 5pF.			3	cycles
t <sub>DC</sub>	Duty Cycle <sup>[4]</sup>					50	%

<sup>1</sup> 5PB1104CMG1 and 5PB1104CMT1 T<sub>A</sub> = -40°C to +125°C unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when VIH on CLKIN pin equals VDD power supply voltage. Consult Renesas for tight duty cycle clock generators.

<sup>5</sup> 5PB1110NDG2 T<sub>A</sub> = -40°C to +105°C unless stated otherwise.



**Table 16. AC Electrical Characteristics –  $V_{DD} = 3.3V \pm 5\%$ , Industrial and Extended**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Industrial and Extended <sup>[1]</sup>		0		200	MHz
$t_{OR}$	Output Rise Time (2pF load)		0.66V to 2.64V, $C_L = 2pF$ .		0.45	0.6	ns
$t_{OF}$	Output Fall Time (2pF load)		2.64V to 0.66V, $C_L = 2pF$ .		0.45	0.6	ns
$t_{OR}$	Output Rise Time (5pF load)		0.66V to 2.64V, $C_L = 5pF$ .		0.7	1.0	ns
$t_{OF}$	Output Fall Time (5pF load)		2.64V to 0.66V, $C_L = 5pF$ .		0.7	1.0	ns
$t_{START-UP}$	Start-up Time		Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3	ms
$t_{PD}$	Propagation Delay, 5PB1102/04 <sup>[2]</sup>			1.7		2.4	ns
	Propagation Delay, 5PB1106/08 <sup>[2]</sup>			1.7		2.7	ns
	Propagation Delay, 5PB1110 <sup>[2]</sup>			1.7		2.5	ns
	Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz–20MHz.			0.05	ps
	Output to Output Skew, 5PB1102/04		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	50	ps
	Output to Output Skew, 5PB1106		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	58	ps
	Output to Output Skew, 5PB1108/10		Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		45	65	ps
	Device to Device Skew		Rising edges at $V_{DD}/2$ .			200	ps
$t_{EN}$	Output Enable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DIS}$	Output Disable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DC}$	Duty Cycle <sup>[4]</sup>			50		%	

<sup>1</sup> 5PB11xxPGGI, 5PB11xxPGGK, 5PB11xxCMGI, 5PB11xxCMGK.  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when  $V_{IH}$  on CLKIN pin equals  $V_{DD}$  power supply voltage. Consult Renesas for tight duty cycle clock generators.

**Table 17. AC Electrical Characteristics –  $V_{DD} = 3.3V \pm 5\%$ , Automotive**

Symbol	Parameter	Applies to	Conditions	Minimum	Typical	Maximum	Units
	Input Frequency	Automotive <sup>[1][5]</sup>		0		200	MHz
$t_{OR}$	Output Rise Time (5pF load)		0.66V to 2.64V, $C_L = 5pF$ .		0.61	1.2	ns
$t_{OF}$	Output Fall Time (5pF load)		2.64V to 0.66V, $C_L = 5pF$ .		0.61	1.2	ns
$t_{START-UP}$	Start-up Time		Part start-up time for valid outputs after $V_{DD}$ ramp-up.			3	ms
$t_{PD}$	Propagation Delay <sup>[2]</sup>	5PB1104 <sup>[1]</sup>		1.0		3.4	ns
		5PB1110 <sup>[5]</sup>		1.0		4.0	ns
	Buffer Additive Phase Jitter, RMS	5PB1104 <sup>[1]</sup>	156.25MHz, Integration Range: 12kHz–20MHz.			0.05	ps
		5PB1110 <sup>[5]</sup>	156.25MHz, Integration Range: 12kHz–20MHz.			0.065	ps
	Output to Output Skew	Automotive <sup>[1][5]</sup>	Rising edges at $V_{DD}/2$ . <sup>[3]</sup>		35	87	ps
	Device to Device Skew		Rising edges at $V_{DD}/2$ .			200	ps
$t_{EN}$	Output Enable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DIS}$	Output Disable Time		$C_L \leq 5pF$ .			3	cycles
$t_{DC}$	Duty Cycle <sup>[4]</sup>					50	%

<sup>1</sup> 5PB1104CMG1 and 5PB1104CMT1 only.  $T_A = -40^\circ C$  to  $+125^\circ C$  unless stated otherwise.

<sup>2</sup> With rail-to-rail input clock.

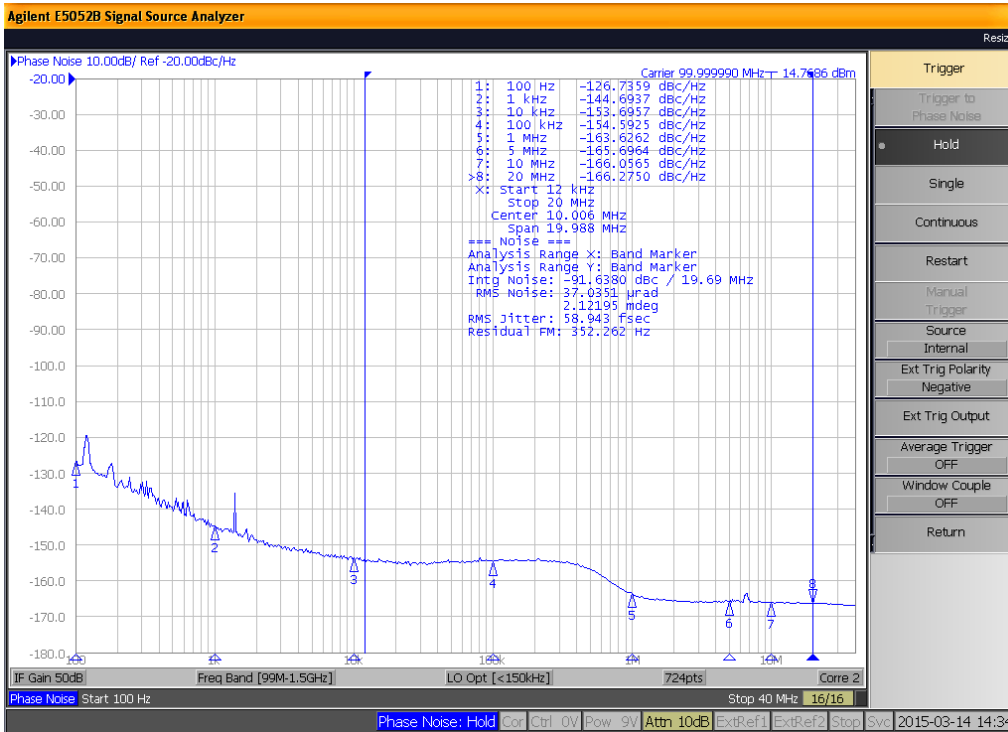
<sup>3</sup> Between any 2 outputs with equal loading.

<sup>4</sup> Duty cycle on outputs will match incoming clock duty cycle when  $V_{IH}$  on CLKIN pin equals  $V_{DD}$  power supply voltage. Consult Renesas for tight duty cycle clock generators.

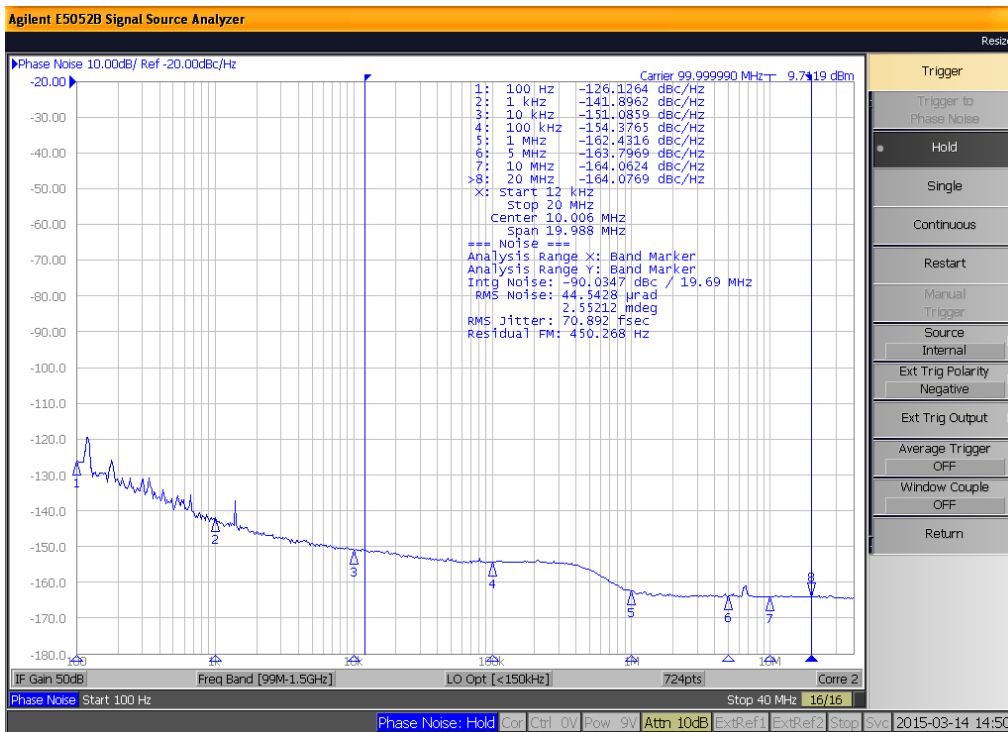
<sup>5</sup> 5PB1110NDG2  $T_A = -40^\circ C$  to  $+105^\circ C$  unless stated otherwise.

## Phase Noise Plots

The phase noise plots show the low additive jitter of the 5PB11xx high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB11xx has about 70.9fs of RMS phase jitter. This results in a low additive phase jitter of only 39fs.

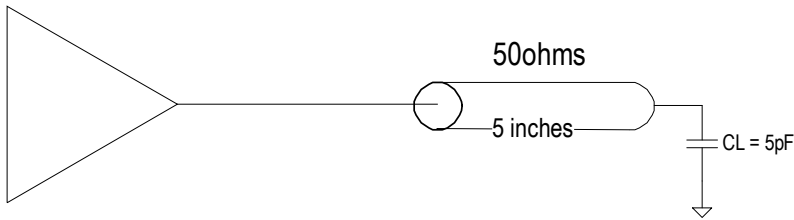


Reference Phase Noise 58.9fs (12kHz to 20MHz)



Output Phase Noise 70.9fs (12kHz to 20MHz)

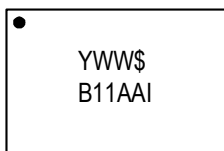
## Test Load and Circuit



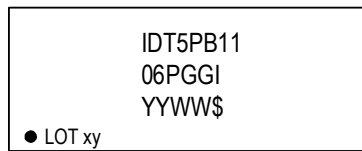
## Package Outline Drawings

The package outline drawings ([PGG8D1](#), [PGG14T1](#), [PGG16T1](#), [PGG20D1](#), [CMG8](#), [CMG16](#), [NDG20P2](#), [NDG20S2](#), [CMT8D1](#)) are appended at the end of this document. The package information is the most current data available.

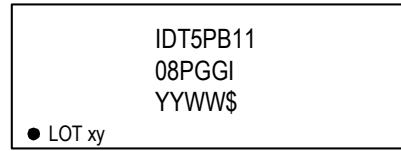
## Marking Diagrams (Industrial)



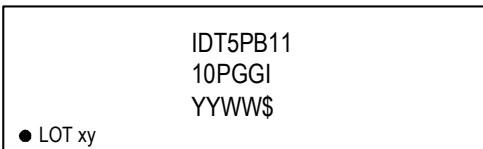
8-pin TSSOP



14-pin TSSOP



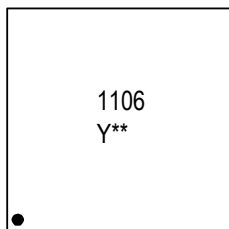
16-pin TSSOP



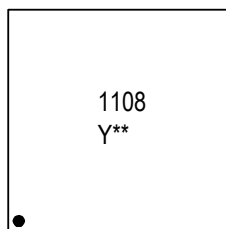
20-pin TSSOP



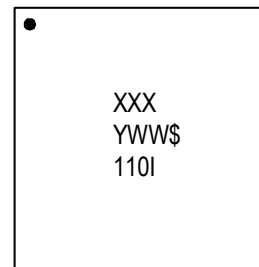
8-pin DFN



16-pin VFQFPN



16-pin VFQFPN



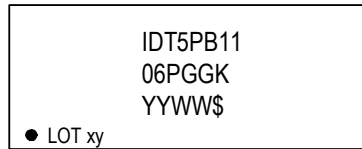
20-pin VFQFPN

- “AA” denotes the last two digits of the part number for 8-TSSOP and DFN (e.g. 02, 04).
- “\*\*” is the lot sequence.
- “XXX” denotes the last three characters of the Asm lot (20-VFQFPN only).
- “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and work week that the part was assembled.
- “\$” denotes the mark code.
- “G” after the two-letter package code denotes RoHS compliant package.
- “I” denotes industrial temperature range device.

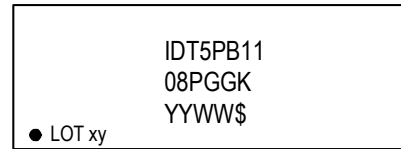
## Marking Diagrams (Extended)



8-pin TSSOP



14-pin TSSOP



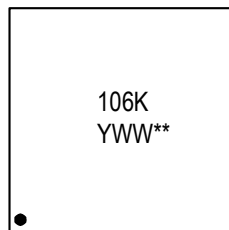
16-pin TSSOP



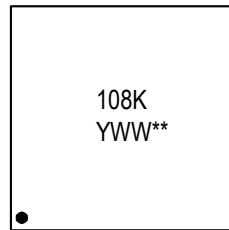
20-pin TSSOP



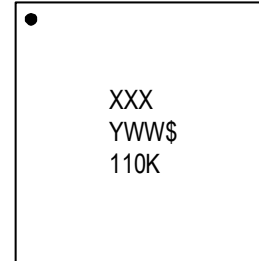
8-pin DFN



16-pin VFQFPN



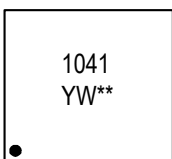
16-pin VFQFPN



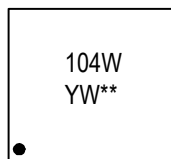
20-pin VFQFPN

- “AA” denotes the last two digits of the part number for 8-TSSOP and DFN (e.g. 02, 04).
- “\*\*” is the lot sequence.
- “XXX” denotes the last three characters of the Asm lot (20-VFQFPN only).
- “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and week that the part was assembled.
- “\$” denotes the mark code.
- “G” after the two-letter package code denotes RoHS compliant package.
- “K” denotes extended temperature range device.

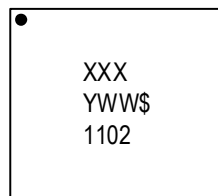
## Marking Diagrams (Automotive)



8-pin DFN



8-pin DFN (wetttable flank)



20-pin VFQFPN (wetttable flank)

- Line 1:
  - For 8-pin devices: truncated part number; last number is the temperature grade: 1 = Automotive Grade 1.
  - For 20-pin device: “XXX” denotes ASM lot number.
- Line 2:
  - “YW” or “YWW” is the last digit(s) of the year and work week that the part was assembled.
  - “\*\*” denotes the lot sequence number.
- “1102” on 20-pin device denotes truncated part number; last number is the temperature grade: 2 = Automotive Grade 2.

## Ordering Information (Industrial)

Orderable Part Number	Package	Carrier Type	Temperature
5PB1102PGGI	4.4mm body, <b>8-TSSOP</b>	Tubes	-40 to +85°C
5PB1102PGGI8		Tape and Reel	
5PB1104PGGI		Tubes	
5PB1104PGGI8		Tape and Reel	
5PB1106PGGI	4.4mm body, <b>14-TSSOP</b>	Tubes	
5PB1106PGGI8		Tape and Reel	
5PB1108PGGI	4.4mm body, <b>16-TSSOP</b>	Tubes	
5PB1108PGGI8		Tape and Reel	
5PB1110PGGI	4.4mm body, <b>20-TSSOP</b>	Tubes	
5PB1110PGGI8		Tape and Reel	
5PB1102CMGI	2.0 × 2.0 × 0.5 mm, <b>8-DFN</b>	Cut Tape	
5PB1102CMGI8		Tape and Reel	
5PB1104CMGI		Cut Tape	
5PB1104CMGI8		Tape and Reel	
5PB1104CMGI/W <sup>[a]</sup>		Tape and Reel	
5PB1106CMGI	2.5 × 2.5 × 0.5 mm, <b>16-VFQFPN</b>	Cut Tape	
5PB1106CMGI8		Tape and Reel	
5PB1108CMGI		Cut Tape	
5PB1108CMGI8		Tape and Reel	
5PB1110NDGI	3.0 × 3.0 × 0.90 mm, <b>20-VFQFPN</b>	Tubes	
5PB1110NDGI8		Tape and Reel	

[a] "/W" stands for tape and reel with pin 1 orientation: EIA-481-D. All other tape and reels options come with EIA-481-C pin 1 orientation.

## Ordering Information (Extended)

Orderable Part Number	Package	Carrier Type	Temperature
5PB1102PGGK	4.4mm body, <b>8-TSSOP</b>	Tubes	-40 to +105°C
5PB1102PGGK8		Tape and Reel	
5PB1104PGGK		Tubes	
5PB1104PGGK8		Tape and Reel	
5PB1106PGGK	4.4mm body, <b>14-TSSOP</b>	Tubes	
5PB1106PGGK8		Tape and Reel	
5PB1108PGGK	4.4mm body, <b>16-TSSOP</b>	Tubes	
5PB1108PGGK8		Tape and Reel	
5PB1110PGGK	4.4mm body, <b>20-TSSOP</b>	Tubes	
5PB1110PGGK8		Tape and Reel	
5PB1102CMGK	2.0 × 2.0 × 0.5 mm, <b>8-DFN</b>	Cut Tape	
5PB1102CMGK8		Tape and Reel	
5PB1104CMGK		Cut Tape	
5PB1104CMGK8		Tape and Reel	
5PB1104CMGK/W <sup>[a]</sup>		Tape and Reel	
5PB1106CMGK	2.5 × 2.5 × 0.5 mm, <b>16-VFQFPN</b>	Cut Tape	
5PB1106CMGK8		Tape and Reel	
5PB1108CMGK		Cut Tape	
5PB1108CMGK8		Tape and Reel	
5PB1110NDGK	3.0 × 3.0 × 0.90 mm, <b>20-VFQFPN</b>	Tubes	
5PB1110NDGK8		Tape and Reel	

[a] "/W" stands for tape and reel with pin 1 orientation: EIA-481-D. All other tape and reels options come with EIA-481-C pin 1 orientation.

## Ordering Information (Automotive)

Orderable Part Number	Package	Carrier Type	Temperature
5PB1104CMG1	2.0 × 2.0 × 0.5 mm, <b>8-DFN</b>	Cut Tape	-40° to +125°C
5PB1104CMG18		Tape and Reel	
5PB1104CMT1	2.0 × 2.0 × 0.5 mm, <b>8-DFN</b> , Wettable flank	Cut Tape	-40° to +125°C
5PB1104CMT18		Tape and Reel	
5PB1110NDG2	3.0 × 3.0 × 0.9 mm, <b>20-VFQFPN</b> , Wettable flank	Tube	-40° to +105°C
5PB1110NDG28		Tape and Reel	

## Ordering Information (Special Material Request)

For customers with a special material request, an alphanumeric code is assigned to the standard part number (see examples below). Contact Renesas for more information.

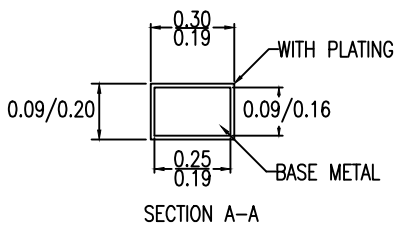
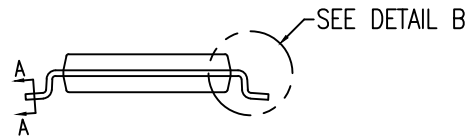
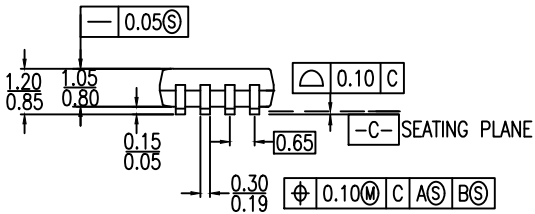
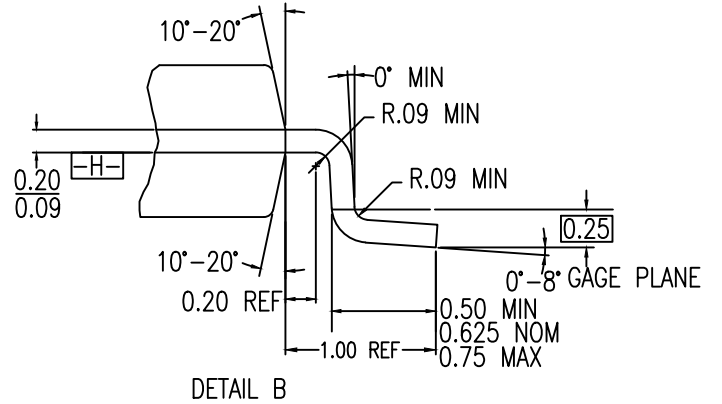
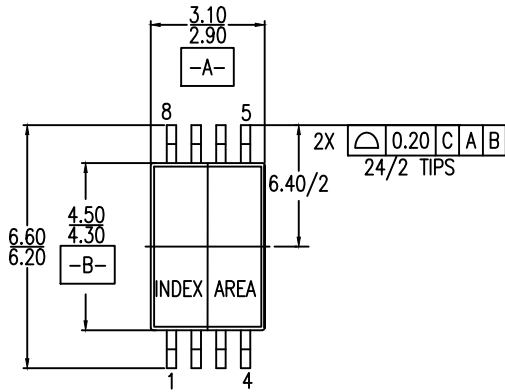
Standard Part Number Example	Special Material Request Part Number <sup>[a]</sup>
5PB1104CMGI	5PB1104CMGI/X
5PB1104CMGI8	5PB1104CMGI8/X

[a] "/X" is a code added to the standard part number when a customer has a special request for material. If no special material is requested, "/X" can be omitted.

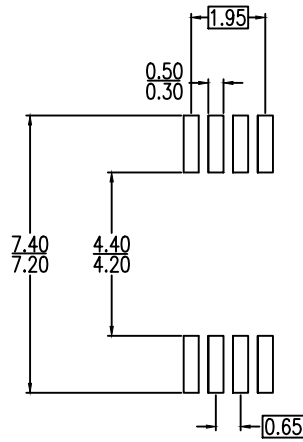
## Revision History

Revision Date	Description of Change
March 31, 2021	Added Ordering Information (Special Material Request) table.
March 11, 2021	Added 5PB1110NDG2 automotive device information.
January 5, 2021	Updated supply voltage pin numbers for 5PB1110PGG in TSSOP Pin Descriptions table.
December 2, 2020	<ul style="list-style-type: none"> <li>▪ Added 5PB1104CMG/W option to the ordering information (Extended) table.</li> <li>▪ Updated Package Outline Drawings links.</li> </ul>
September 29, 2020	Updated marking diagrams for 5PB1106/08/10PGGI and 5PB1106/08/10PGGK.
January 31, 2020	Rebranded the document as Renesas. No technical changes were made.
December 4, 2019	Added Input High and Low Leakage parameters to tables 6–11.
May 31, 2019	<ul style="list-style-type: none"> <li>▪ Added 5PB1104CMT1 wettable flank package information.</li> <li>▪ Updated Propagation Delay values for automotive.</li> </ul>
December 18, 2018	<ul style="list-style-type: none"> <li>▪ Updated <math>t_{PD}</math> and skew values.</li> <li>▪ Added 5PB1104CMG1 automotive part information.</li> </ul>
October 24, 2018	Initial release.





- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
  2. ALL DIMENSION ARE IN MM.

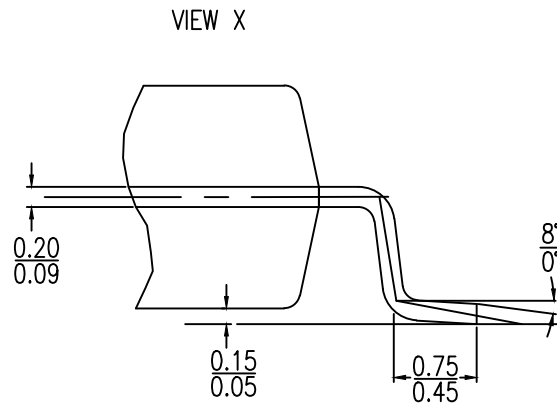
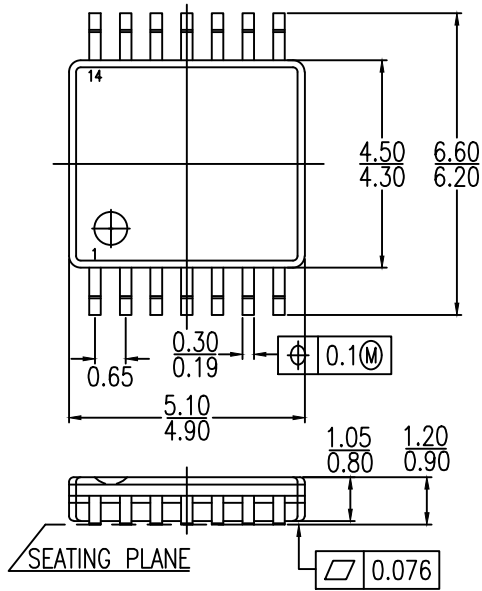


RECOMMENDED LAND PATTERN DIMENSIONS

NOTES:

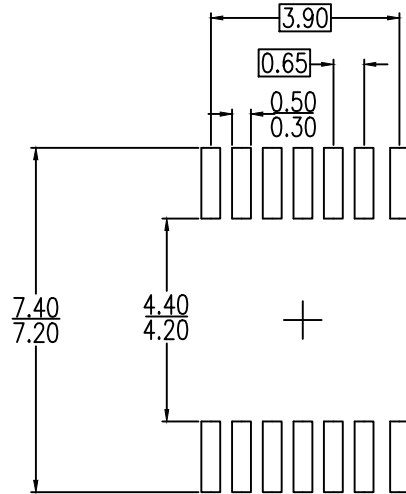
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 00	Initial Release



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

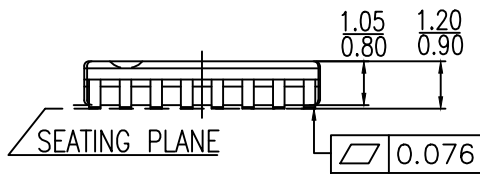
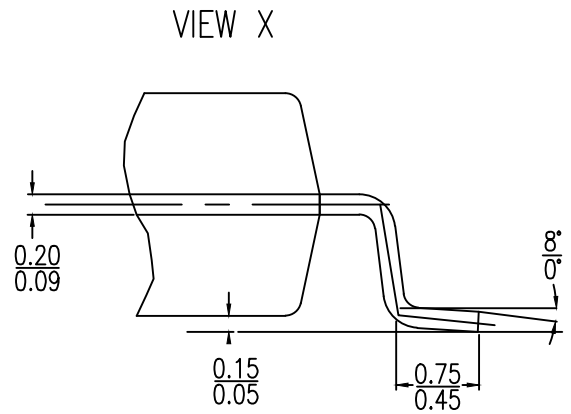
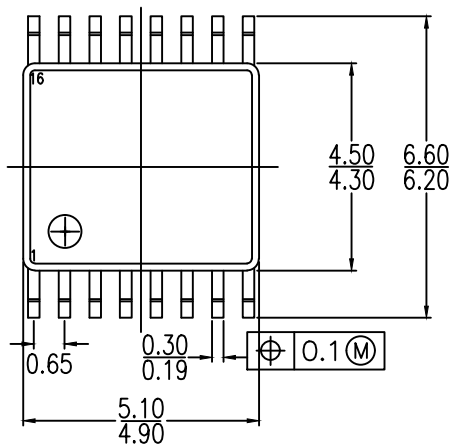


LAND PATTERN DIMENSIONS

NOTE:

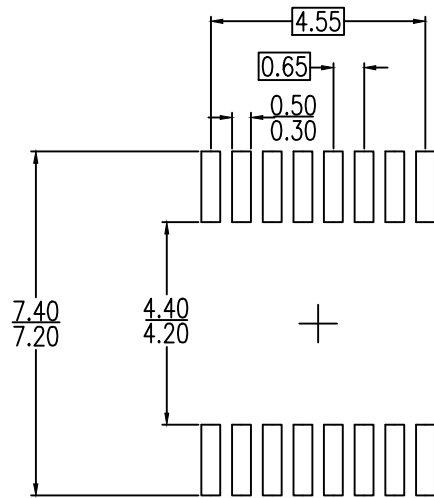
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Mar, 10 2017	Rev 01	Added Land Pattern
Dec, 19 2017	Rev 02	New Format



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

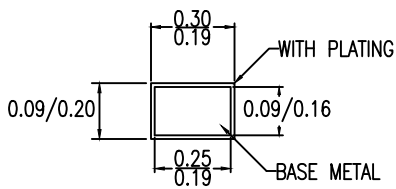
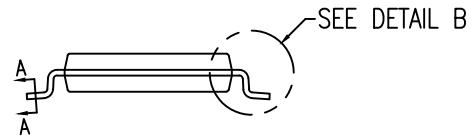
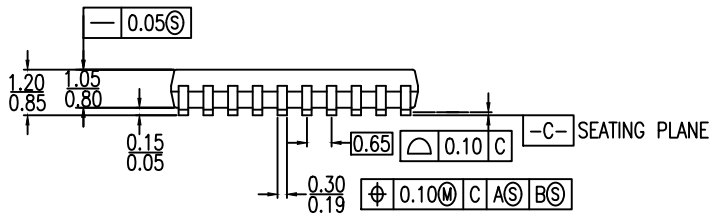
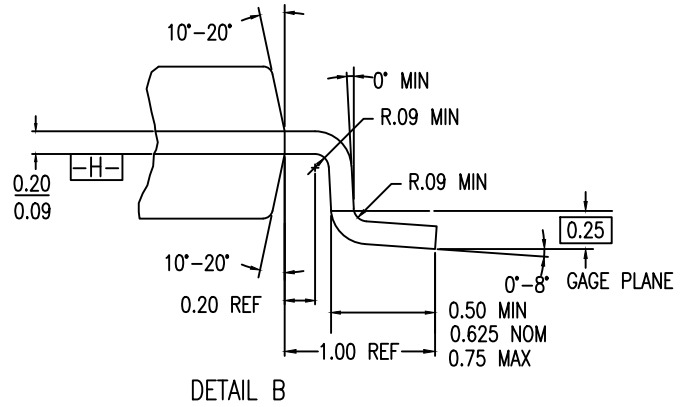
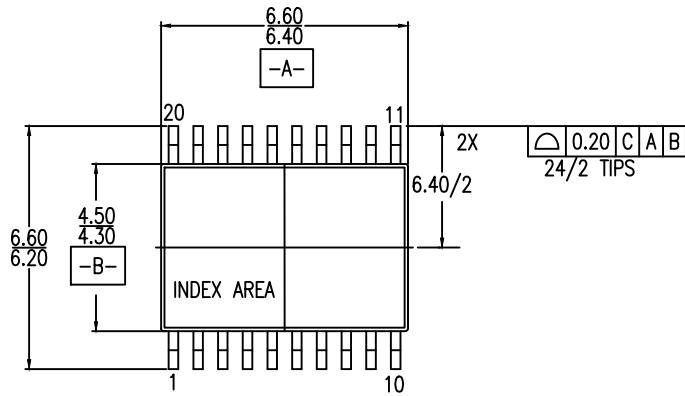


LAND PATTERN DIMENSIONS

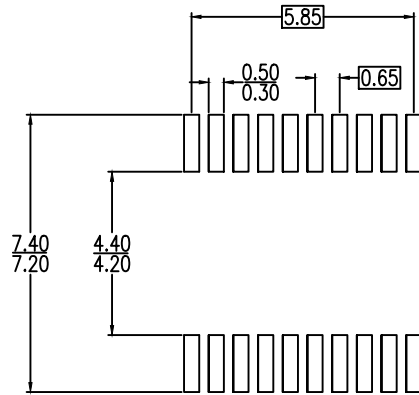
NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Jan 26, 2018	Rev 00	Revised from PSC-4056-02 PGG16



- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
  2. ALL DIMENSION ARE IN MM.



RECOMMENDED LAND PATTERN DIMENSIONS

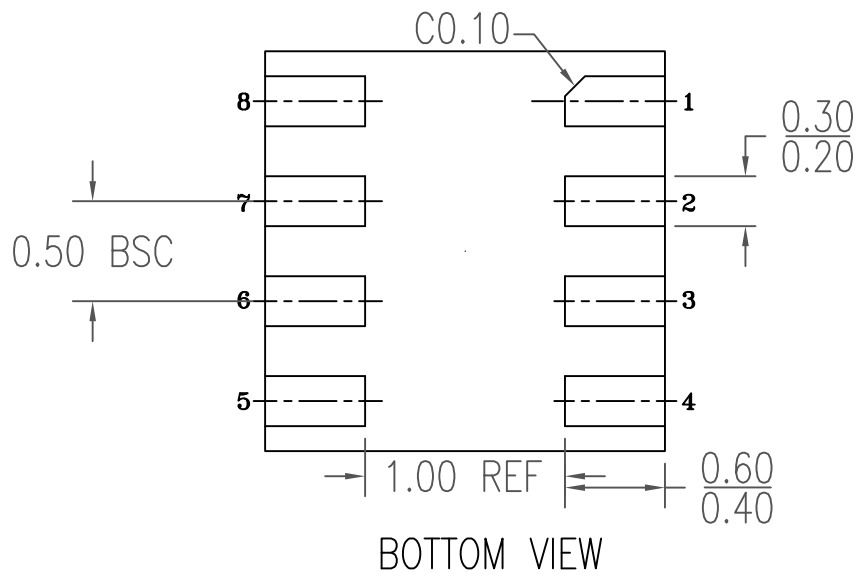
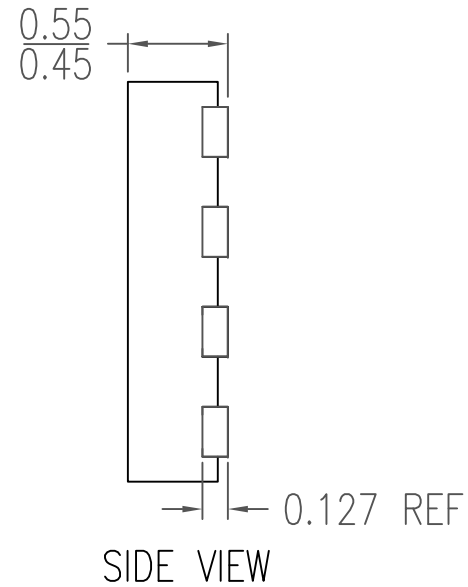
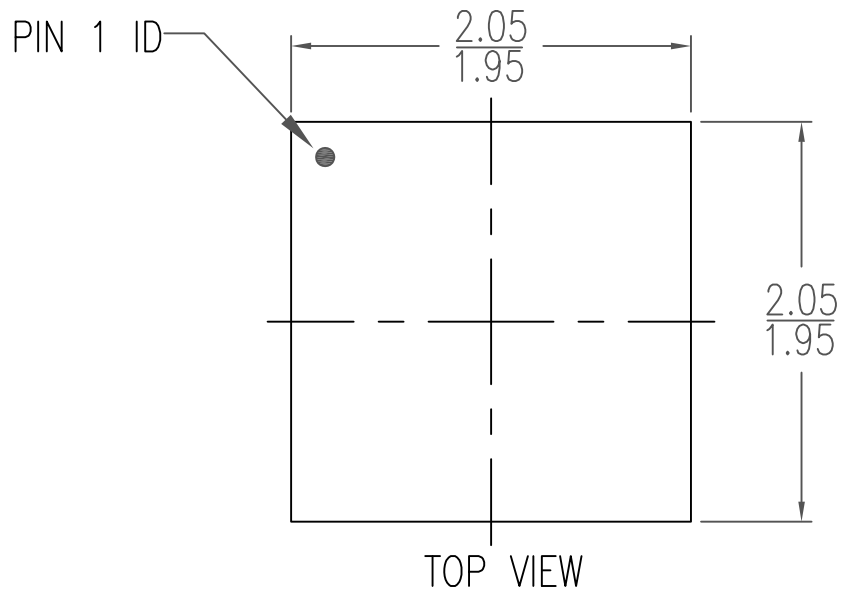
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
July 24, 2018	Rev 00	Initial Release



REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
09/18/14	00	INITIAL RELEASE	J.HUA
4/5/18	01	CHANGE VFQFN to DFN	R.C
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

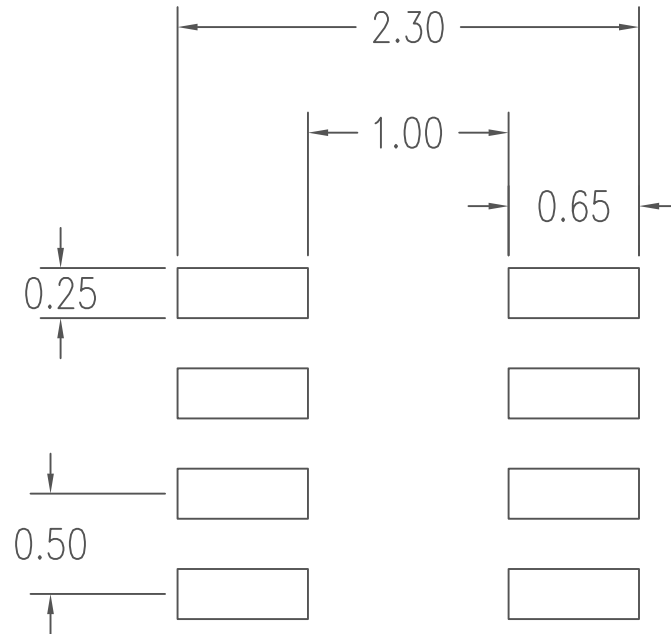


NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± ± XXXX± ±	<b>IDT</b> 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674 <small>www.IDT.com</small>	
	TITLE CMC8 Package Outline Drawing 2.0 x 2.0 x 0.5 mm Body 0.5mm Pitch DFN	
SIZE C	DRAWING No. PSC-4490	REV 01
DO NOT SCALE DRAWING		SHEET 1 OF 2


REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
09/18/14	00	INITIAL RELEASE	J.HUA
4/5/18	01	CHANGE VQFN to DFN	R.C
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			



### RECOMMENDED LAND PATTERN DIMENSION

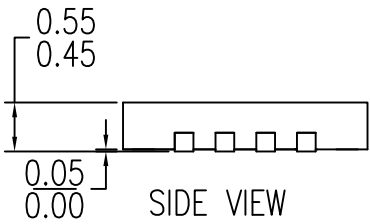
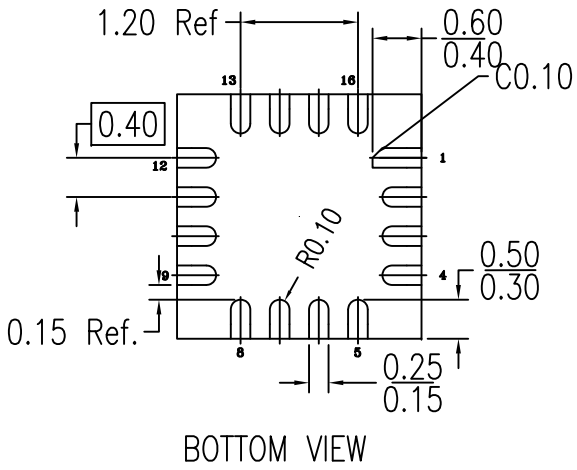
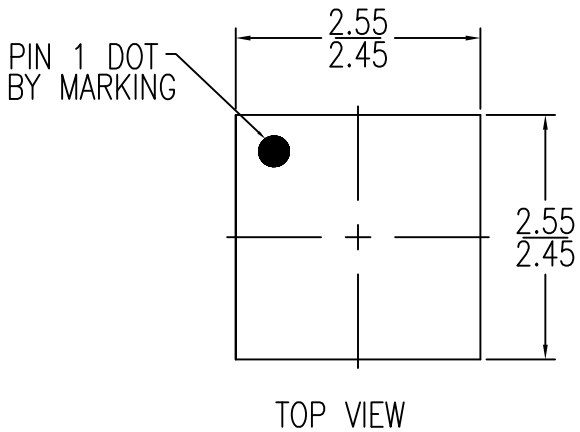
#### NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.


TOLERANCES UNLESS SPECIFIED		 <b>IDT</b> 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
TITLE		CMG8 Package Outline Drawing 2.0 x 2.0 x 0.5 mm Body 0.5mm Pitch DFN
SIZE	DRAWING No.	REV
C	PSC-4490	01
DO NOT SCALE DRAWING		SHEET 2 OF 2

REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
4/3/14	00	INITIAL RELEASE	JH
12/11/14	01	ADD PIN1 CHAMFER	JH
4/5/18	02	CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN	RC

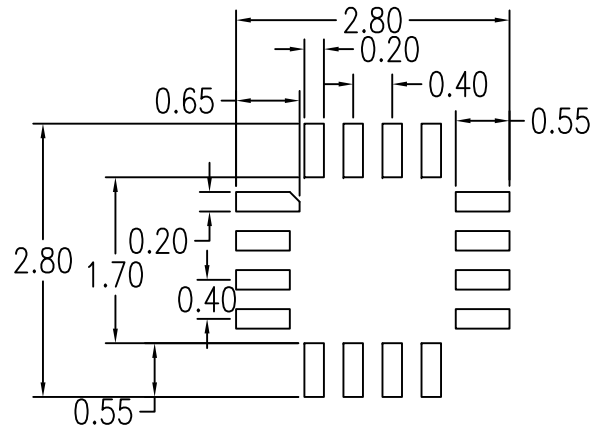
NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE



- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
  2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX±	ANGULAR ±1°	 <b>IDT™</b> www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591	
			TITLE CMG16 Package Outline Drawing 2.5 x 2.5 x 0.5 mm Body 0.40mm Pitch VFQFPN	
DRAWN	SIZE	DRAWING No.	REV	
	C	PSC-4478	02	
DO NOT SCALE DRAWING			SHEET 1 OF 2	


REVISIONS			
DATE CREATED	REV	DESCRIPTION	AUTHOR
4/3/14	00	INITIAL RELEASE	JH
12/11/14	01	ADD PIN1 CHAMFER	JH
4/5/18	02	CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN	RC
NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

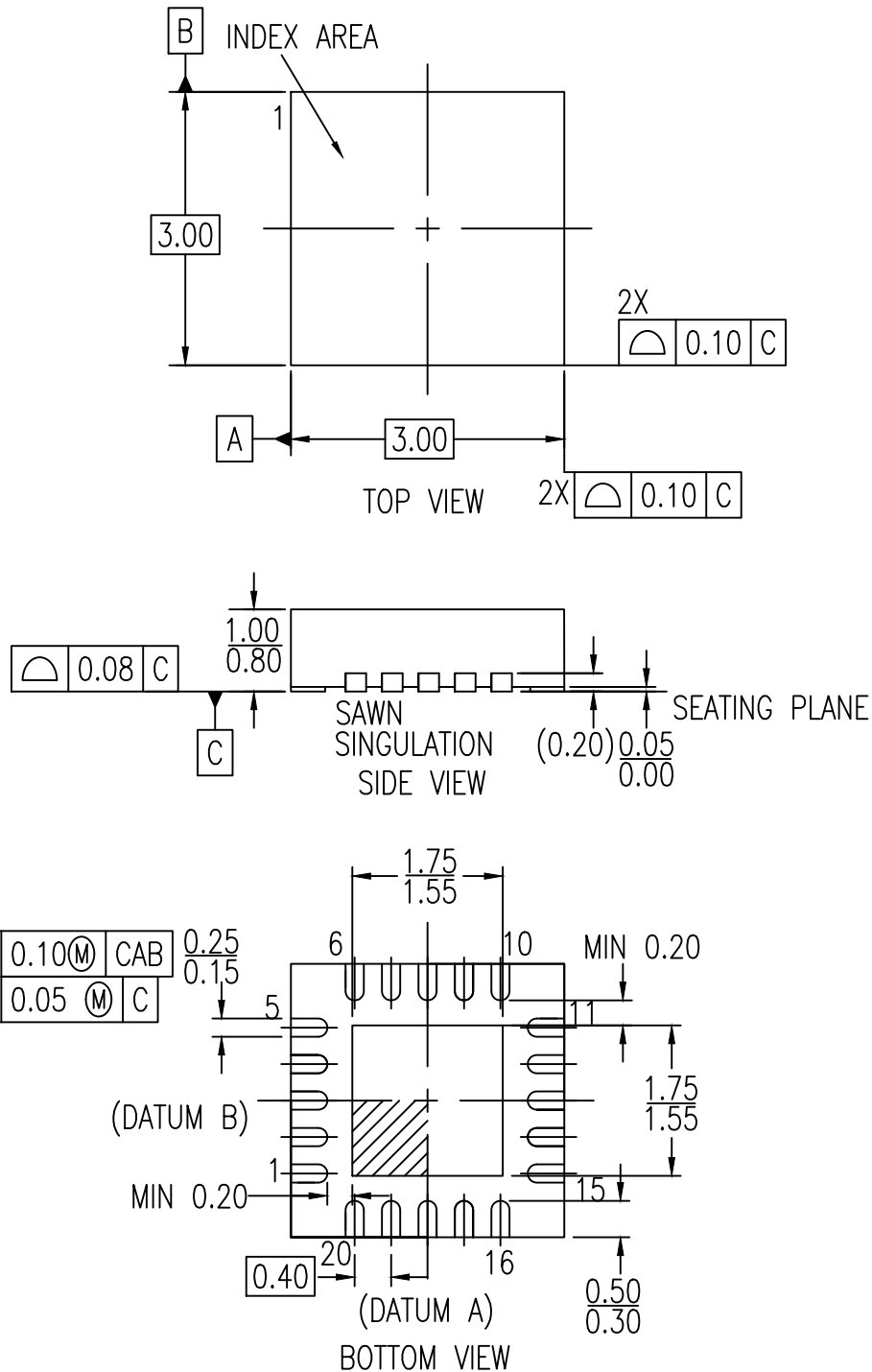


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>IDT™</b> www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591	
DECIMAL	ANGULAR			
X±	±1°			
XX±				
XXX±				
DRAWN		TITLE CMG16 Package Outline Drawing 2.5 x 2.5 x 0.5 mm Body 0.40mm Pitch VFQFPN		
SIZE	DRAWING No.	REV		
C	PSC-4478	02		
DO NOT SCALE DRAWING			SHEET 2 OF 2	



NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
3. PIN 1 LOCATION IDENTIFIER IS EITHER BY CHAMFER OR NOTCH

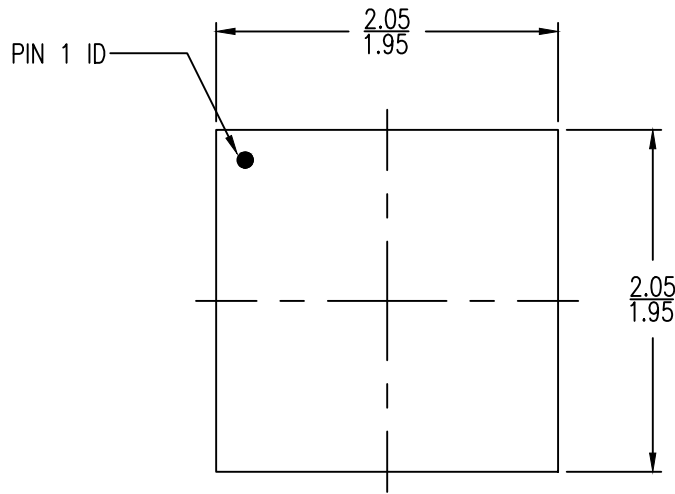


RECOMMENDED LAND PATTERN DIMENSION

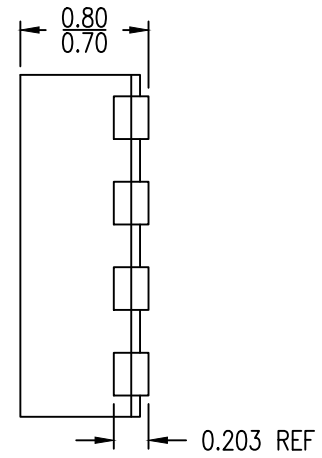
NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

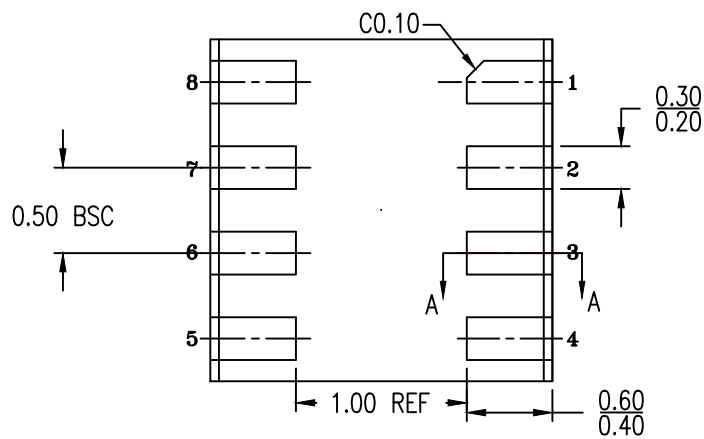
Package Revision History		
Date Created	Rev No.	Description
Sept 13, 2018	Rev 01	Change QFN to VFQFPN
Mar 30, 2016	Rev 00	Initial Release



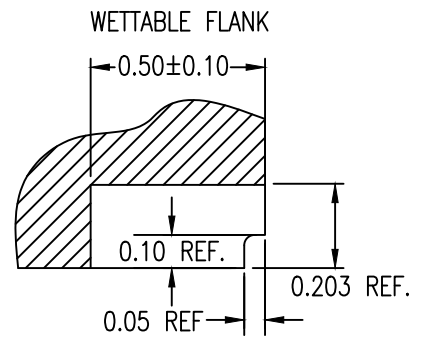
TOP VIEW



SIDE VIEW



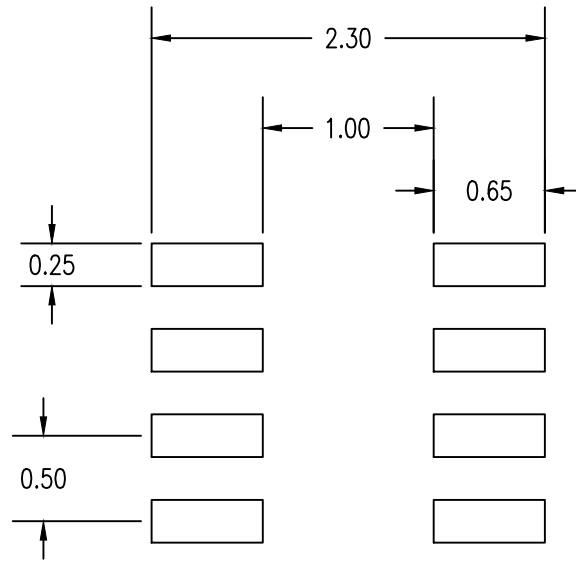
BOTTOM VIEW



A-A CROSS SECTION

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Oct 23, 2018	Rev 00	Initial Release