THAT Corporation

2-Channel Low-Noise Programmable-Gain Preamplifier - ADC Driver IC

THAT 6261, 6263, 6266

FEATURES

- Low noise: –127 dBu EIN[1] (max gain)
- –8 dB to +34 dB gain
- Choice of step size: 1, 3, or 6dB
- +16.5 dBu maximum input (min gain)
- Integrated ADC driver with reference input
- High common-mode rejection: >65dB
- Very low power: 30 mW per channel
- Unipolar or Bipolar power supplies
  Analog: +10V +5V or ±5V; Digital: +3.3V
- Small form factor: 7x7mm QFN package
- Zero crossing detectors minimize zipper noise
- Daisy-chainable SPI control interface
- Individually controlled Standby and Mute

APPLICATIONS

- Digitally controlled input stages
  Microphone preamplifiers
  Instrumentation amplifiers
  Differential amplifiers
- Audio mixing consoles
- PC audio interfaces
- Digital video cameras
- Digital audio snakes
- Portable audio recorders
- Programmable gain amplifiers

Description

The THAT 626x is a family of two-channel "all-in-one" digitally controlled preamplifiers with integrated ADC drivers. Gain is programmable from -8 to +34 dB. The 626x family includes three products distinguished primarily by step size:

Part	6261	6263	6266
Step size	1dB	3dB	6dB

All three parts offer excellent noise performance: at +34dB gain, the 6261 EIN is –127 dBu, while the 6263 and 6266 are -126 dBu. Dynamic range at -8dB gain is up to 118.7 dB.

The parts' outputs interface directly to commonly used 5 V ADC ICs with 2 Vrms differential full-scale inputs. Therefore, they serve as a complete solution to connect an audio input to an A/D converter.

To minimize audibility of gain changes with signal, all 626x family members can be programmed to synchronize gain changes with signal zero crossings. A BUSY pin for each channel allows external events to be synchronized with zero crossings. This enables external gain changes to by seamless with internal ones.

The low-power (60 mW) devices can be powered from unipolar (+10 V and +5 V) or bipolar (±5 V) supplies. The parts are controlled via a 4-wire SPI interface running at up to 7.5 MHz (+3.3V supply). Multiple devices may be daisy-chained using one chip select.

Four general purpose logic outputs (GPOs) are available to control external circuitry (e.g., pad, phantom power). The GPOs may be synchronized with zero-crossings. Each channel may be set to low-power standby mode, and can be muted by about 62 dB.

The 626x comes in a 7X7 mm 48-pin QFN package. They are truly all-in-one mic preamps – from XLR to ADC.

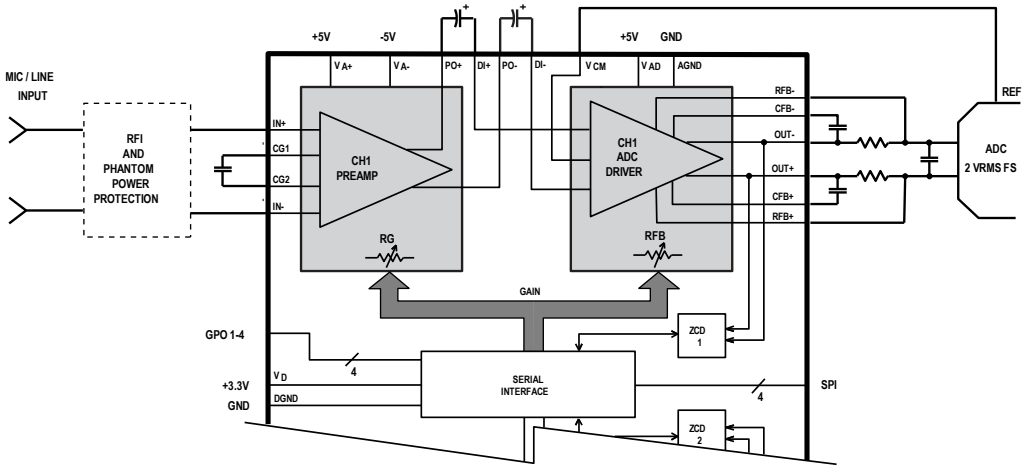

Figure 1. 626x simplified block diagram, bipolar supplies (one channel shown).

[1] 6261, 150Ω termination, 20kHz bandwidth, unweighted

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SPECIFICATIONS[2]

Absolute Maximum Ratings[3]

Total Analog Supply	(V_{A+} – V_{A-})	13 V	Maximum Analog Dix Input Voltage	V_{IAMAX_DI}	V_{A+}+2.5V
Preamp Positive Supply	(V_{A+} – AGND)	6.5 V	Minimum Analog Dix Input Voltage	(V_{IAMIN_DI})	V_{A-} - 0.3V
Preamp Negative Supply	(V_{A-} – AGND)	-6.5 V	Maximum Analog Inx Input Voltage	(V_{IAMAX_IN})	V_{A+} + 0.3V
Digital Logic Supply	(V_D – DGND)	+4.5 V	Minimum Analog Inx Input Voltage	(V_{IAMIN_IN})	V_{A-} - 0.3V
AGND – DGND Difference	(AGND – DGND)	0.3 V	Maximum Digital Input Voltage	(V_{IDMAX})	V_D + 0.3 V
Maximum Input Current	(IN+$_{\_CH1}$, IN-$_{\_CH1}$, IN+ $_{CH2}$, IN- $_{CH2}$)	20 mA	Minimum Digital Input Voltage	(V_{IDMIN})	DGND – 0.3 V
Maximum V_D – DGND Current		65 mA	Storage Temperature Range	(T_{STG})	-40 to +125 ºC
ADC Driver Supply	(V_{AD} – AGND)	+5.5V	Operating Temperature Range	(T_{OP})	-40 to +85 ºC
			Maximum Junction Temperature	(T_{JMAX})	+125 ºC

626x Electrical Characteristics[4]

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supply						
Recommended Operating Voltages						
Preamp Positive Supply	V_{A+}	Bipolar supply Unipolar supply	+3.9 +7.8	+5.0 +10.0	+5.5 +11.0	V V
Preamp Negative Supply	V_{A-}	Bipolar supply Unipolar supply	-3.9 -0.1	-5.0 0	-5.5 +0.1	V V
ADC Driver Supply	V_{AD}		+3.8	+5.0	+5.25	V
Digital Logic Supply	V_D		+3.0	+3.3	+3.6	V
Quiescent Current						
Preamp Positive Supply Current	I_{A+} I_{A+_off}	Normal operation Both channels in standby	— —	4.8 100	6.5 —	mA µA
Preamp Negative Supply Current	I_{A-} I_{A-_off}	Normal operation Both channels in standby	— —	4.8 100	6.5 —	mA µA
ADC Driver Supply Current	I_{AD} I_{AD_off}	Normal operation Both channels in standby	— —	2.5 100	4.0 —	mA µA
Digital Logic Supply Current	I_D	6261/6263 6266	— —	10 0.5	— —	µA µA

System AC Characteristics

Parameter	Symbol	Conditions	6261 Min.	6261 Typ.	6261 Max.	6263 Min.	6263 Typ.	6263 Max.	6266 Min.	6266 Typ.	6266 Max.	Units
Gain Range			-8	—	34	-8	—	34	-8	—	34	dB
Step Size			0.5	1	1.5	2	3	4	4	6	8	dB
Gain Error		Gain:[-8dB ~30dB] Gain:[31dB ~ 34dB]	-0.5 -1	±0.2 ±0.3	0.5 1	-0.5 -1	±0.2 ±0.3	0.5 1	-0.5 -1	±0.2 ±0.3	0.5 1	dB dB
Gain Matching Between Channels			-0.25	±0.02	0.25	-0.25	±0.02	0.25	-0.25	±0.02	0.25	dB
Mute Attenuation			—	-62	—	—	-62	—	—	-62	—	dB
Channel Isolation		Rs=150 ohm f=1kHz	—	-100	—	—	-100	—	—	-100	—	dB
CMRR		f=1kHz,Gain=-8dB Gain= +34dB	— —	65 104	— —	— —	65 104	— —	— —	65 104	— —	dB dB
Max Differential Input Level	V_{ID}	(-8 dB Gain THD: 0.15% @1kHz)		16.5			16.5			16.5		dBu
Input Common-Mode Range	V_{ICM}	Linear operation	V_{A-}+1.2	—	V_{A+}-1.2	V_{A-}+1.2	—	V_{A+}-1.2	V_{A-}+1.2	—	V_{A+}-1.2	V

System AC Characteristics (cont'd)												
THD+N		1kHz, 2Vrms Out +10dB Gain -8dB Gain	— —	0.0015 0.05	— —	— —	0.0015 0.05	— —	— —	0.0015 0.05	— —	% %
Equivalent Input Noise	EIN	Rs=150Ω,20kHz BW Gain = -8 dB Gain = 1 dB Gain = +10 dB Gain = +22 dB Gain = +34 dB	 — — — — —	 -102.5 -111.0 -118.5 -125.0 -127	 — — — — —	 — — — — —	 -102.5 -111.0 -118.5 -125.0 -126	 — — — — —	 — — — — —	 -102.5 -111.0 -118.5 -125.0 -126	 — — — — —	 dBu dBu dBu dBu dBu

Preamp						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage, Differential	V_{HV_OSI}		—	±2.0	—	mV
Input Bias Current	I_{HV_B}		—	2.5	—	µA
Input Offset Current	I_{HV_OS}		—	250	—	nA
Slew Rate	SR	R_L = 2 kΩ, C_L = 5 pF	—	6.7	—	V/µS
V_{A+}, V_{A-} Power Supply Rej.	$PSRR_{HV}$	DC V_{A+} = -V_{A-} = 3.9 V to 5.5 V	—	85	—	dB
Output Swing	V_{HV_OUT}		V_{A-} +1	—	V_{A+} –1	V

ADC Driver						
Input Differential Voltage	$V_{LV\_in\_dif}$		V_{A-}		V_{A+}+2	V
Input Common-Mode Voltage	$V_{LV\_in\_cm}$	Linear operation	3.5-2.5*V_{CM}		V_{A+}+2	V
Voltage at CFB+, CFB-	$V_{CFG+,\ CFB-}$		1.0		V_{AD}	V
Differential Output Offset	V_{LV_OD}		-2	±0.3	2	mV
LV Output Voltage	V_{LV_OUT}	R_L = 1 kΩ	0.5	—	V_{AD} – 0.5	V
Slew Rate	SR	R_L = 5 kΩ, C_L = 10 pF	—	4.5	—	V/µS
Output Resistive Loading	R_L		1	—	—	kΩ
Capacitive Load Stability	C_L	C_L Directly on Output Pins	—	—	100	pF
V_{AD} Power Supply Rejection	$PSRR_{LV}$	DC V_{AD} = +3.8 V to +5.25 V	—	95	—	dB
V_{CM} Input Impedance	Z_{CM}		—	>100/2	—	MΩ /pF
V_{CM} Input Voltage Range	V_{ICM}		(V_{AD}/2)-1	V_{AD}/2	(V_{AD}/2)+1	V

Zero-Crossing Detector						
Zero-Crossing Detector Threshold	V_{TZCD}		—	±10	—	mV
Zero-Crossing Timeout	T_{ZCD}		—	22	35	ms

Digital I/O and Switching						
High Level Input Voltage	V_{IH}		0.7*V_D	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3*V_D	V
High Level Output Voltage	V_{OH}	Iout = 4 mA	0.8*V_D	—	—	V
Low Level Output Voltage	V_{OL}	Iout = -4 mA	—	—	0.4	V

Digital I/O and Switching (cont'd)					
Input Leakage Current	I_{IN}	—	2	—	µA
Input Capacitance	C_{IN}	—	3.5	—	pF
High-level Output Current	I_{OH}	—	4	25	mA
Low-level Output Current	I_{OH}	-25	4	—	mA
S_{CLK} Frequency	f_{SCLK}	—	—	7.5	MHz
S_{CLK} Low Time	t_{SCL}	40	—	—	ns
S_{CLK} High Time	t_{SCH}	40	—	—	ns
D_{IN} to S_{CLK} Rising Setup	t_{DSU}	15	—	—	ns
S_{CLK} Rising to D_{IN} Hold Time	t_{DH}	15	—	—	ns
$\overline{CS}$ Enabled to S_{CLK} High	t_{CSCR}	50	—	—	ns
$\overline{CS}$ Enabled to D_{OUT} Active	t_{CSDA}	100	—	—	ns
$\overline{CS}$ Release to D_{OUT} Tristate	t_{CSDH}	5	—	20	ns
S_{CLK} Falling to D_{OUT} Valid	t_{CFDO}	—	—	15	ns
S_{CLK} Falling to $\overline{CS}$ Inactive	t_{CFCS}	40	—	—	ns
$\overline{CS}$ High Time Bet. Transmissions	t_{CSH}	25	—	—	µs
$\overline{CS}$ Release to S_{CLK} Rising	t_{CSRCR}	100	—	—	ns

[2] All specifications subject to change without notice.

[3] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[4] Unless otherwise noted, V_{A+} = +5V, V_{A-} =-5V, V_{AD} = +5V, V_D = +3.3V, V_{CM} = +2.5V, T_A = 25 ºC.

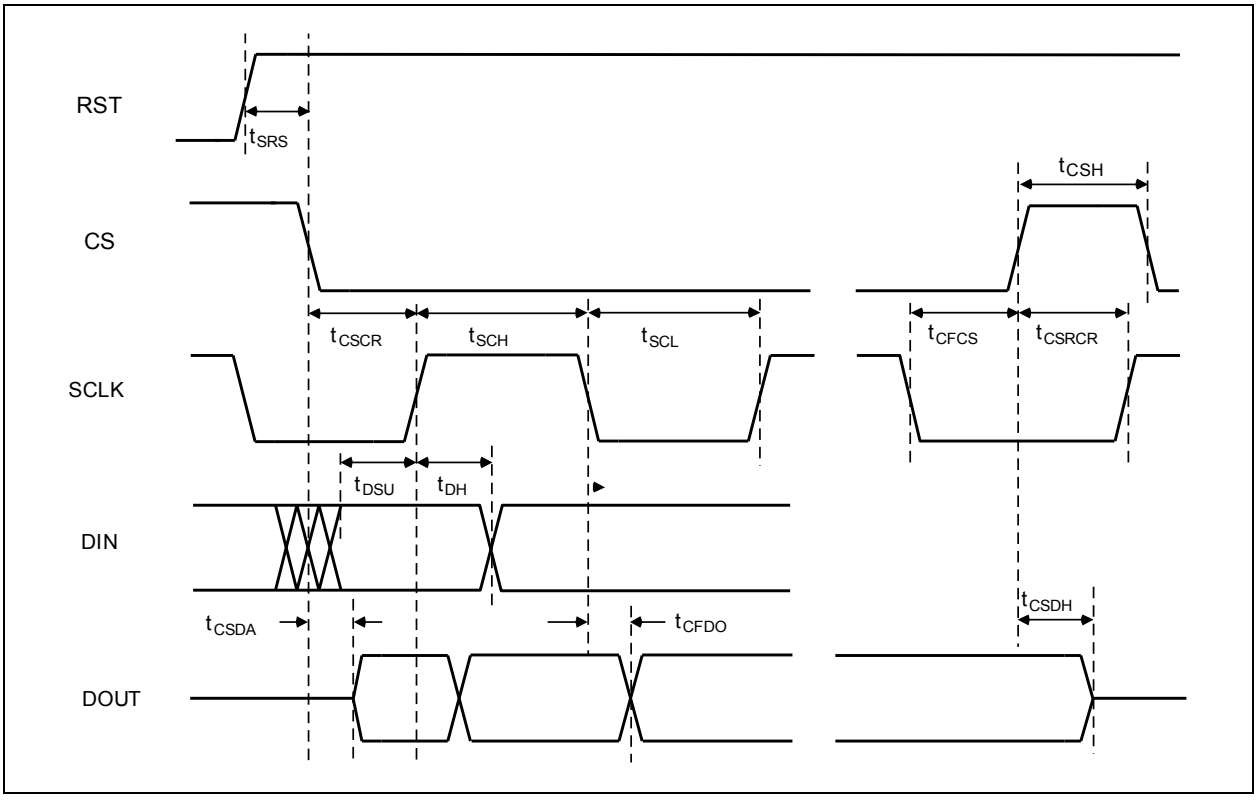


Figure 2. SPI timing diagram.

Typical Performance Graphs

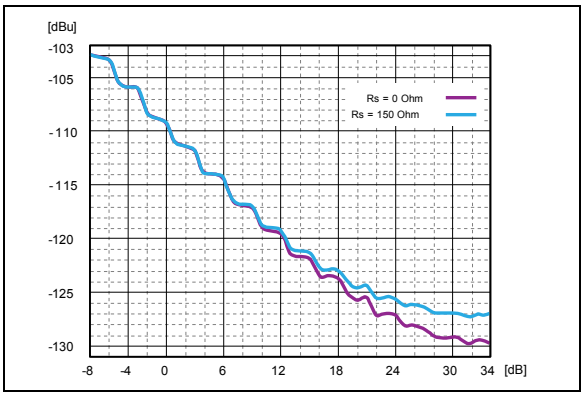


Figure 3. 6261 EIN vs. gain, 0Ω and 150Ω termination.

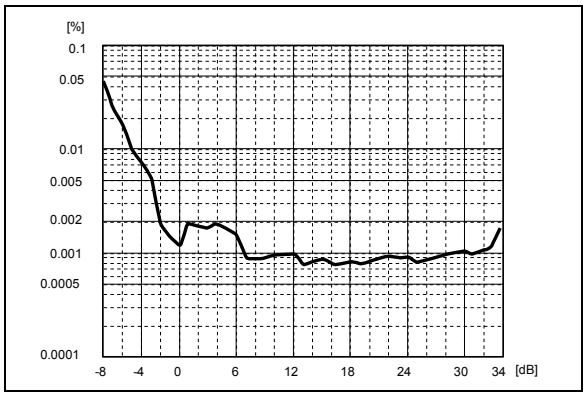


Figure 4. 6261 THD+N vs gain, f=1kHz, Vout=2Vrms

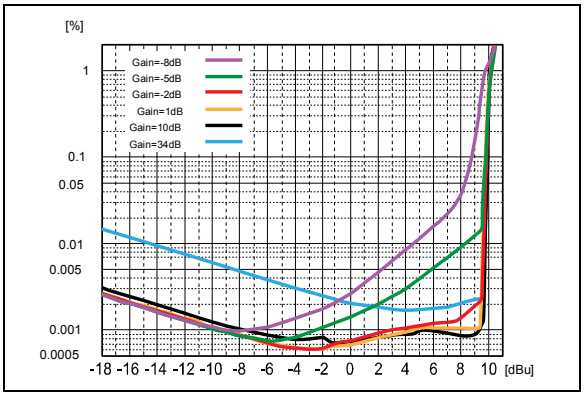


Figure 5. 6261 THD+N vs. output swing at different gains.

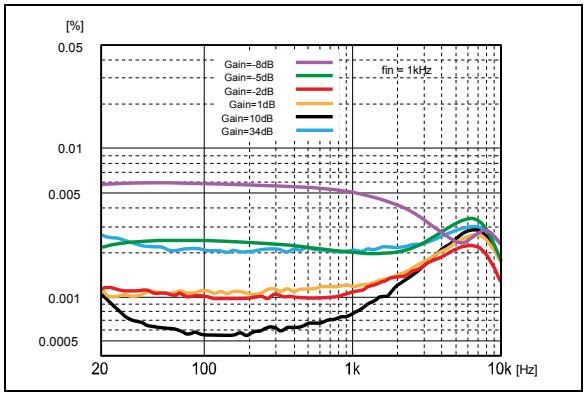


Figure 6. 6261 THD+N at Vout=1Vrms vs. frequency, 22kHz BW.

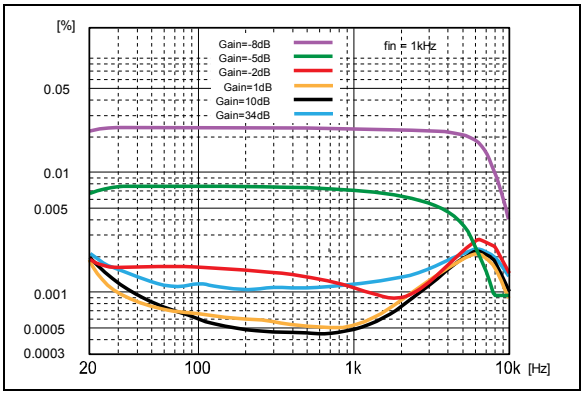


Figure 7. 6261 THD+N at Vout=1.8Vrms vs. frequency, 22kHz BW.

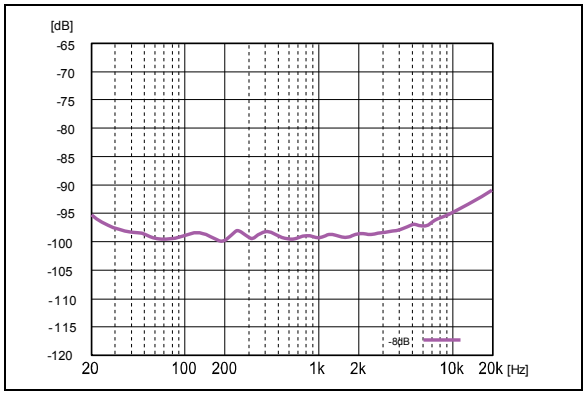


Figure 8. 6261 ADC driver stage VAD PSRR vs. frequency.

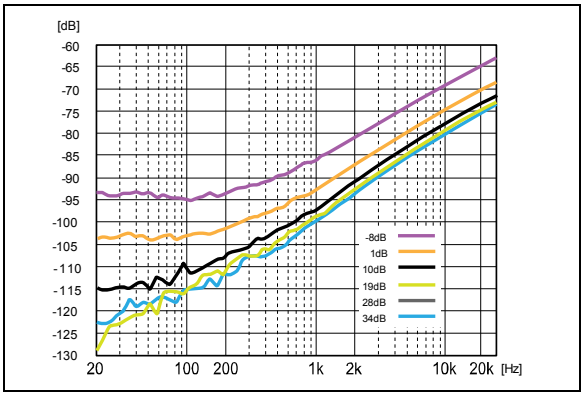


Figure 9. 6261 preamp stage VA+ PSRR vs. frequency & gain setting.

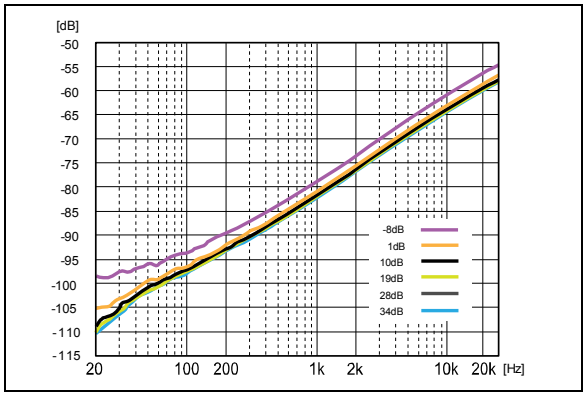


Figure 10. 6261 preamp stage VA- PSRR vs. frequency & gain.

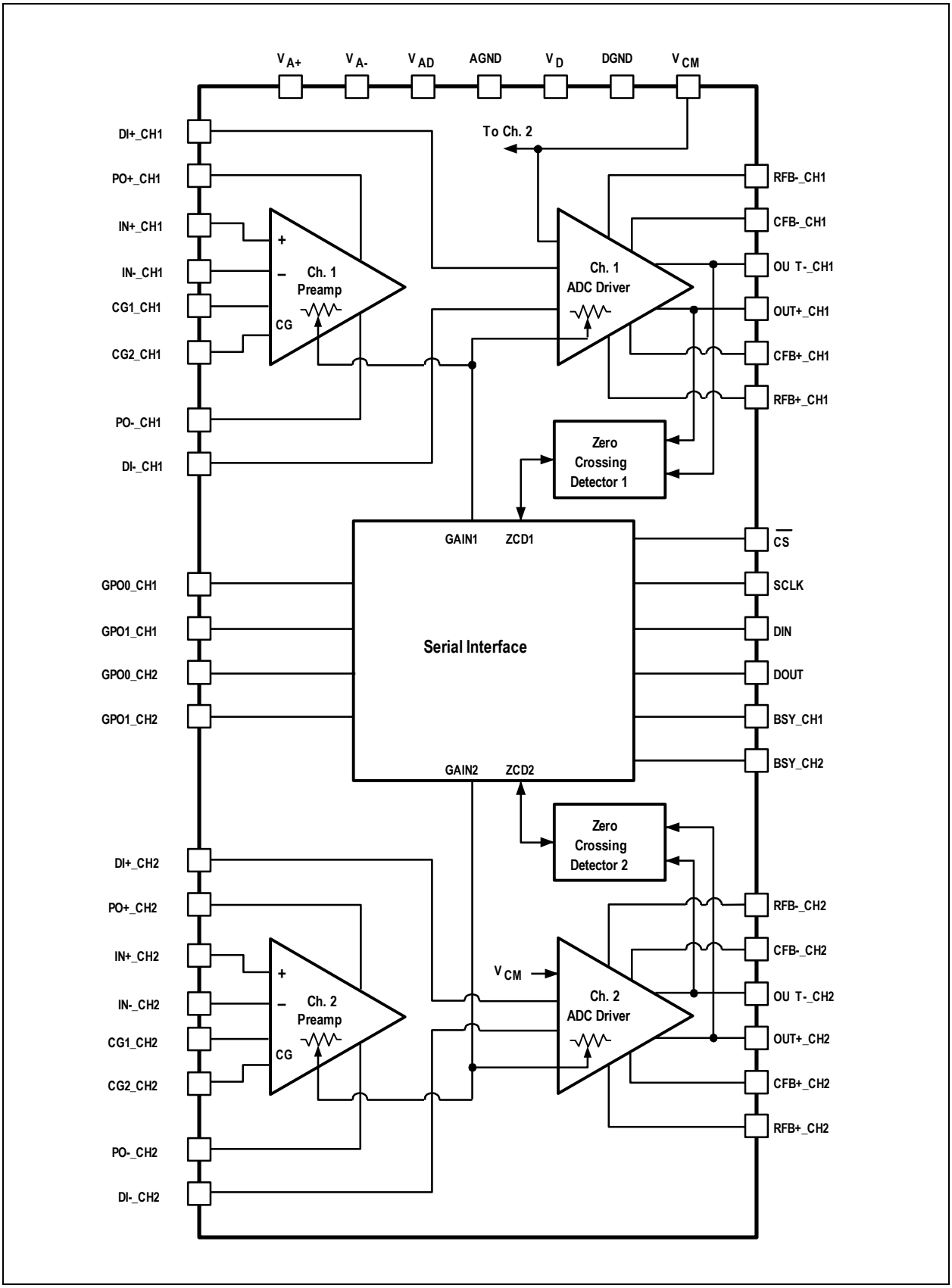


Figure 11. 626x block diagram.

Pin Name	Pin Number	Description
RFB+_CH1	1	Ch. 1 out+ resistive feedback
CFB-_CH1	2	Ch. 1 out- capacitive feedback
CFB+_CH1	3	Ch. 1 out+ capacitive feedback
V_{A+}	4	Preamp positive supply voltage
DI+_CH1	5	Ch. 1 ADC driver + input
DI-_CH1	6	Ch. 1 ADC driver - input
PO+_CH1	7	Ch. 1 preamp + output
PO-_CH1	8	Ch. 1 preamp - output
V_{A-}	9	Preamp negative supply voltage
V_{A+}	10	Preamp positive supply voltage
CG2_CH1	11	Ch. 1 feedback ac-coupling, term. 2
CG1_CH1	12	Ch. 1 feedback ac-coupling, term. 1
IN-_CH1	13	Ch. 1 preamp - input
IN+_CH1	14	Ch. 1 preamp + input
V_{A-}	15	Preamp negative supply voltage
CG2_CH2	16	Ch. 2 feedback ac-coupling, term. 2
CG1_CH2	17	Ch. 2 feedback ac-coupling, term. 1
IN-_CH2	18	Ch. 2 preamp - input
IN+_CH2	19	Ch. 2 preamp + input
V_{A-}	20	Preamp negative supply voltage
PO+_CH2	21	Ch.2 preamp + output
PO-_CH2	22	Ch. 2 preamp - output
DI+_CH2	23	Ch. 2 ADC driver + input
DI-_CH2	24	Ch. 2 ADC driver - input
V_{A-}	Thermal pad	

Pin Name	Pin Number	Description
GPO0_CH1	25	Ch. 1 GPO0
GPO1_CH1	26	Ch. 1 GPO1
BSY_CH1	27	Ch. 1 busy pin
DGND	28	Digital ground
V_D	29	Digital power supply (3.3V)
$\overline{CS}$	30	Chip select (active low)
SCLK	31	Serial clock input
DIN	32	Serial port data input
DOUT	33	Serial port data output
BSY_CH2	34	Ch. 2 busy pin
GPO0_CH2	35	Ch. 2 GPO0
GPO1_CH2	36	Ch. 2 GPO1
CFB+_CH2	37	Ch. 2 out+ capacitive feedback
CFB-_CH2	38	Ch. 2 out- capacitive feedback
RFB+_CH2	39	Ch. 2 out+ resistive feedback
RFB-_CH2	40	Ch. 2 out- resistive feedback
OUT+_CH2	41	Ch. 2 + output to ADC
OUT-_CH2	42	Ch. 2 - output to ADC
AGND	43	Analog ground
V_{CM}	44	ADC driver CM reference input
V_{AD}	45	5V ADC driver supply voltage
OUT-_CH1	46	Ch. 1 - output to ADC
OUT+_CH1	47	Ch. 1 + output to ADC
RFB-_CH1	48	Ch. 1 out- resistive feedback

Table 1. Pin Assignments.

Theory of Operation

The THAT 626x (x=1, 3 or 6) is a family of two-channel digitally controlled microphone preamplifiers with integrated ADC drivers. Depending on the model, gain of the parts is programmable in 1, 3, or 6 dB steps.

Part	6261	6263	6266
Step size	1 dB	3 dB	6 dB

The 626x family is implemented in a mixed-voltage multi-well Bi-CMOS process that integrates 10 V, 5 V, and 3.3 V circuitry onto a single silicon die. The combination of process and design also allows operating the device with ±5 V, 5 V, and 3.3 V supplies, but it may also be powered from 10 V, 5 V, and 3.3 V supplies.

THAT 626x seamlessly bridges between a professional-audio line/microphone input and a 5 V-powered A/D converter. It contains two independently controlled differential analog signal processing channels. The high level of integration minimizes the PCB area required for such systems. Further, THAT 626x's low power consumption simplifies system heat management; this is especially helpful when integrating many channels in a single system.

Each differential analog channel in the 626x consists of a low-voltage-noise, gain-programmable preamplifier stage, a gain-programmable ADC driver stage and a zero-crossing detector (ZCD). To minimize audible switching noise, gain switching events can be synchronized to moments when the ADC driver differential output signal is close to zero. An external signal (at the BSY pins) indicates when zero-crossing-based gain changes or GPO updates take place. Each channel can also be put into a minimum power stand-by mode when not in use. And, each channel can be muted. The part is programmed via a 4-wire serial peripheral interface (SPI) shared by the two channels.

Programmable Gain Settings

The 626x implements its overall gain in two stages: a preamp stage and an ADC driver stage. The preamp stage gain ranges from 0 dB to +39 dB. It can accommodate input signals as high as +16.5 dBu at the lowest gain. The ADC driver attenuates the preamp's output by from –5 to –8dB in order to fit the signal within the typical 2 Vrms full-scale input voltage of integrated ADCs. The ADC driver also rejects common-mode signals, providing a dc pedestal (derived from the V_{CM} input) on which to queue the differential outputs.

Gain-Programmable Preamplifier Stage

The preamp stage consists of a low-voltage-noise current-feedback differential amplifier with gain programmed by an array of resistors and CMOS switches that makes up R_G. See Figure 12 for detail of one of the two channels. The R_G resistor/switch array is programmed via the SPI digital control interface. The resulting gain varies from 0 dB to 39 dB in 3 dB steps (in the 6261 and 6263) or 6 dB steps (6266). The preamp feedback resistors have a nominal value of 2 kΩ. The R_G values with the corresponding gains for THAT 6261, 6263 and 6266 are listed in Table 2.

The R_G network should be ac-coupled using an external capacitor C_G. This limits dc gain to unity for all ac gain settings, ensuring that the preamp's output offset voltage will be constant for all gain settings.

The preamp's differential output (between the PO+ and PO- pins) has a fixed dc common-mode level of one V_{BE} (~0.6V) below the voltage at the input pins (IN+ and IN-). The PO+ and PO- pins are typically ac-coupled to the ADC driver stage through external capacitors (C_{C1} and C_{C2}). This allows the ADC driver stage to operate around the voltage (typically +2.5V) supplied at the V_{CM} pin. This voltage should match that required for the ADC being driven.

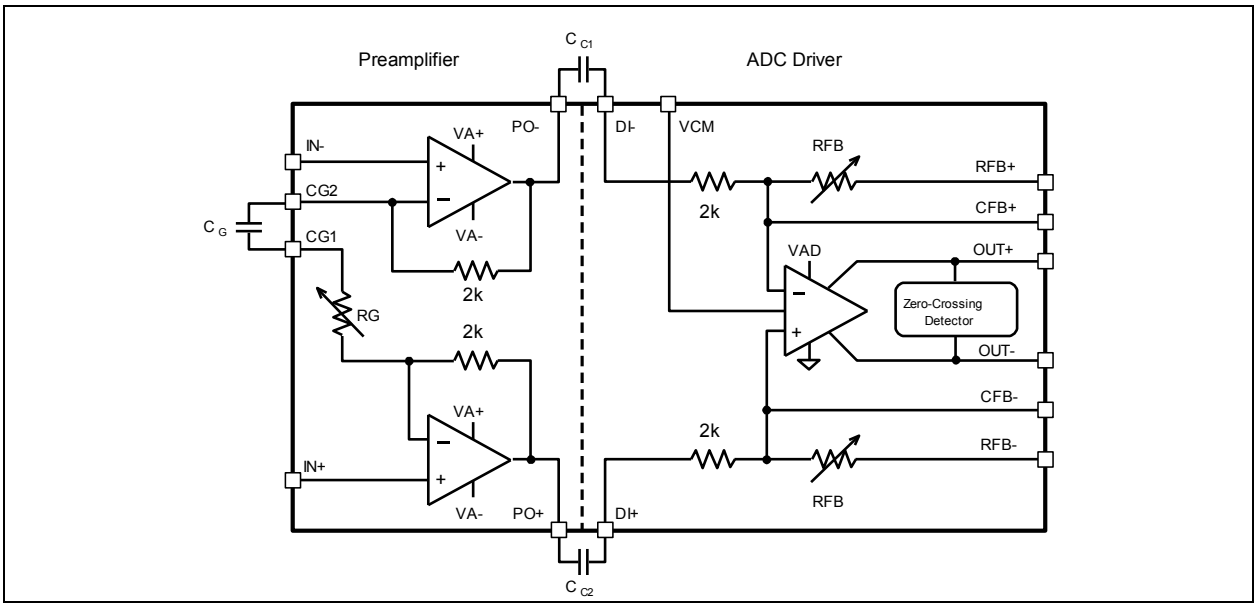


Figure 12. Analog Section Functional Block Diagram

Note that the preamp stage has unity common-mode gain, regardless of the differential gain setting.

Gain-Programmable ADC Driver Stage

The ADC driver stage operates from a single +5V supply. It includes a fully differential amplifier with gain controlled by internal resistors and CMOS switches programmed via the SPI interface. The inputs of this stage (DI-, DI+) can handle the full differential signal swing available at the outputs of the preamp (PO+ and PO-).

Each input has a nominal input resistance of 2kΩ. As shown in Table 2, the feedback resistor array enables gains of –8, –7, and –6dB in the 6261, while in the 6263 and 6266 the gain is fixed at –8dB.

Six external pins per channel (OUT+, OUT-, RFB+, RFB-, CFB+, and CFB-) provide the flexibility to configure the ADC driver's feedback network into different anti-aliasing filter topologies for driving different ADCs. One common configuration is shown in Figures 17 and 20. An alternative is shown in Figure 18. We recommend that you follow the ADC maker's recommendations.

The ADC driver includes a common-mode feedback circuit which rejects common-mode input signals, and forces the common-mode output voltage of the amplifier outputs (pins OUT+_CHx and OUT-_CHx, x=1,2) to equal the voltage supplied to the V_{CM} pin. For the feedback loop to function properly, the common-mode voltage at the amplifier's differential inputs (pins CFB+_CHx and CFB-_CHx) must stay at or above the minimum value in the specification table. These nodes are virtual grounds for differential signals, and only move with common-mode input signals. However, if the level on the virtual ground pins falls below the minimum value, the amplifier's input transistors will become improperly biased, which will result in the feedback loop opening, and the amplifier outputs being stuck at ground. See comments (under "ADC Driver V_{CM} Input", on page 15 and again – for unipolar supplies—on page 18) in the Applications section for preventative measures,

Due to the good matching of the on-chip resistors, the common-mode rejection of this stage is typically 62 dB. Combined with the unity common-mode gain of the preamp section, the 626x's overall common-mode rejection performance increases from this minimum value directly with the preamp gain.

Note, however, that the matching between the input coupling capacitors C_{C1} and C_{C2} will impact each individual amplifier's common-mode gain, thus limiting CMR at frequencies where the capacitors present significant impedance to the signal. For optimum low-frequency CMR, choose large values for these capacitors, or ensure that smaller values are well matched. Power supply rejection will also be affected by the differential matching between the internal resistors and external capacitors.

The preamp gain-setting resistor (R_G) and ADC driver feedback resistor (R_{FB}) values (Figure 12) with the corresponding gains for THAT 6261, 6263 and 6266 are listed in Table 2.

6261 Gain (dB)	6263 Gain (dB)	6266 Gain (dB)	Preamp Gain (dB)	R_G (Ω)	ADC Driver Gain (dB)	R_{FB} (Ω)
-8	-8	-8	0	250k	-8	796
-7					-7	893
-6					-6	1002
-5	-5		3	9696	-8	796
-4					-7	893
-3					-6	1002
-2	-2	-2	6	4019	-8	796
-1					-7	893
0					-6	1002
1	1		9	2270	-8	796
2					-7	893
3					-6	1002
4	4	4	12	1352	-8	796
5					-7	893
6					-6	1002
7	7		15	847	-8	796
8					-7	893
9					-6	1002
10	10	10	18	575	-8	796
11					-7	893
12					-6	1002
13	13		21	387	-8	796
14					-7	893
15					-6	1002
16	16	16	24	269	-8	796
17					-7	893
18					-6	1002
19	19		27	183	-8	796
20					-7	893
21					-6	1002
22	22	22	30	130	-8	796
23					-7	893
24					-6	1002
25	25		33	92	-8	796
26					-7	893
27					-6	1002
28	28	28	36	65	-8	796
29					-7	893
30					-6	1002
31	31		39	45	-8	796
32					-7	893
33					-6	1002
34	34	34			-5	1125

Table 2. THAT 626x gain and internal resistor values.

Switching Noise

The 626x includes several features which minimize the gain switching noise in both the preamp and ADC driver stages. First, the gate drive to the programmable CMOS switches is purposely slowed to minimize charge injection. This helps suppress clicks during gain-changing events. To further minimize gain-switching noise, the 626x also includes zero-crossing detectors to restrict gain changes to times when the analog differential signal is very close to zero. With the zero-crossing feature enabled, gain changes in the presence of program material are significantly less audible than when disabled.

Zero Crossing Detectors (ZCD)

When enabled, the zero-crossing detectors monitor the differential signal present at the ADC driver outputs of the 626x. Gain changes are permitted only when the differential output signal in the associated channel is typically within ±10 mV. An internal ~22 msec timeout forces the gain change to occur (at the expiration of the timeout) in case the signal has not moved within the voltage window by that time. The zero-crossing detectors can be enabled to synchronize gain changes and/or GPO updates with signal zero crossings. Both channels are enabled or disabled simultaneously, but GPO and Gain change synchronization with ZCDs are independently controlled. See "Zero Crossing Detectors", page tk.

Busy Pins

With zero-crossing mode enabled, the BSY pin for the associated channel goes high when a gain change or GPO update is commanded. It remains high until the actual gain change or GPO update occurs. This enables synchronizing external circuitry with the signal's zero crossings. The zero-crossing detectors and the Busy pins are more fully described in the Applications section.

SPI Control Interface

The 626x includes a daisy chainable serial-peripheral interface (SPI) port for digital control of its internal parameters. The SPI port may be clocked at speeds up to 7.5 MHz; thus a 24-bit data word can be clocked into the chip in less than 3.5 µs.

The SPI port consists of four signals: Chip Select Bar ($\overline{CS}$), Data In (DIN), Data Out (DOUT), and Serial Clock (SCLK). See Table 3. Figure 13 shows a single 626x device connected to the SPI port of a typical host microcontroller. A command sequence is initiated when $\overline{CS}$ transitions from high to low. Data is clocked into DIN on rising edge of SCLK through an internal 24-bit shift register which holds the 626x configuration, and out the DOUT pin on falling edges of SCLK. $\overline{CS}$ makes a low to high transition at the conclusion of a command sequence. The DOUT pin is tri-stated while $\overline{CS}$ is high so that multiple devices can be connected to a single SPI MISO port on a host processor (see Figure 15).

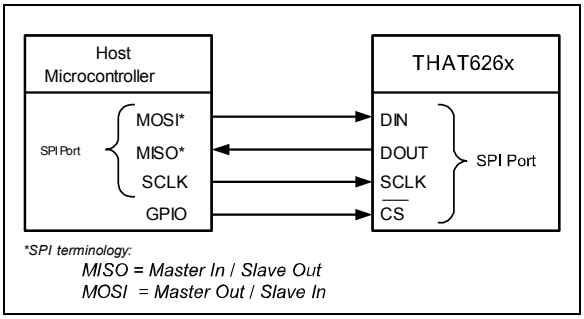


Figure 13. Single 626x connected to a host controller.

Parameters

The 626x SPI control word is 24 bits (3 bytes) long, as shown in Figure 14. The parameters that are controlled via the SPI interface are shown in Table 4 below.

Parameter	Name	Bits
Channel Gain	G_CH1 (CH2)	6/Channel
GPO State	GPO_CH1 (CH2)	2/Channel
Channel Enable	EN_CH1 (CH2)	1/Channel
Channel Mute	MT_CH1 (CH2)	1/Channel
ZCD Enable	GMD & GPOMD	2

Table 4. SPI-controllable parameters.

Signal	Pin	I/O	Function
$\overline{CS}$	30	Input	Device chip select input, active low. An SPI transfer begins with a high-to-low $\overline{CS}$ transition and ends with a low-to-high $\overline{CS}$ transition. When $\overline{CS}$ is high, SCLK transitions are ignored.
SCLK	31	Input	SPI serial clock input. An SPI master supplies this clock with frequencies up to 7.5MHz. Data is clocked into the DIN pin on the rising edge of SCLK. Data is clocked out of DOUT pin on the falling edge of SCLK.
DIN	32	Input	SPI serial data input (Master-Out, Slave-In).
DOUT	33	Output/Tristate	SPI serial data output (Master-In, Slave-Out). DOUT is tri-stated when $\overline{CS}$ is high.

Table 3. SPI control interface.

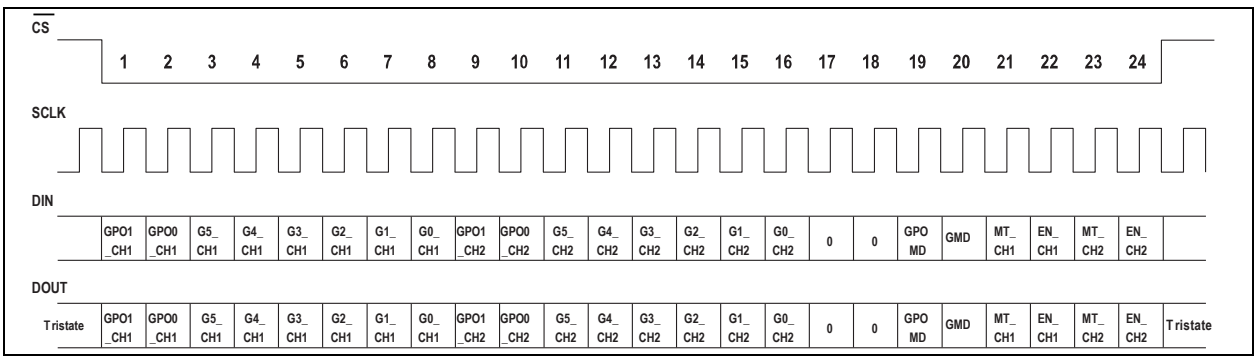


Figure 14. 626x 24-bit SPI control word definition.

Channel Gain

The G_CH1[5:0] (G_CH2[5:0]) bits set the channel 1 (2) gain by configuring its internal resistor arrays. See Tables 5 through 7. Each increment of 1 in the G_CH1 (G_CH2) value results in a 1 dB, 3 dB, or 6 dB increment in gain, depending on the device type. The bit width of the command is the same for all three parts; the 6266 ignores the G3~G5 bits, while the 6263 ignores bits G4 ~ G5. Table 5~7 show the relationship between the gain settings and actual gains of all three 626x product.

On reset, the gain of all three parts is set to its default state of 000000 (–8dB). Gain command values above the 34dB gain setting result in a gain of 34 dB.

G_CH1/2 [5:0]						Decimal Value	6261 Gain
G5	G4	G3	G2	G1	G0		
0	0	0	0	0	0	0	-8
0	0	0	0	0	1	1	-7
0	0	0	0	1	0	2	-6
0	0	0	0	1	1	3	-5
0	0	0	1	0	0	4	-4
0	0	0	1	0	1	5	-3
0	0	0	1	1	0	6	-2
0	0	0	1	1	1	7	-1
0	0	1	0	0	0	8	0
0	0	1	0	0	1	9	1
0	0	1	0	1	0	10	2
0	0	1	0	1	1	11	3
0	0	1	1	0	0	12	4
0	0	1	1	0	1	13	5
0	0	1	1	1	0	14	6
0	0	1	1	1	1	15	7
0	1	0	0	0	0	16	8
0	1	0	0	0	1	17	9
0	1	0	0	1	0	18	10
0	1	0	0	1	1	19	11
0	1	0	1	0	0	20	12
0	1	0	1	0	1	21	13
0	1	0	1	1	0	22	14
0	1	0	1	1	1	23	15
0	1	1	0	0	0	24	16
0	1	1	0	0	1	25	17
0	1	1	0	1	0	26	18
0	1	1	0	1	1	27	19
0	1	1	1	0	0	28	20
0	1	1	1	0	1	29	21
0	1	1	1	1	0	30	22
0	1	1	1	1	1	31	23
1	0	0	0	0	0	32	24
1	0	0	0	0	1	33	25
1	0	0	0	1	0	34	26
1	0	0	0	1	1	35	27
1	0	0	1	0	0	36	28
1	0	0	1	0	1	37	29
1	0	0	1	1	0	38	30
1	0	0	1	1	1	39	31
1	0	1	0	0	0	40	32
1	0	1	0	0	1	41	33
1	0	1	0	1	0	42	34
1	0	1	0	1	1	43	34
.						.	.
1	1	1	1	1	1	63	34

Table 5. 6261 SPI gain command word and settings.

G_CH1/2 [5:0]						Decimal Value	6263 Gain
G5	G4	G3	G2	G1	G0		
x	x	0	0	0	0	0	-8
x	x	0	0	0	1	1	-5
x	x	0	0	1	0	2	-2
x	x	0	0	1	1	3	1
x	x	0	1	0	0	4	4
x	x	0	1	0	1	5	7
x	x	0	1	1	0	6	10
x	x	0	1	1	1	7	13
x	x	1	0	0	0	8	16
x	x	1	0	0	1	9	19
x	x	1	0	1	0	10	22
x	x	1	0	1	1	11	25
x	x	1	1	0	0	12	28
x	x	1	1	0	1	13	31
x	x	1	1	1	0	14	34
x	x	1	1	1	1	15	34

Table 6. 6263 SPI gain command word and settings.

G_CH1/2 [5:0]						Decimal Value	6266 Gain
G5	G4	G3	G2	G1	G0		
x	x	x	0	0	0	0	-8
x	x	x	0	0	1	1	-2
x	x	x	0	1	0	2	4
x	x	x	0	1	1	3	10
x	x	x	1	0	0	4	16
x	x	x	1	0	1	5	22
x	x	x	1	1	0	6	28
x	x	x	1	1	1	7	34

Table 7. 6266 SPI gain command word and settings.

GPO State

Two General Purpose Outputs (GPOs) are associated with each channel. GPO_CH1[1:0] are for channel 1 while GPO_CH2[1:0] are for channel 2. Each of the GPO bits controls the state of the respective GPO_CH1/2 pins as shown in Table 8 below.

On reset, all GPOs are set to their default state of all ports off.

GPO	Channel	GPO #	State
GPO_CH1[0]	1	1	0=off (0V); 1= on (3.3V)
GPO_CH1[1]	1	2	
GPO_CH2[0]	2	1	
GPO_CH2[1]	2	2	

Table 8. GPO bit settings.

Channel Enable (vs. Standby)

Each channel may be enabled or set to a low-power Standby mode through the SPI port by its associated active-high enable bit: EN_CH1 controls channel 1 and EN_CH2 controls channel 2. When EN_CHx=1, channel x's analog circuitry is biased for normal operation. When EN_CHx=0, channel x's analog circuitry enters a low-power stand-by state, and the current status of all channel x's registers is reserved. Any of channel x's registers may be updates while the channel is kept in standby mode. Bringing the EN_CH1 or EN_CH2 registers back to 1 via SPI will restore the last written state of other registers.)

On reset, both channels are set to standby (00).

Channel MUTE

There are two active-high mute bits, MT_CH1 for channel 1 and MT_CH2 for channel 2. Assuming the relevant channel is enabled, setting the MT_CHx register high will mute channel x's output by more than 60 dB. When a channel is in mute mode, its preamplifier stage is set to unity gain while its ADC driver stage is configured for over 60dB attenuation. Setting MT_CHx low returns channel x's gain to the last value previously set (which remains stored in the gain registers).

When programmed, mute is effective immediately independently of the setting of ZCD enable.

While a channel is muted, its gain programmability is still active and the register gain settings can be programmed to any desired value. Gains set in this way will be implemented when the channel is unmuted.

Note that when EN_CHx=0 (channel x is in standby), MT_CHx is invalid and will be ignored.

On reset, both channels are set to the un-muted state (00).

Zero Crossing Detector (ZCD) Enable

The zero-crossing detectors are enabled for gain and GPO changes via the GMD and GPOMD bits, respectively. There is only one control for both channels; their states must be the same in both.

When GMD=1, upon transmission of an SPI gain change command to an enabled channel, gain changes are held until the signal crosses zero at that channel's ADC driver output. When GMD=0 gain setting changes to either enabled channel are applied immediately (regardless of the GPOMD setting).

When GPOMD=1 and a channel is enabled, upon transmission of an SPI command that changes the setting of GPO_CHx[1:0], the change of state at that GPO output is held until the signal crosses zero at channel x's ADC driver output. When GPOMD=0 (and that channel is enabled) and GMD=0, any changes to GPO_CHx[1:0] are effective immediately. Table 9 shows the bit settings for each of the modes.

On reset, the ZCDs are set to their default state of off for both GPOMD and GMD (00).

GPOMD	GMD	Resulting Condition
X	0	Immediate Gain updates
X	1	Gain update synchronized with ZCD event
0	X	Immediate GPO updates
1	X	GPO updates synchronized with ZCD event

Table 9. Zero crossing detector enable bits.

Controlling Multiple Devices

When using multiple 626x devices in the same product, the SPI ports can be controlled in "parallel" by using a separate chip select for each device, or in "serial" by daisy-chaining the devices.

Using Separate Chip Selects

Figure 15 shows multiple 626x devices connected with separate chip selects for each SPI port. The advantage of this method over daisy chaining is that any of the N 626x devices may be updated with a single 24-bit SPI operation (as opposed to the long Nx24 bit data stream required when N devices are daisy chained). The disadvantage of this method is N different chip selects must be supplied – one to each of the individual devices, and each 626x must be programmed at a different time.

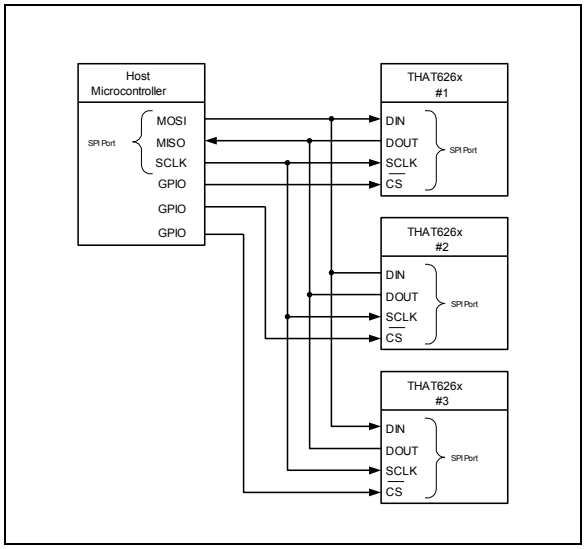


Figure 15. Multiple 626x ICs connected in parallel to a host microcontroller, with independent chip selects.

Daisy Chaining

Figure 16 shows multiple devices daisy-chained by connecting the DOUT of device N to the DIN pin of device N+1. Data is loaded by holding the common $\overline{CS}$ low for 24 x N SCLK pulses, where N = total number of devices in the daisy chain. All devices are simultaneously updated on the rising edge of $\overline{CS}$. Because one chip select is shared by all devices, this approach simplifies the digital control circuitry on the PCB, and ensures that all channels are updated simultaneously. However, since all N devices must be updated even if only one parameter in one device must be changes, the rate of control will be slower than with separate chip selects.

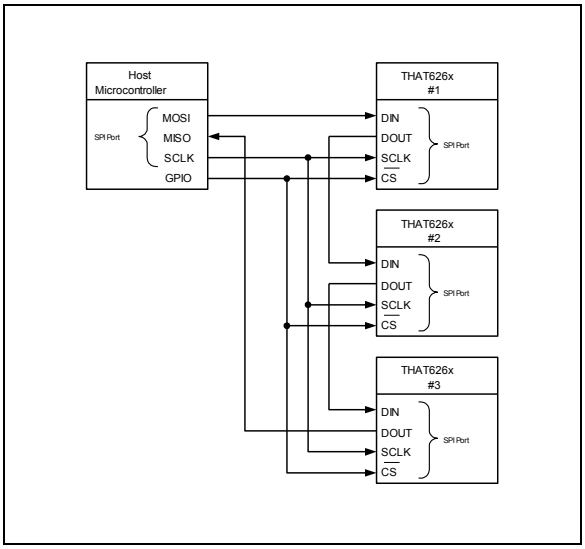


Figure 16. Multiple 626x ICs connected in a daisy-chained mode to a host microcontroller.

Applications

The preamplifier section of the 626x can be operated from bipolar (±5V) or unipolar (+10V/0V) power supplies while the ADC driver and logic sections operate from +5V and +3.3V supplies respectively. Performance is optimized for bipolar operation, but unipolar operation with virtually identical performance is also possible and is discussed in a subsequent section.

Typical Application (Bipolar Supplies)

Figure 17 is a typical 626x application circuit utilizing bipolar power supply rails. In this section, we discuss channel 1 in detail. However, all of the comments apply to the analogous components in channel 2.

C1~C3 form a Radio Frequency Interference (RFI) protection network intended to prevent RF from entering the chassis of the device in which the 626x is used. The ground ends of C1 and C2 should be connected to chassis ground via a low inductance path. All these capacitors should be located as close as possible to the input signal connector to prevent RF from getting inside the chassis.

C6~C8 are intended to minimize any high-frequency interference generated inside the chassis which might otherwise reach the inputs of the 626x. These components should be located close to the device input pins and referenced to the local signal ground.

R1~R4, C4~C5 and D1~D4 are related to phantom power, and are discussed in detail in the Phantom Power section below.

R5 and R6 provide bias current for the preamp's input transistors. R9 is to set the termination impedance for the microphone. In this case, the differential input impedance is 3kΩ. The high-pass filter corner frequency set by C4-C5 and R3~R9 is 3.8Hz for the values shown.

Limiting Input Stage DC Gain

The coupling capacitor (C9 in Figure 17, or CG in Figure 12) limits DC gain in the preamplifier to unity, regardless of the differential audio gain setting. The on-chip gain-setting R_G resistors in series with these capacitors vary with gain, which causes the cutoff frequency of the resulting high-pas filter also to vary with gain. This filter reaches its highest frequency at the minimum RG (the highest gain), which is about 45 Ω (see Table 2). Hence, the highest cut-off frequency, with the 470µF value shown in Figure 17 is ~7.5 Hz. Larger values will scale this frequency down proportionately. Since these capacitors, which are often physically large and stick up from the PCB, are effectively in series with the preamplifiers' inputs, they can serve as antennae to collect interfering signals. Take care to minimize possible sources of interference nearby that may be picked up by these large coupling capacitors.

These C_G capacitors see very little voltage across them so polarized types can be safely used without regard for polarity. We recommend selecting a rated voltage of at least 3.3 V.

C_G Time Constant and Clicks on Gain Change

The C_G coupling capacitors can accumulate charge as a result of stray leakage on the PCB. The 626x incorporates an internal 250 kΩ R_G resistor for the minimum gain setting to provide a means to discharge accumulated charge on C_G. But, at minimum gain, the time constant is approximately two minutes with the recommended 470 µf C_G. Furthermore, it does not take much stray leakage to create significant dc potential across 250 kΩ. So, if the gain is set to minimum for a long time, and there are even small leakage currents on the PCB, audible thumps may result when transitioning from the minimum preamp gain setting to higher gains. This can be minimized with careful attention to PCB cleanliness.

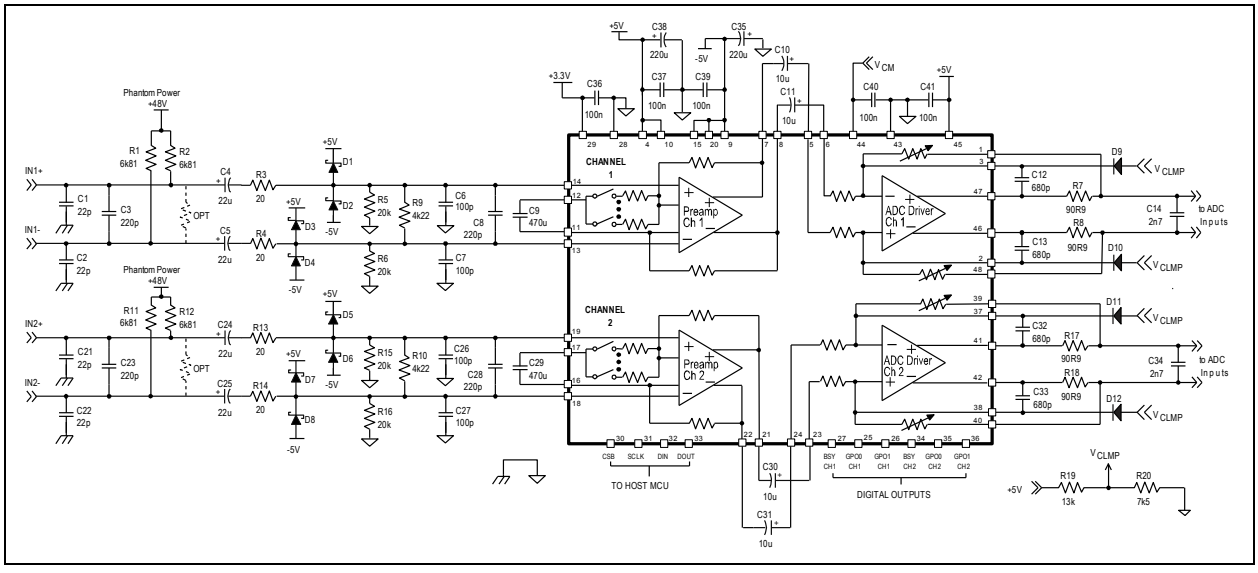


Figure 17. A typical bipolar-supply THAT 626x application circuit.
See also Figure 18 for an alternative ADC anti-aliasing filter configuration.

At power-up, the 626x gain is set by default to the minimum value of -8 dB. As noted above, at the minimum gain setting, the C_G–R_G time constant is about 2 minutes. Until C_G charges (to the input offset voltage of the preamplifier), any gain increase can result in audible pops. To speed up the charging time and minimize audible pop sounds, we recommend that the gain be set to a higher than minimum value for a short period of time after the channel is enabled, while muting the final output of the system (not the 626x internal mute function, which sets the preamp at its minimum gain). Bringing the gain setting to the maximum of 34 dB shortens the time constant to 21 msec with the recommended 470µF C_G capacitors. After a few hundred milliseconds for C_G to acquire its final charge, change gain to a lower value (whatever is desired for the system default) and unmute the system. This will ensure that the C_G capacitors are charged to the proper voltages without causing audible disturbance.

AC Coupling Between Stages

With ±5 V power rails, the preamplifier outputs have a DC level of one V_{BE} below ground, and the ADC driver inputs have a DC level equal to the potential at V_{CM} (normally ~+2.5 V). The ac-coupling capacitors between the stages (C10 and C11) are required to block the common-mode and differential dc-offset voltages of the preamplifier from causing dc currents to flow in the ADC driver input resistors. Since these capacitors see a little over 3 V dc across them, they should be rated at least 6.3 V.

The 10µF coupling capacitors shown result in a highpass cut-off frequency of around 8 Hz (working against the ~2kΩ input impedance of the ADC driver stage). The capacitor values can be increased if a lower cut-off frequency is desired. As noted earlier (see "Gain-Programmable ADC Driver Stage"), matching between these capacitors will affect common-mode rejection (CMR) and power-supply rejection (PSR) at low frequencies. Larger values will improve CMR and PSR at lower frequencies for any given tolerance.

ADC Driver Input Clamp

The 626x ADC driver inputs (pins DI+_CHx and DI-_CHx) are capable of accommodating the full differential and common-mode signal range at the preamp outputs. However, the ADC driver's fully- differential opamp inputs (brought out on pins CFB+_CHx and CFB-_CHx) have a common-mode input range of 1V to +5V. If this common-mode range is exceeded in the negative direction, the opamp's inputs and outputs can get stuck close to ground. Diodes D9 and D10 in Figure 17 clamp the minimum voltage at the ADC driver opamp's inputs to one diode drop below the voltage V_{CLMP}. For V_{CLMP} nominally +1.8V, the diodes ensure that the opamp's inputs do not go below 1V above ground. This ensures that the ADC driver will accept the full $3.8V_P$ common-mode signal swing that can be present at the preamp outputs.

The voltage V_{CLMP} may be generated from a voltage divider between the V_{AD} supply rail (nominally +5V) and ground. In Figure 17, this divider is made up of 13 kΩ and 7.5 kΩ resistors R19 and R20.

Note that the clamp is not needed when powering the 626x from unipolar supplies. See page 18 under "Unipolar Supply Operation".

ADC Driver V_{CM} Input

The V_{CM} input (pin 44) must be tied to a voltage approximately equal to $V_{AD}/2$ (+/-1V). When driving differential-input ADCs, the 626x V_{CM} voltage should be equal to the quiescent common mode voltage of the converter inputs. Most ADCs include a pin where this voltage is available for filtering (often called V_Q or V_{COM}). We recommend connecting this pin on the ADC to the V_{CM} pin on the 626x. (Note that the input impedance at the V_{CM} pin is very high. It will not draw currents that might disturb the ADC's common mode reference.)

Some ADC manufacturers discourage any external connections (except for filter capacitors) to such pins. If this is a concern, we recommend using a discrete voltage divider for V_{CM}, which can be made up of a pair of 100kΩ resistors between V_{AD} and ground filtered with a 1µF capacitor from the junction of the resistors to ground.

Note that the recommendation for V_{CM} is different when powering the 626x from unipolar supplies. See the section "ADC Driver V_{CM} Input" under "Unipolar Supply Operation", page tk.

Phantom Power Protection

Phantom power is required for many condenser microphones. It is connected to the preamp inputs through resistors, R1 and R2, per +48V phantom power standards. THAT recommends the protection circuits as shown in Figure 17 when phantom power is included. R3 and R4 are to limit the current that flows through the preamp inputs during phantom power faults that can occur if one or both of the inputs are shorted to ground while phantom power is on. We recommend that R3 and R4 should be at least 20 Ω to limit destructive currents to under ~2.5A. (Higher values provide more protection by further limiting current flow, but their additional source impedance adds noise.) The protection resistors used should be able to handle the short-term inrush current; many small surface-mount types cannot. With the values shown for C4 and C5, we recommend at least ¼ W resistors.

Together with R3 and R4, Schottky diodes D1~D4 cause C4 or C5 to discharge through them instead of other circuit components, including especially the 626x inputs. Note that the transient current during a phantom power fault can be several amps. These diodes prevent the IC's inputs from significantly exceeding the supply rails. For the best results, D1~D4 should be *low-leakage* Schottky diodes[5], to ensure that they do not spoil the 626x's excellent noise performance.

As mentioned above, we recommend a 220 µF decoupling capacitor between V_{A-} and ground (C35 in

5. We have had good experience with the Nexperia PMEG6020AELPX

Figure 17) when C4 and C5 are as shown at 22 µF. The large 220 µF capacitor absorbs the charge dumped by C4 and/or C5, and keeps the –5 V rail from being pulled excessively negative, which could damage the 626x. If larger values are employed for C4 and C5, then C35 and C38 should be increased proportionately.

C38 on the positive rail, also shown at 220µf, is advisable in order to prevent damage in case the input is connected to another preamp whose phantom power is turned on. Doing so will cause a positive spike in voltage as its input coupling capacitors discharge into the 626x's input protection network.

For further insights into this subject, see the Audio Engineering Society preprint "The 48 Volt Phantom Menace Returns" by Rosalfonso Bortoni and Wayne Kirkwood, presented at the 127th AES Convention (available on THAT's web site), and subsequently published in the Journal of the Audio Engineering Society.

Anti-aliasing Filter Configurations

The most common anti-aliasing filter configuration for driving audio ADCs is shown in Figure 17. Capacitors C12 ~ C14, resistors R7 and R8, and the internal feedback resistors of the ADC driver form a second-order lowpass filter. Since R7 and R8 are inside the amplifier's feedback loop, the closed-loop output impedance remains quite low inside the audio band, but they still serve to isolate the ADC driver's output from the high-frequency charging currents for the typical ADC's switched-capacitor inputs. C14 should be placed physically close to the ADC input pins.

Note that in the 6261, the internal feedback resistors vary in value between 796 Ω at –8 dB ADC driver gain and 1.12 kΩ at –5 dB ADC driver gain, as indicated in Tables 2. This does affect the filter response somewhat. For the values shown, the nominal response for the –8 dB gain case is –3 dB at 350 kHz and –51 dB at 6.144 MHz. The nominal response for the –5 dB gain case is –3 dB at 265 kHz and –54 dB at 6.144 MHz. Both responses are very close to a 2nd-order Butterworth response with the –8 dB case exhibiting less than 0.5 dB of peaking at 164 kHz, while the –5 dB case shows no response peaking. In the 6263 and 6266, the response is the same as that for the 6261 with –8 dB ADC driver gain.

The 626x's ADC driver can also be configured as shown in Figure 18. (For illustration purposes, only one channel is shown.) In this configuration, capacitors C12 and C13 in conjunction with the ADC driver's internal feedback resistors form a single real lowpass pole, while resistors R7 and R8 form a second real lowpass pole with capacitor C14. Again, C14 should be placed close to the ADC input pins.

As noted above, in the 6261, the ADC driver's internal feedback resistors vary, which will have a small effect on the overall filter response. The frequency response for the –8 dB case is –3 dB at 560 kHz and –48 dB at 6.144 MHz. The response of the –5 dB case is –3 dB at 419 kHz and –51 dB at 6.144 MHz. As with the filter shown in Figure 17, for the 6263 and 6266, the response is the same as that for the 6261 with –8 dB ADC driver gain.

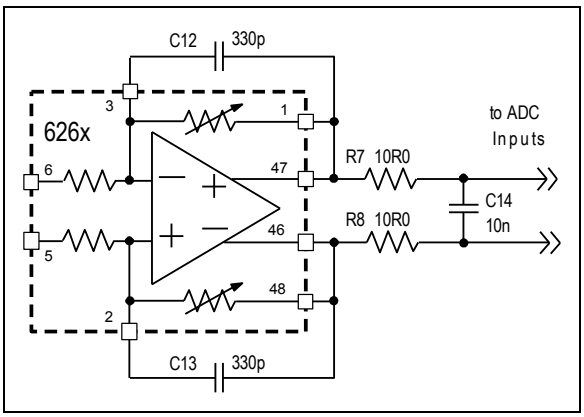


Figure 18. THAT 626x ADC driver in an alternate anti-aliasing filter configuration.

The minimum value for the ADC driver feedback capacitors C12 and C13 is 100 pF. Designers may, of course, choose larger capacitor values to implement the desired filter characteristics.

Supply/Reference Filtering

As shown in Figure 17, THAT recommends a 100nF capacitor to ground on all the supply rails plus the VCM reference (pin 44) for high frequency noise filtering. For best effectiveness, place each 100nF capacitor close to its associated pin in the PCB layout. For rails with multiple pins, e.g., V_{A-} and V_{A+}, only a single 100nF capacitor is needed per supply; connect the capacitors near pins 9 and 10.

In addition to the 100nF high-frequency bypass caps, two 220µF capacitors (C35 and C38) to ground are required on the V_{A-} and V_{A+} preamplifier rails primarily as part of phantom power fault protection (see Phantom Power Protection below).

Zero Crossing Detectors

The integrated zero-crossing detectors (ZCD) may be enabled or disabled for the GAIN and GPO parameters independently (see Table 8). Note, however, that both channels' ZCDs are enabled or disabled simultaneously. When enabled, each detector prevents gain and/or GPO changes from occurring until either a) the differential output signal amplitude in the associated channel is within ±10 mV of 0 V, or b) the timeout (approximately 22 ms) has elapsed, whichever occurs first. When the GMD or GPOMD bits are zero (Table 9), Gain and GPO updates are made immediately following a rising edge on the $\overline{CS}$ pin. When GMD and GPOMD are logic high, updates are made on the next output signal zero-crossing after a rising edge on the $\overline{CS}$ pin.

The choice between "immediate" vs "zero crossing" mode depends on the application. Immediate mode has the advantage of providing gain updates with short and deterministic latency, whereas zero crossing mode has the advantage of minimizing glitches and zipper noise.

When using the zero-crossing detector, an additional consideration is that if a second gain command

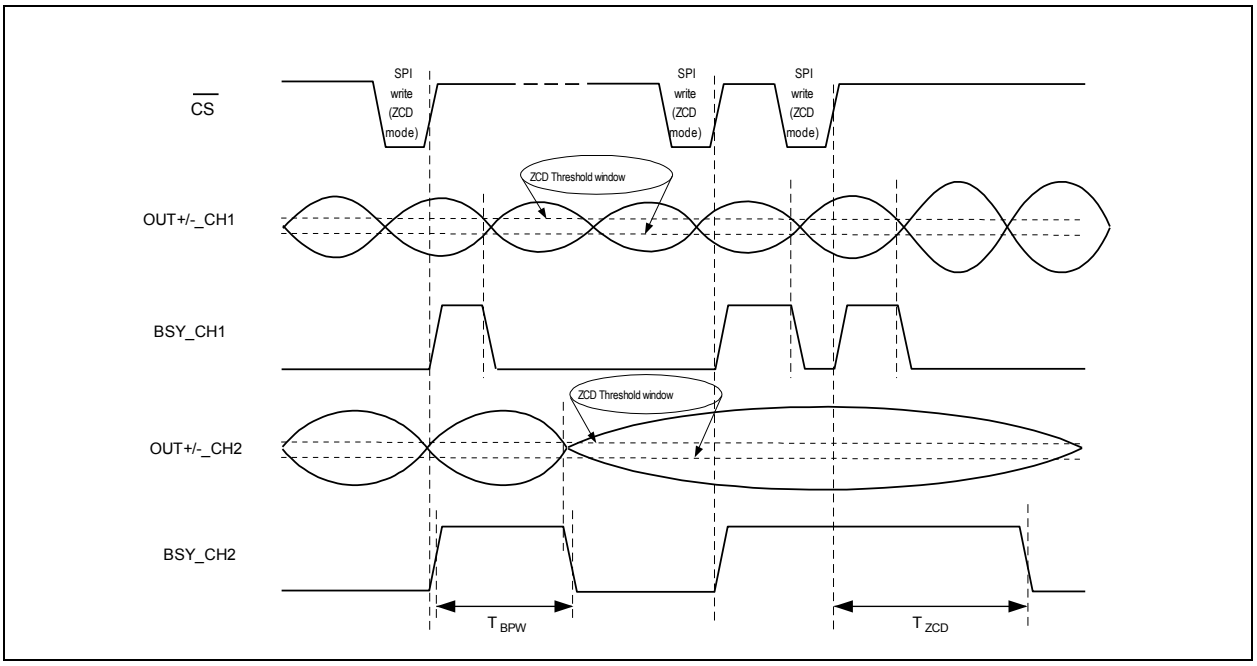


Figure 19. Timing diagram for the Zero-Crossing Detector and Busy Pin operation.

is sent to the part before the first gain command takes effect (either through a zero-crossing or timing out), the timeout resets, and only the second gain command takes effect. In extreme cases, if a series of commands is sent, each within the timeout period, and no zero-crossing is reached before each gain command's timeout, only the last gain command will take effect. Accordingly, we recommend that when using the zero-crossing detector, individual gain commands should be separated by at least the timeout period.

Busy (BSY pins)

The BSY pin for its associated channel is asserted high when a gain update or GPO update for that channel is pending a zero-crossing. This pin may be monitored by the host microcontroller (e.g. connected to an external interrupt pin) in order to hold off a new gain command until the previous gain command has been executed.

If finer or additional gain steps are implemented in external processing (DSP or in additional analog circuitry) the BSY signal can be employed to synchronize external gain changes with those implemented by the 626x. This is important when the interpolated gain "wraps" from maximum to minimum as, for example, each of the 6266's 6dB steps occurs. Note that latency in A/D conversion must be considered when attempting to synchronize digital with analog gain updates.

Figure 19 is a timing diagram for the ZCD and busy pin operation. T_{BPW} is the pulse-width of the busy signal, which depends on the ADC driver output signal amplitude and when the ZCD function is enabled. When the ADC driver output stays high, the ZCD enters time-out status and T_{BPW} equals to T_{ZCD}, which is the time-out time.

Power-on Reset

The 626x has an on-chip power-on reset circuit which resets the SPI control registers to their default state after power-up. However, if the +3.3 V supply is not discharged to below 0.3 V before coming back up to the nominal level, the device may enter an unknown random state. (This might happen if a product using a 626x loses power momentarily and comes back soon after.) To avoid situations like this, it is good practice to send a command to the 626x after each power-up to ensure that the device is in a known state.

Unipolar Supply Operation

As shown in Figure 20, the 626x preamps can also be powered from +10V/0V. In this case (once again following the channel 1 reference designators), the input bias resistors (R5 and R6) are biased to +5V (instead of ground as with ±5V rails). The power supplies for the rest of 626x circuitry stay unchanged (at +5V for the ADC driver and +3.3V for the logic).

Provided that the rails are generated and filtered properly, there is no performance degradation using either of the two power-supply schemes. The major changes for unipolar operation are these:

- Use non-polar capacitors at the input for C4 and C5;
- Reverse the polarity of the inter-stage-coupling capacitors C10 and C11;
- AC couple the ADC Driver outputs (C44 and C45;
- Change the V_{CM} reference voltage from +2.5V to +3.1V and;
- Delete clamp diodes D9 and D10 and the V_{CLMP} voltage divider R19 and R20 (from Figure 17) as these are not required for unipolar operation.

AC Coupling (Unipolar Supplies)

The potential at the inputs in Figure 20 will vary between +48 V and 0 V depending on whether phantom power is on or not, while the preamp's inputs (at the right side of C4 and C5) are biased at +5 V. These capacitors must be nonpolar types, rated for at least 50V.

Further, the DC level of the preamplifier output is one V_{BE} below +5V Filt (thus about +4.3 V), while the ADC driver input's DC level is at V_{CM} (nominally +3.1 V). Hence, the ac-coupling capacitors between the preamp and ADC driver stages (C10 and C11) are reversed in polarity from those in Figure 17. We recommend these capacitors be rated at least 3.3 V.

+5V Filt for the Preamp's DC Pedestal (Unipolar Supplies)

While noise or interference at the "+5V Filt" node in Figure 20 nominally appears only in common-mode and should be rejected by the CMRR of the ADC driver stage, that rejection is subject to the limitations of passive component matching as well the 626x's inherent CMRR. Accordingly, we recommend that +5V Filt be derived from the +5V supply with the additional filtering of R21 and C43.

ADC Driver V_{CM} Input (Unipolar Supplies)

When powered from a unipolar supply, the V_{CM} input (pin 44) should be tied to approximately 3.1V in order to allow the ADC driver's outputs to swing the full range of 2Vrms. The divider that generates V_{CM} can be made using a 75 kΩ resistor from V_{AD} to V_{CM} and a 130 kΩ resistor from V_{CM} to ground along with a 1μF capacitor from V_{CM} to ground (Figure 20).

As a result of the above arrangement, the ADC driver output will have a common mode level of 3.1V, which is different from the typical 2.5V ADC IC input common mode voltage. Hence, AC coupling capacitors, C44 and C45 in Figure 20, are added to block the DC voltage. Along with the differential input impedance of the ADC's input, these capacitors form a high-pass filter. With the typical 3kΩ ADC input differential resistance the 22μf capacitors show results in a high-pass cut-off frequency of 4.8Hz. Customers may choice a value based on their applications.

ADC Driver Diode Clamps (Unipolar Supplies)

Because the ADC driver Vcm voltage is set to +3.1V for unipolar applications, the full common-mode swing output swing from the preamp cannot force the ADC driver opamp inputs below the minimum allowable level. Hence, diodes D9 and D10 (and the associated voltage divider) as in Figure 17 are not needed when the 626x is powered by unipolar supplies.

Phantom Power Protection and Power Supply Filtering (Unipolar Supplies)

Most of the components used for phantom power protection and power supply bypassing in the unipolar supply circuit are the same as for bipolar supplies. However, with unipolar supplies, as shown in Figure 20, only C38 and C37 are needed, because V_{A-} is connected to ground.

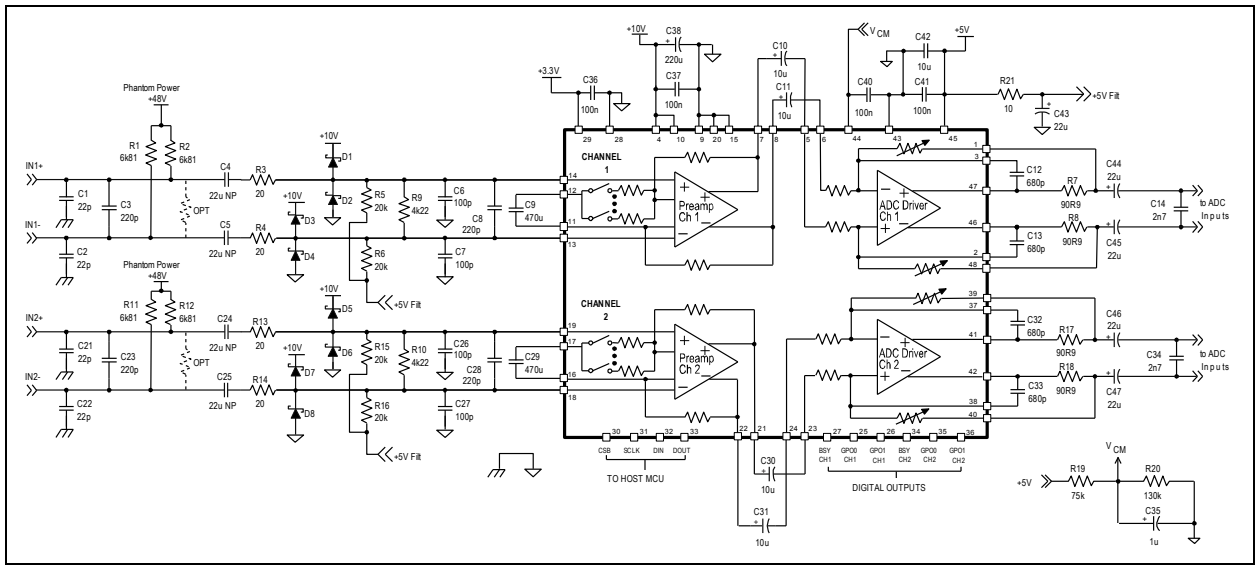


Figure 20. A typical unipolar-supply THAT626x application circuit.
See also Figure 18 for an alternative ADC anti-aliasing filter configuration.

Package and Soldering Information

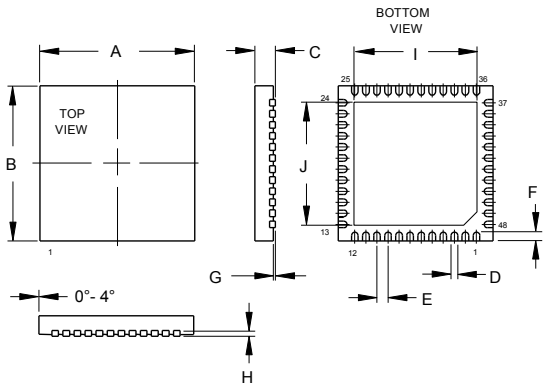
Package Characteristics

Parameter	Symbol	Conditions	Spec	Units
Package Style		See Fig. 21 for dimensions	7 X 7 mm 48 Pin QFN	
Thermal Resistance	θ_{JA}	QFN package soldered to board[6]	35	ºC/W
Environmental Regulation Compliance			Complies with RoHS 2 requirements	
Moisture Sensitivity Level	MSL	JEDEC JESD22-A113-D (250 ºC	MSL-3	

The THAT626x is available in a 7mm x 7mm 48-pin QFN package. The package dimensions are shown in Figure 21. Pinouts are given in Table 1.

The 626x is lead free and RoHS-2 compliant.

Material Declaration Data Sheets on the parts are available at our web site, www.thatcorp.com or upon request. For ordering information, see Table 10.



SYM	MM		Mils	
	MIn	Max	MIn	Max
A	6.9	7.1	271.65	279.53
B	6.9	7.1	271.65	279.53
C	0.80	1.00	31.50	39.37
D	0.2	0.3	7.87	11.81
E	0.5 BSC		19.69 BSC	
F	0.35	0.45	13.78	17.72
G	0.00	0.05	0.00	1.97
H	0.175	0.225	6.89	8.86
I	5.31	5.6	209.06	220.47
J	5.31	5.6	209.06	220.47

Figure 21. QFN-48 Package Dimensions

Package	Order Number
48 pin QFN	6261N48-U
	6263N48-U
	6266N48-U

Table 10. Ordering Information

[6] Two layer board used for characterization.