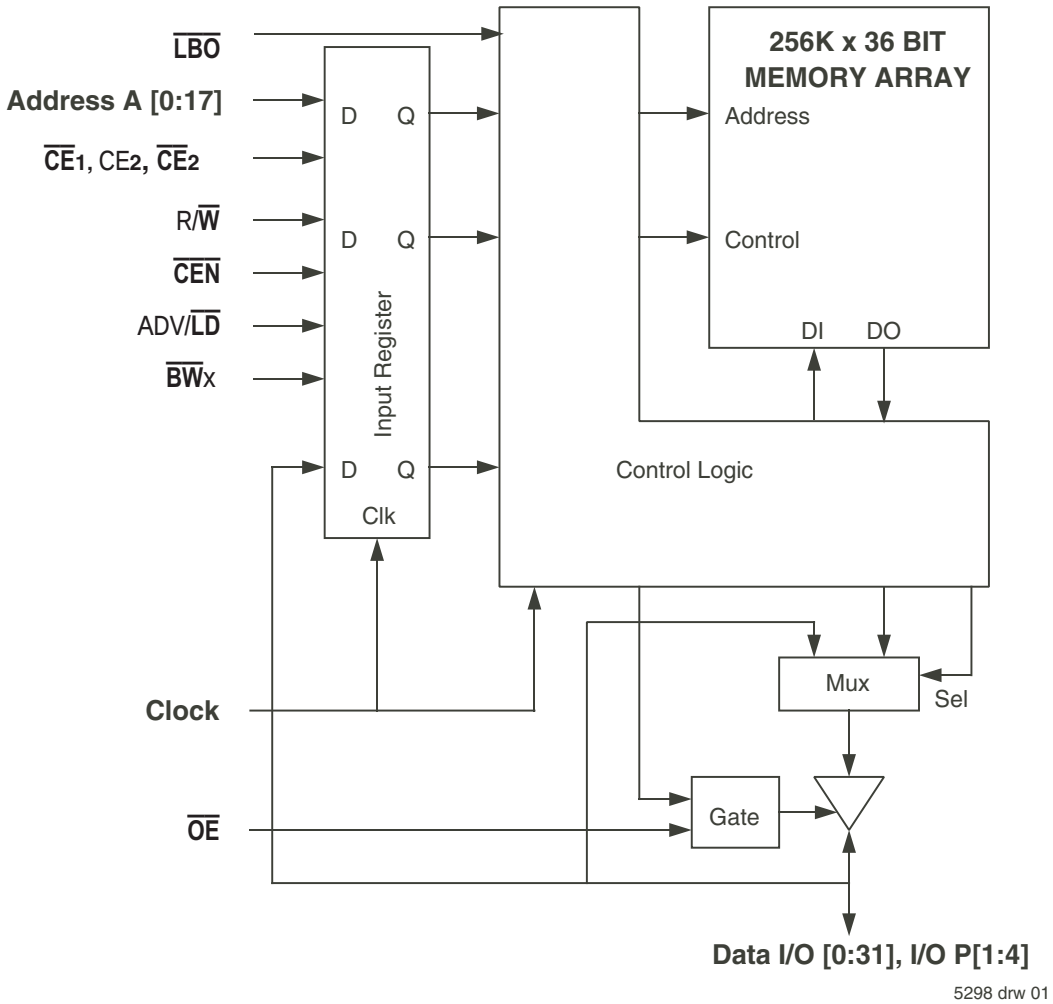
256K x 36, 512K x 18
3.3V Synchronous ZBT™ SRAMs
3.3V I/O, Burst Counter
Flow-Through Outputs

71V65703
71V65903

Features

- 256K x 36, 512K x 18 memory configurations
- Supports high performance system speed - 100 MHz (7.5 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- 4-word burst capability (Interleaved or linear)
- Individual byte write ($\overline{BW}_1$ - $\overline{BW}_4$) control (May tie active)
- Three chip enables for simple depth expansion
- 3.3V power supply (±5%)
- 3.3V (±5%) I/O Supply (V_{DDQ})
- Power down controlled by ZZ input
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram — 256K x 36



5298 drw 01

Description

The IDT71V65703/5903 are 3.3V high-speed 9,437,184-bit (9 Megabit) synchronous SRAMs organized as 256K x 36 / 512K x 18. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and on the next clock cycle the associated data cycle occurs, be it read or write.

The IDT71V65703/5903 contain address, data-in and control signal registers. The outputs are flow-through (no output data register). Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

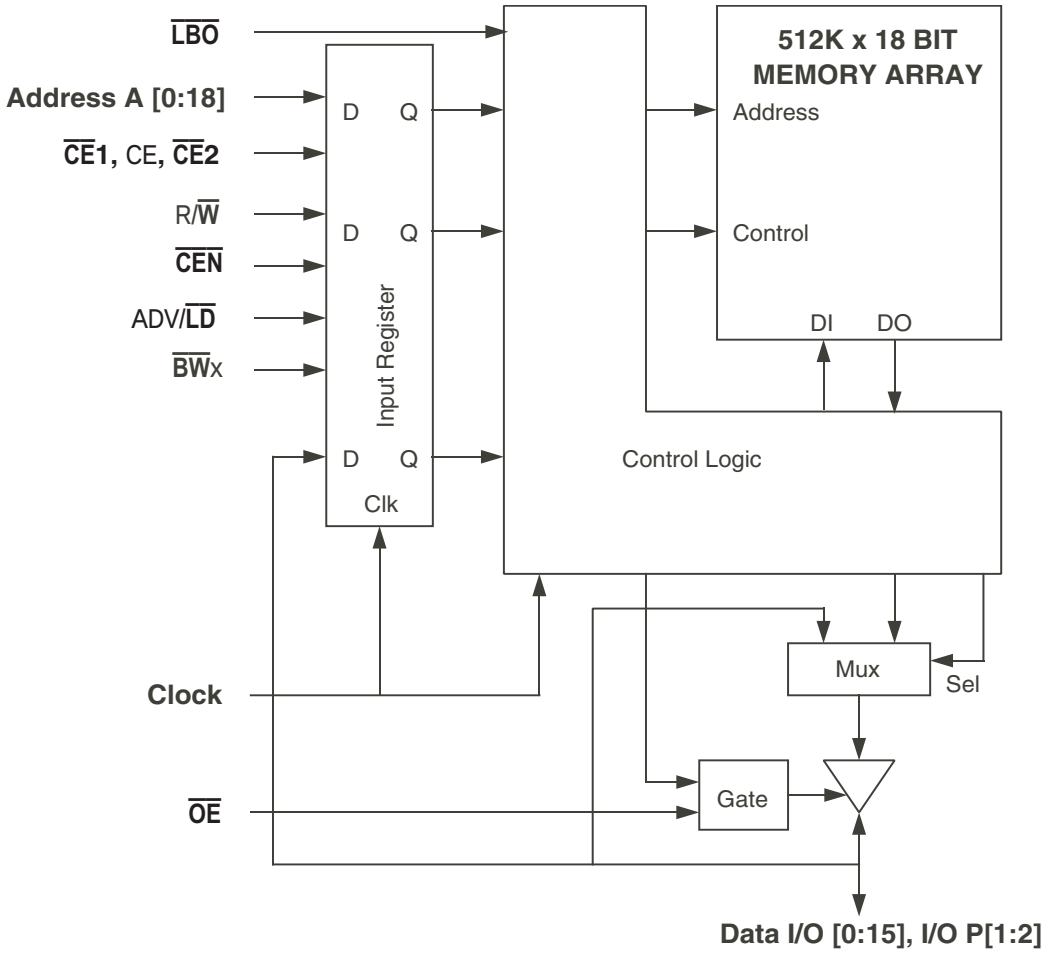
A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V65703/5903 to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state one cycle after the chip is deselected or a write is initiated.

The IDT71V65703/5903 have an on-chip burst counter. In the burst mode, the IDT71V65703/5903 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V65703/5903 SRAMs utilize a high-performance CMOS process and are packaged in a JEDEC Standard 14mm x 20mm 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Functional Block Diagram — 512K x 18



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Pin Description Summary

A_0-A_{18}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance Burst Address/Load New Address	Input	Synchronous
$\overline{LBO}$	Linear/Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/OP_1-I/OP_4	Data Input/Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5298 tbl 01

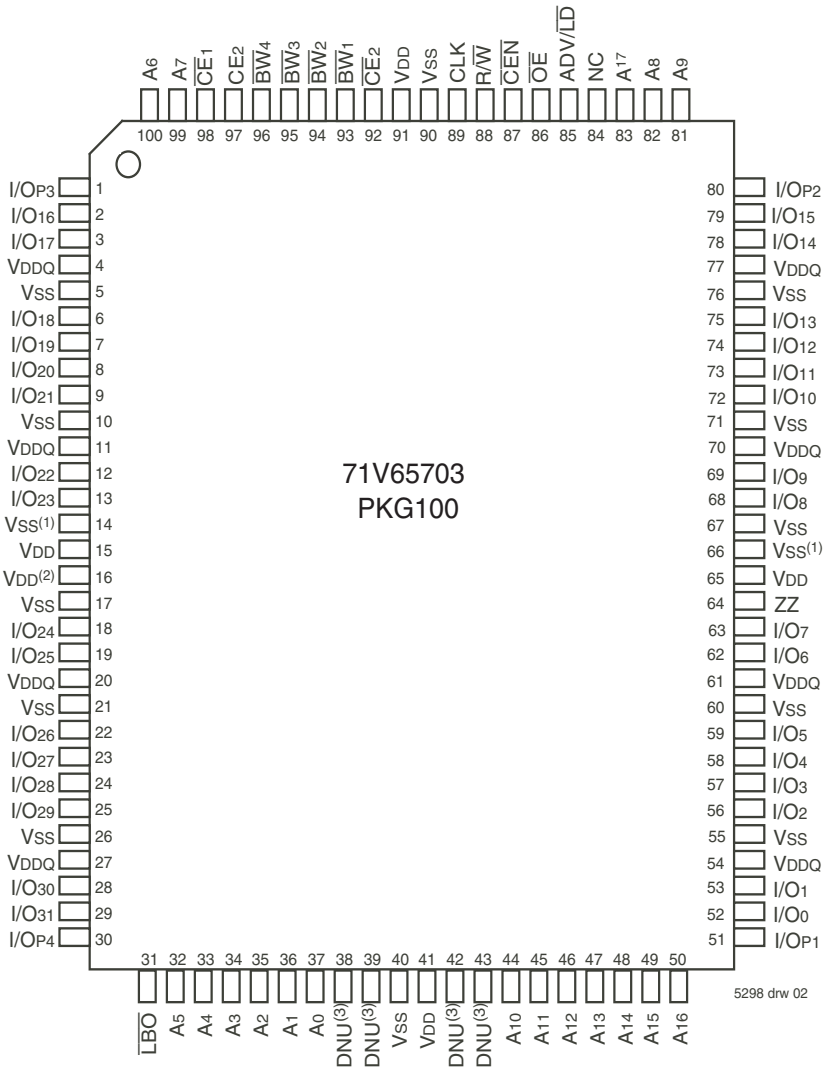
Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{18}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place one clock cycle later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW_1}$-$\overline{BW_4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BW_1}$-$\overline{BW_4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE_1}$ and $\overline{CE_2}$ are used with CE_2 to enable the IDT71V65703/5903 ($\overline{CE_1}$ or $\overline{CE_2}$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a one cycle deselect, i.e., the data bus will tri-state one clock cycle after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE_1}$ and $\overline{CE_2}$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE_1}$ and $\overline{CE_2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V65703/5903. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input, and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the 71V65703/5903. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V65703/5903 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	3.3V I/O supply.
V_{SS}	Ground	N/A	N/A	Ground.

5298 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration — 256K x 36, PKG100[4]

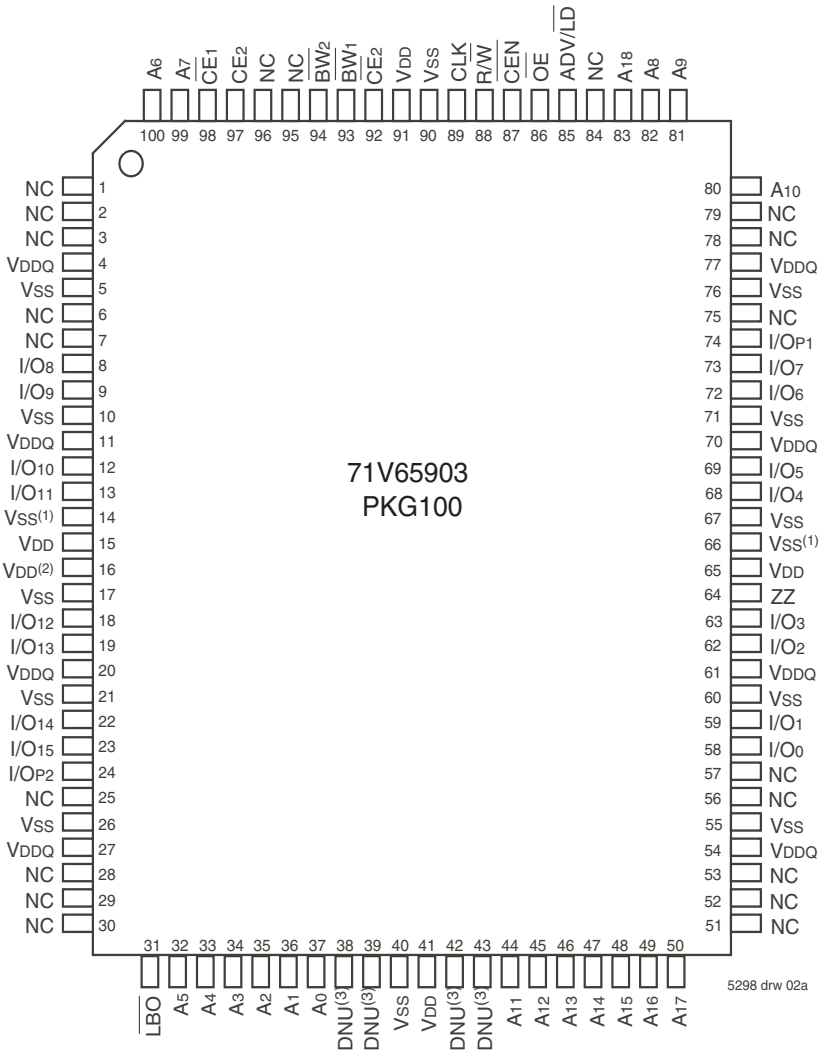


Top View
100 TQFP

NOTES:

1. Pins 14 and 66 do not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. Pin 16 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
3. DNU = Do not use. Pins 38, 39, 42 and 43 can be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
4. This text does not indicate the orientation of the actual part-marking.

Pin Configuration — 512K x 18, PKG100(4)



Top View
100 TQFP

NOTES:

1. Pins 14 and 66 do not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. Pin 16 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
3. DNU = Do not use. Pins 38, 39, 42 and 43 can be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
4. This text does not indicate the orientation of the actual part-marking.

Pin Configuration — 256K x 36, BG119, BGG119(4)

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	NC	A8	A16	V_{DDQ}
B	NC	$\overline{CE}_2$	A3	ADV/$\overline{LD}$	A9	$\overline{CE}_2$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O_{16}	I/O_{P3}	V_{SS}	NC	V_{SS}	I/O_{P2}	I/O_{15}
E	I/O_{17}	I/O_{18}	V_{SS}	$\overline{CE}_1$	V_{SS}	I/O_{13}	I/O_{14}
F	V_{DDQ}	I/O_{19}	V_{SS}	$\overline{OE}$	V_{SS}	I/O_{12}	V_{DDQ}
G	I/O_{20}	I/O_{21}	$\overline{BW}_3$	A17	$\overline{BW}_2$	I/O_{11}	I/O_{10}
H	I/O_{22}	I/O_{23}	V_{SS}	R/$\overline{W}$	V_{SS}	I/O_9	I/O_8
J	V_{DDQ}	V_{DD}	V_{DD}(2)	V_{DD}	V_{SS}(1)	V_{DD}	V_{DDQ}
K	I/O_{24}	I/O_{26}	V_{SS}	CLK	V_{SS}	I/O_6	I/O_7
L	I/O_{25}	I/O_{27}	$\overline{BW}_4$	NC	$\overline{BW}_1$	I/O_4	I/O_5
M	V_{DDQ}	I/O_{28}	V_{SS}	$\overline{CEN}$	V_{SS}	I/O_3	V_{DDQ}
N	I/O_{29}	I/O_{30}	V_{SS}	A1	V_{SS}	I/O_2	I/O_1
P	I/O_{31}	I/O_{P4}	V_{SS}	A0	V_{SS}	I/O_{P1}	I/O_0
R	NC	A5	$\overline{LBO}$	V_{DD}	V_{SS}(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	$\overline{ZZ}$
U	V_{DDQ}	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	V_{DDQ}

Top View

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Pin Configuration — 512K x 18, BG119, BGG119(4)

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	NC	A8	A16	V_{DDQ}
B	NC	CE_2	A3	ADV/$\overline{LD}$	A9	$\overline{CE}_2$	NC
C	NC	A7	A2	V_{DD}	A13	A17	NC
D	I/O_8	NC	V_{SS}	NC	V_{SS}	I/O_{P1}	NC
E	NC	I/O_9	V_{SS}	$\overline{CE}_1$	V_{SS}	NC	I/O_7
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	I/O_6	V_{DDQ}
G	NC	I/O_{10}	$\overline{BW}_2$	A18	V_{SS}	NC	I/O_5
H	I/O_{11}	NC	V_{SS}	R/$\overline{W}$	V_{SS}	I/O_4	NC
J	V_{DDQ}	V_{DD}	V_{DD}(2)	V_{DD}	V_{SS}(1)	V_{DD}	V_{DDQ}
K	NC	I/O_{12}	V_{SS}	CLK	V_{SS}	NC	I/O_3
L	I/O_{13}	NC	V_{SS}	NC	$\overline{BW}_1$	I/O_2	NC
M	V_{DDQ}	I/O_{14}	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	I/O_{15}	NC	V_{SS}	A1	V_{SS}	I/O_1	NC
P	NC	I/O_{P2}	V_{SS}	A0	V_{SS}	NC	I/O_0
R	NC	A5	$\overline{LBO}$	V_{DD}	V_{SS}(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	$\overline{ZZ}$
U	V_{DDQ}	DNU(3)	DNU(3)	DNU(3)	DNU(3)	DNU(3)	V_{DDQ}

Top View

5298 drw 13b

NOTES:

1. R5 and J5 do not have to be directly connected to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. J3 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
3. DNU = Do not use. Pins U2, U3, U4, U5 and U6 can be left unconnected, tied LOW (V_{SS}), or tied HIGH (V_{DD}).
4. This text does not indicate the orientation of the actual part-marking.

Pin Configuration — 256K x 36, BQ165, BQG165(4)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}_1$	$\overline{BW}_3$	$\overline{BW}_2$	$\overline{CE}_2$	$\overline{CEN}$	ADV/$\overline{LD}$	A17	A8	NC
B	NC	A6	CE2	$\overline{BW}_4$	$\overline{BW}_1$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VSS(1)	VDD(2)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	DNU(3)	NC	VSS(1)	VSS	VDDQ	NC	I/OP1
P	NC	NC	A5	A2	DNU(3)	A1	DNU(3)	A10	A13	A14	NC
R	$\overline{LBO}$	NC	A4	A3	DNU(3)	A0	DNU(3)	A11	A12	A15	A16

5298 tbl 25a

Pin Configuration — 512K x 18, BQ165, BQG165(4)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	$\overline{CE}_1$	$\overline{BW}_2$	NC	$\overline{CE}_2$	$\overline{CEN}$	ADV/$\overline{LD}$	A18	A8	A10
B	NC	A6	CE2	NC	$\overline{BW}_1$	CLK	R/$\overline{W}$	$\overline{OE}$	NC	A9	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VSS(1)	VDD(2)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	DNU(3)	NC	VSS(1)	VSS	VDDQ	NC	NC
P	NC	NC	A5	A2	DNU(3)	A1	DNU(3)	A11	A14	A15	NC
R	$\overline{LBO}$	NC	A4	A3	DNU(3)	A0	DNU(3)	A12	A13	A16	A17

5298 tbl 25b

NOTES:
1. Pins H1 and N7 do not have to be connected directly to VSS as long as the input voltage is ≤ VIL.
2. Pin H2 does not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
3. DNU = Do not use. Pins P5, R5, P7, R7 and N5 can be left unconnected, tied LOW (VSS), or tied HIGH (VDD).
4. This text does not indicate the orientation of the actual part-marking.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	V_{DD} + 0.3	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DDQ} + 0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

5298 tbl 04

NOTE:
1. V_{IL} (min.) = –1.0V for pulse width less than $t_{CYC}/2$, once per cycle.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature[1]	V_{SS}	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

5298 tbl 05

NOTE:
1. T_A is the "instant on" case temperature.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}[4,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}[5,6]	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A[7]	Commercial	0 to +70	°C
	Industrial	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5298 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

100 TQFP Capacitance[1]

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5298 tbl 07

165 fBGA Capacitance[1]

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5298 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

119 BGA Capacitance[1]

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5298 tbl 07a

Synchronous Truth Table(1)

$\overline{CEN}$	R/$\overline{W}$	$\overline{CE}_1$,$\overline{CE}_2$(5)	ADV/$\overline{LD}$	BWx	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (One cycle later)
L	L	L	L	Valid	External	X	LOAD WRITE	D(7)
L	H	L	L	X	External	X	LOAD READ	Q(7)
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)(2)	D(7)
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)(2)	Q(7)
L	X	H	L	X	X	X	DESELECT or STOP(3)	HIZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HIZ
H	X	X	X	X	X	X	SUSPEND(4)	Previous Value

5298 tbl 08

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{LD}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{W}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{W}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{CE}_1$, or $\overline{CE}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{LD}$ is sampled low at rising edge of clock. The data bus will tri-state one cycle after deselect is initiated.
4. When $\overline{CEN}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H on these chip enable pins. The chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z during device power-up.
7. Q - data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

OPERATION	R/$\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$(3)	$\overline{BW}_4$(3)
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O_{P1})(2)	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O_{P2})(2)	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O_{P3})(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O_{P4})(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5298 tbl 09

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for x18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5298 tbl 10

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

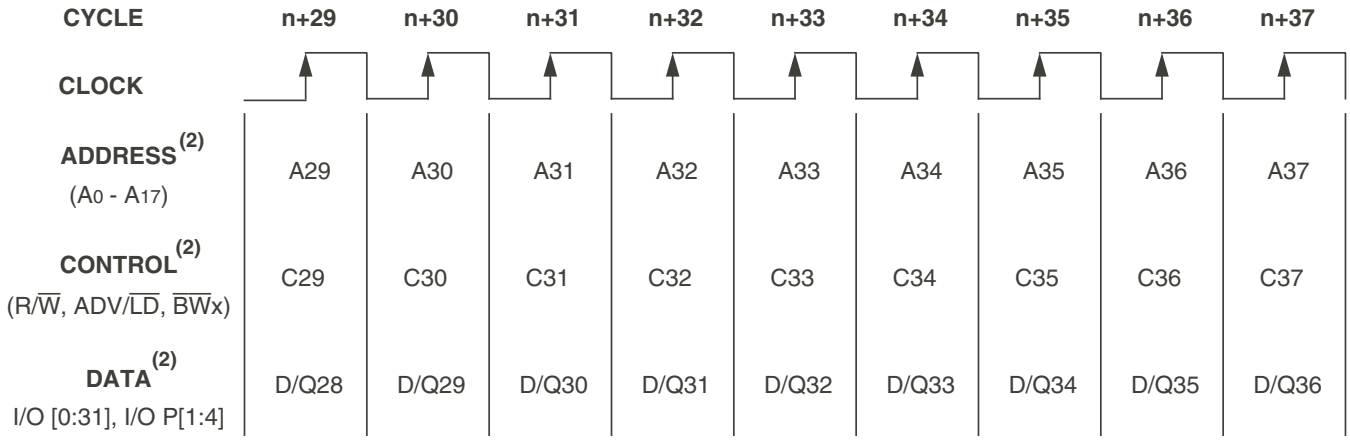
Linear Burst Sequence Table ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5298 tbl 11

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram(1)



5298 drw 03

NOTES:
1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2 and $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	D_1	Load read
n+1	X	X	H	X	L	X	L	Q_0	Burst read
n+2	A_1	H	L	L	L	X	L	Q_{0+1}	Load read
n+3	X	X	L	H	L	X	L	Q_1	Deselect or STOP
n+4	X	X	H	X	L	X	X	Z	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	L	Q_2	Burst read
n+7	X	X	L	H	L	X	L	Q_{2+1}	Deselect or STOP
n+8	A_3	L	L	L	L	L	X	Z	Load write
n+9	X	X	H	X	L	L	X	D_3	Burst write
n+10	A_4	L	L	L	L	L	X	D_{3+1}	Load write
n+11	X	X	L	H	L	X	X	D_4	Deselect or STOP
n+12	X	X	H	X	L	X	X	Z	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	D_5	Load read
n+15	A_7	L	L	L	L	L	L	Q_6	Load write
n+16	X	X	H	X	L	L	X	D_7	Burst write
n+17	A_8	H	L	L	L	X	X	D_{7+1}	Load read
n+18	X	X	H	X	L	X	L	Q_8	Burst read
n+19	A_9	L	L	L	L	L	L	Q_{8+1}	Load write

5298 tbl 12

NOTES:
1. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5298 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Burst Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+2	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+5	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+6	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+7	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5298 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	D_0	Write to Address A_0

5298 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Burst Write Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+2	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+5	A_1	L	L	L	L	L	X	D_0	Address A_0 Write, Inc. Count
n+6	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+7	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5298 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Read Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	AddressA_0 and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out, Load A_1
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_1	Address A_1 Read out, Load A_2
n+6	A_3	H	L	L	L	X	L	Q_2	Address A_2 Read out, Load A_3
n+7	A_4	H	L	L	L	X	L	Q_3	Address A_3 Read out, Load A_4

5298 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Write Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE_1}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address A_0 and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	D_0	Write data D_0, Load A_1.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_1	Write Data D_1, Load A_2
n+6	A_3	L	L	L	L	L	X	D_2	Write Data D_2, Load A_3
n+7	A_4	L	L	L	L	L	X	D_3	Write Data D_3, Load A_4

5298 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE_2}$ timing transition is identical to $\overline{CE_1}$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE_1}$ and $\overline{CE_2}$ signals.

Read Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}_1$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O(3)	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address A_0 and Control meet setup.
n+3	X	X	L	H	L	X	L	Q_0	Address A_0 read out, Deselected.
n+4	A_1	H	L	L	L	X	X	Z	Address A_1 and Control meet setup.
n+5	X	X	L	H	L	X	L	Q_1	Address A_1 read out, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address A_2 and Control meet setup.
n+8	X	X	L	H	L	X	L	Q_2	Address A_2 read out, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5298 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}_2$ timing transition is identical to $\overline{CE}_1$ signal. CE_2 timing transition is identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals.
3. Device outputs are ensured to be in High-Z during device power-up.

Write Operation with Chip Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address A_0 and Control meet setup
n+3	X	X	L	H	L	X	X	D_0	Data D_0 Write In, Deselected.
n+4	A_1	L	L	L	L	L	X	Z	Address A_1 and Control meet setup
n+5	X	X	L	H	L	X	X	D_1	Data D_1 Write In, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address A_2 and Control meet setup
n+8	X	X	L	H	L	X	X	D_2	Data D_2 Write In, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

5298 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LI}\|$	$\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +8mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -8mA, V_{DD} = Min.	2.4	—	V

NOTE:
5298 tbl 21

1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	7.5ns		8ns		8.5ns		Unit
			Com'l	Ind	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	275	295	250	60	225	60	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	40	60	40	60	40	60	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	105	125	100	120	95	115	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	40	60	40	60	40	60	mA
I_{ZZ}	Full Sleep Mode Supply Current	Device Selected, Outputs Open, $\overline{CEN} \leq V_{IL}$, V_{DD} = Max., ZZ $\geq V_{HD}$ $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	40	60	40	60	40	60	mA

NOTES:
5298 tbl 22

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.

AC Test Load

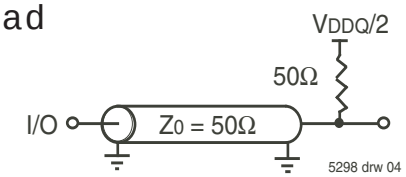


Figure 1. AC Test Load

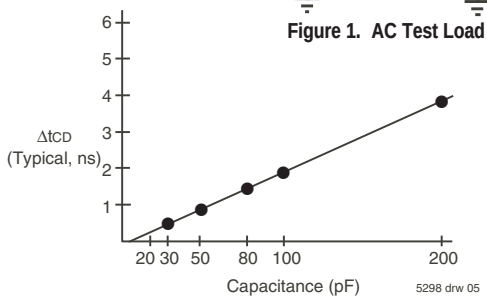


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1

5298 tbl 23

AC Electrical Characteristics

(VDD = 3.3V±5%, Commercial and Industrial Temperature Ranges)

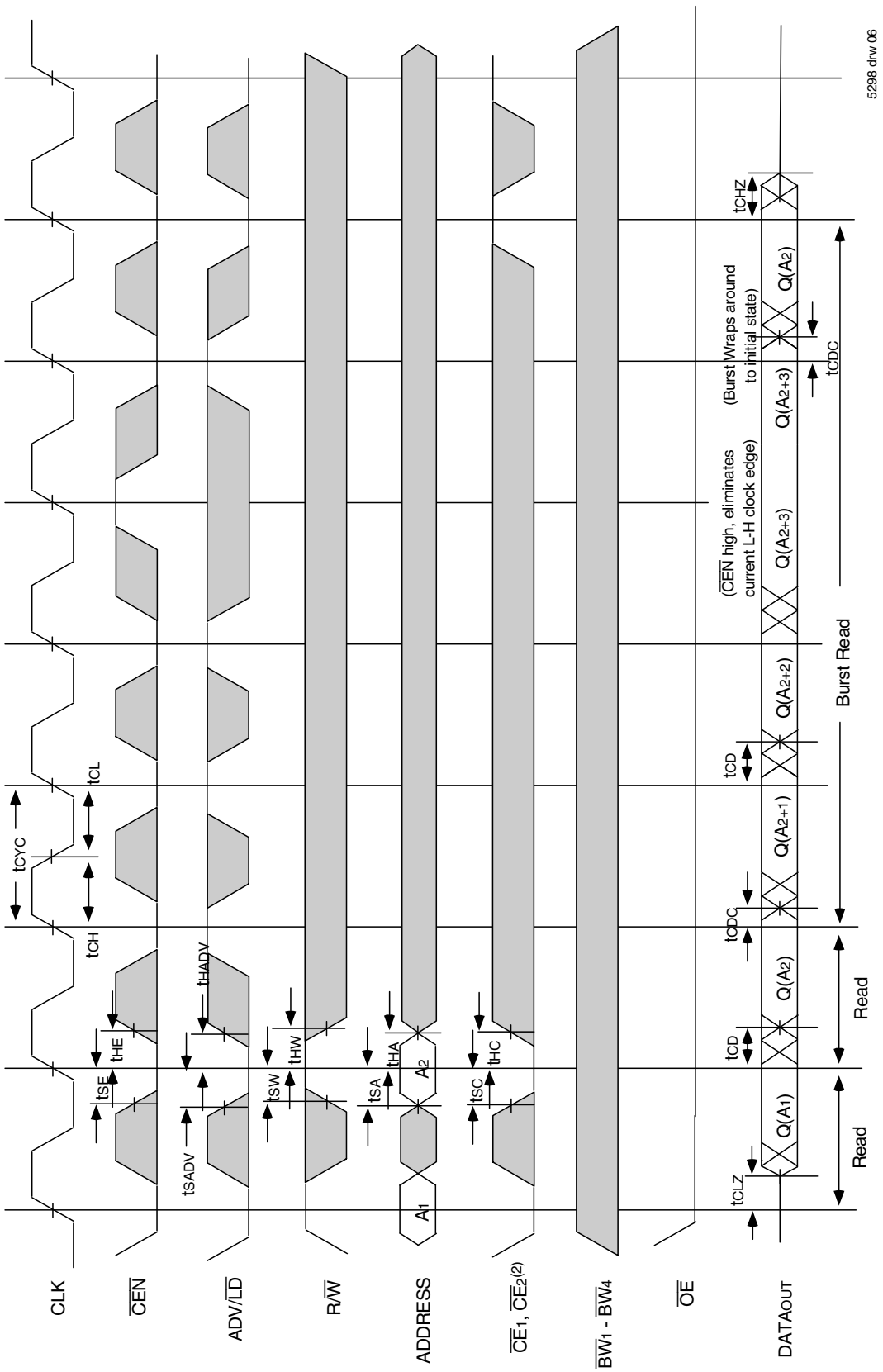
Symbol	Parameter	7.5ns		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	10	—	10.5	—	11	—	ns
t_{CH}(1)	Clock High Pulse Width	2.5	—	2.7	—	3.0	—	ns
t_{CL}(1)	Clock Low Pulse Width	2.5	—	2.7	—	3.0	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	2	—	ns
t_{CLZ}(2,3,4)	Clock High to Output Active	3	—	3	—	3	—	ns
t_{CHZ}(2,3,4)	Clock High to Data High-Z	—	5	—	5	—	5	ns
t_{OE}	Output Enable Access Time	—	5	—	5	—	5	ns
t_{OLZ}(2,3)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(2,3)	Output Enable High to Data High-Z	—	5	—	5	—	5	ns
Set Up Times								
t_{SE}	Clock Enable Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SA}	Address Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SD}	Data In Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	2.0	—	2.0	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	2.0	—	2.0	—	2.0	—	ns
Hold Times								
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	ns

5298 tbl 24

NOTES:

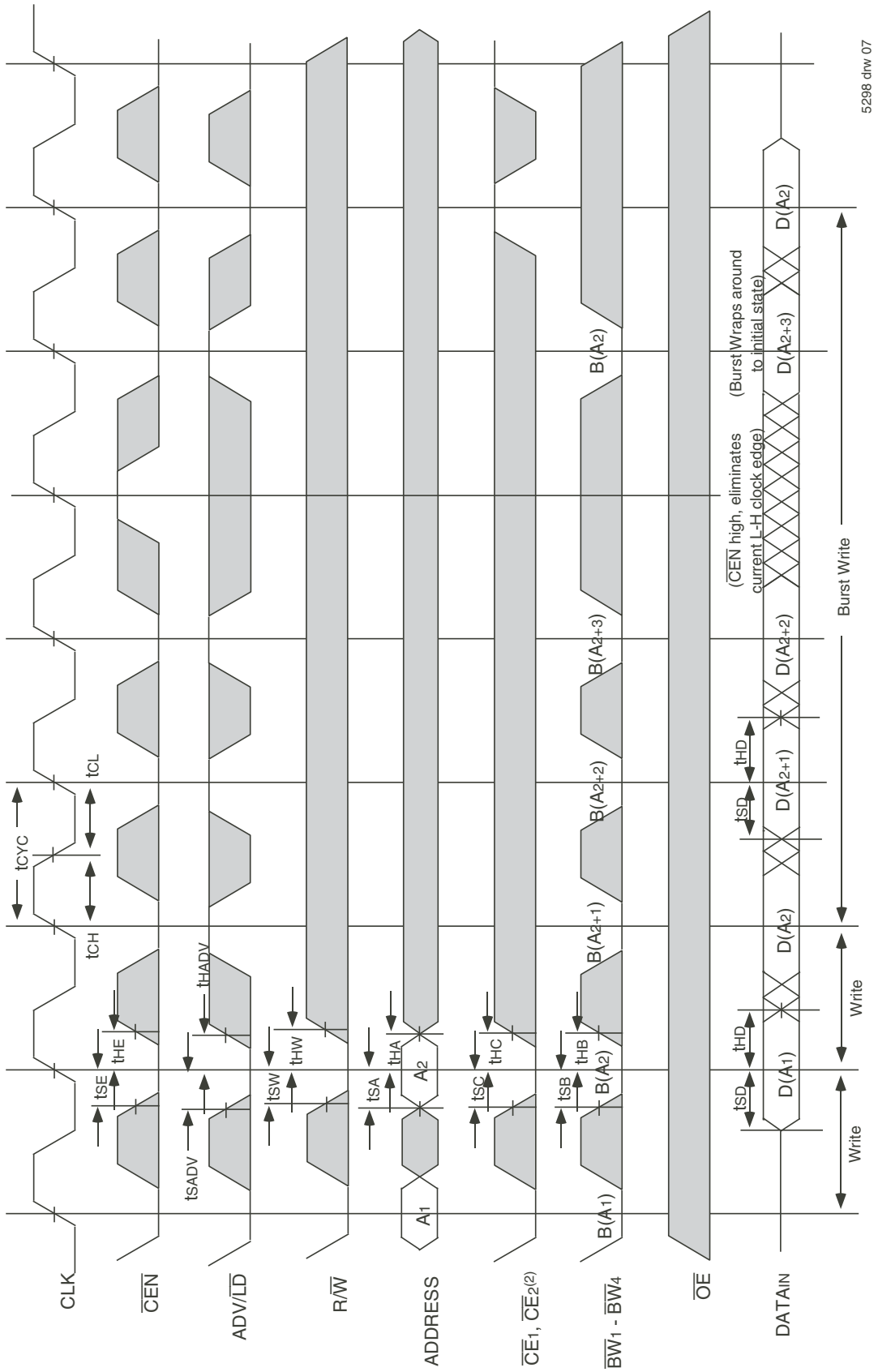
1. Measured as HIGH above 0.6VDDQ and LOW below 0.4VDDQ.
2. Transition is measured ±200mV from steady-state.
3. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
4. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).

Timing Waveform of Read Cycle(1,2,3,4)



NOTES:
1. Q (A1) represents the first output from the external address A1. Q (A2) represents the first output from the external address A2; Q (A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.

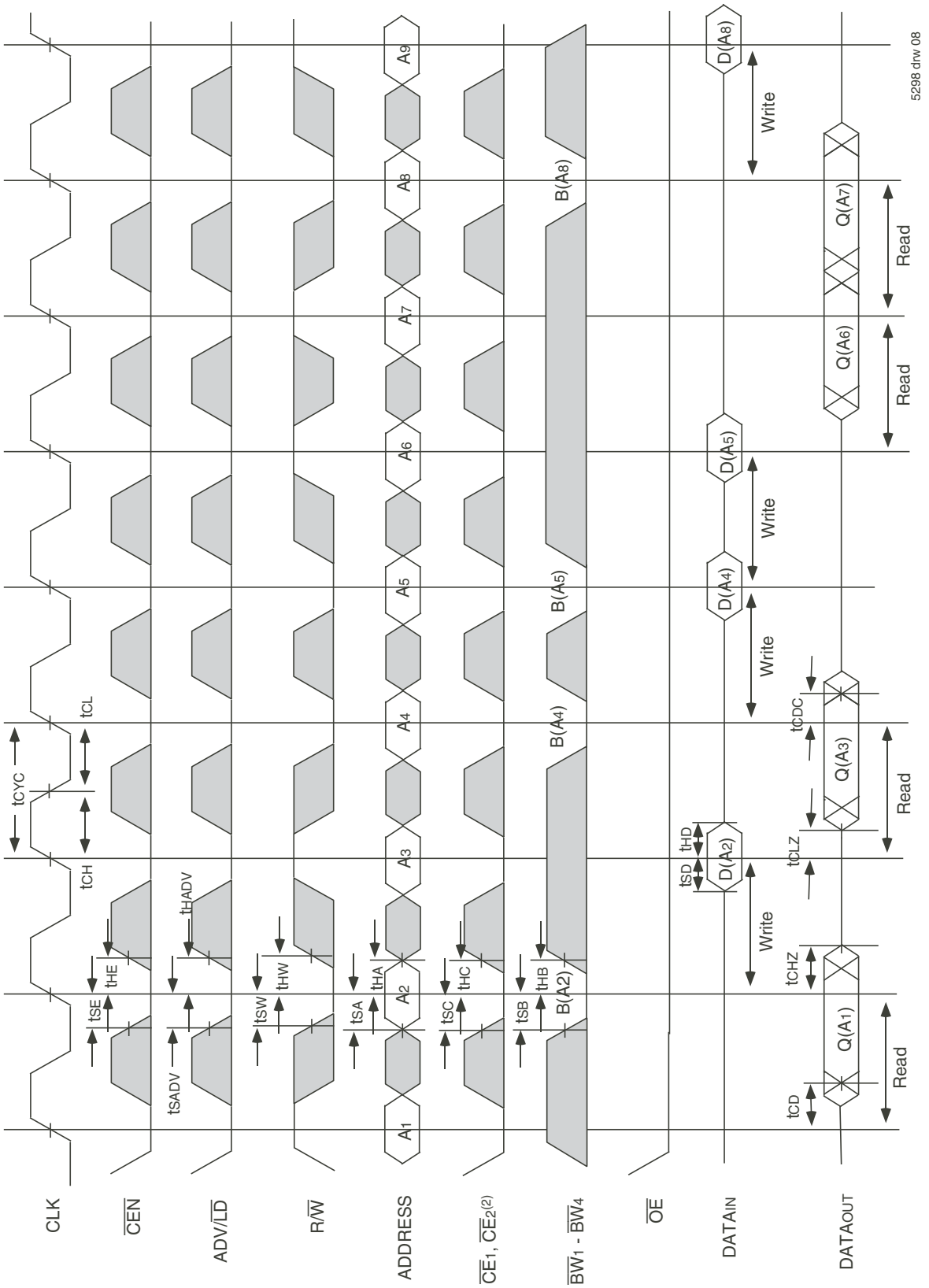
Timing Waveform of Write Cycles(1,2,3,4,5)



NOTES:

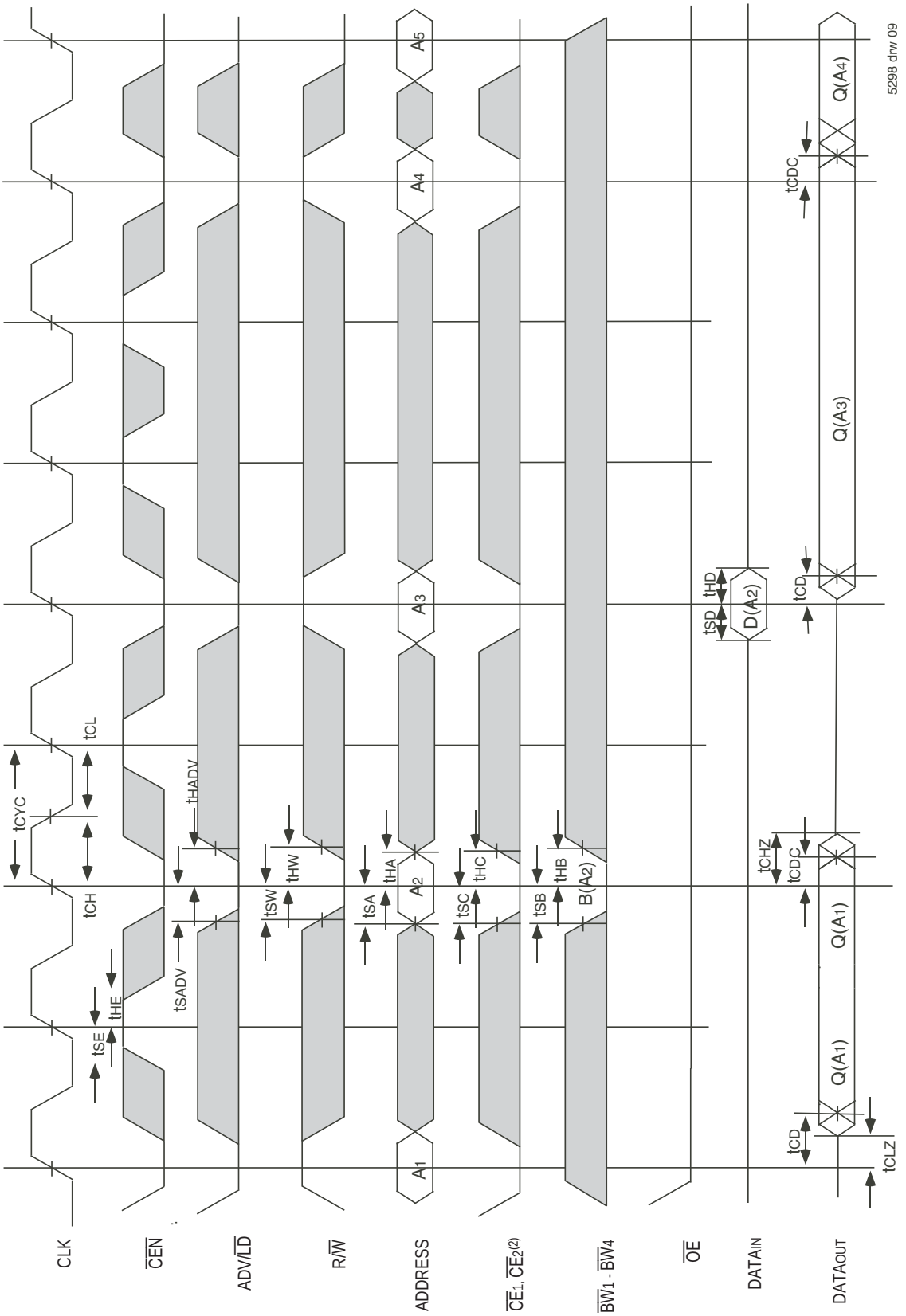
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. R/W is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles(1,2,3)



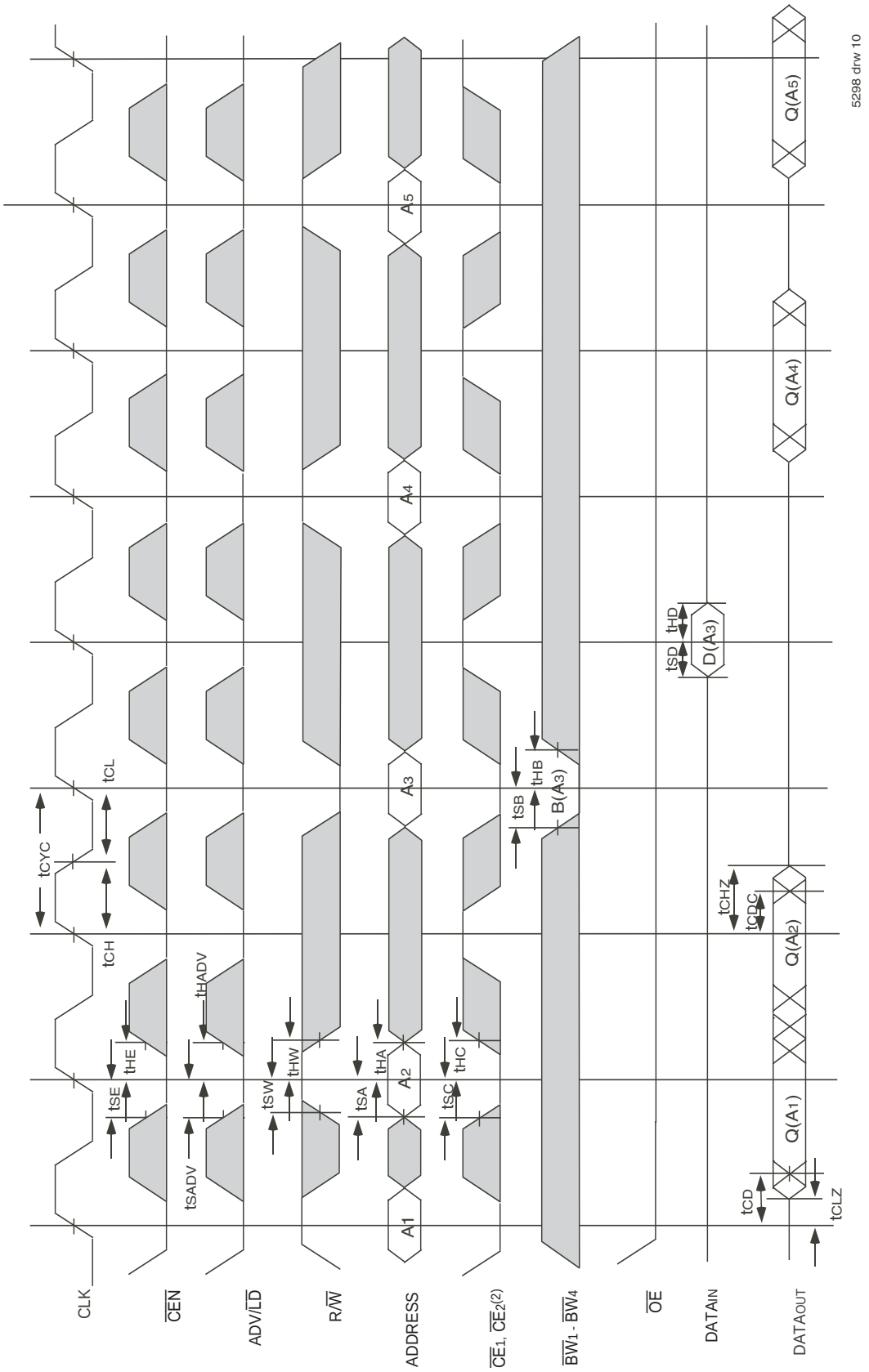
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{CEN}$ Operation(1,2,3,4)



NOTES:
1. Q (A_1) represents the first output from the external address A_1. D (A_2) represents the input data to the SRAM corresponding to address A_2.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. $\overline{CEN}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $R\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

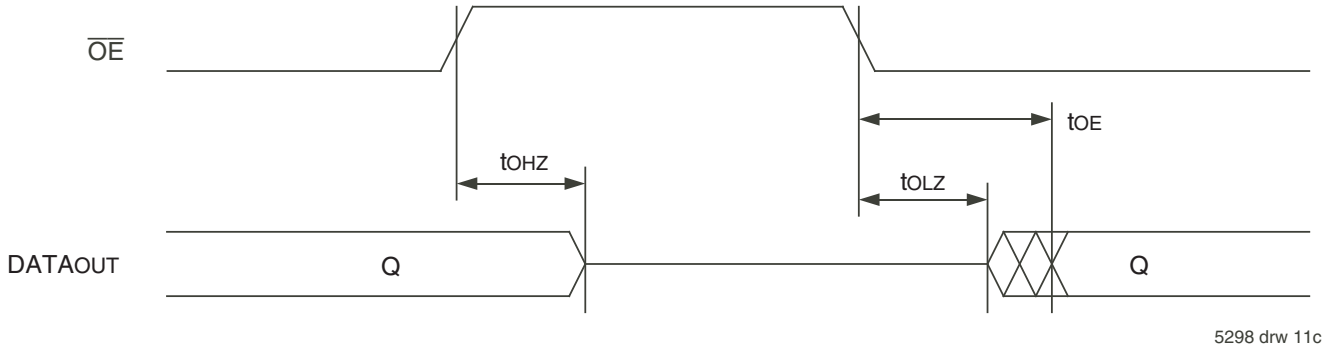
Timing Waveform of $\overline{CS}$ Operation(1,2,3,4)



NOTES:

1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. When either one of the Chip enables ($\overline{CE}_1$, CE2, $\overline{CE}_2$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{OE}$ Operation(1)



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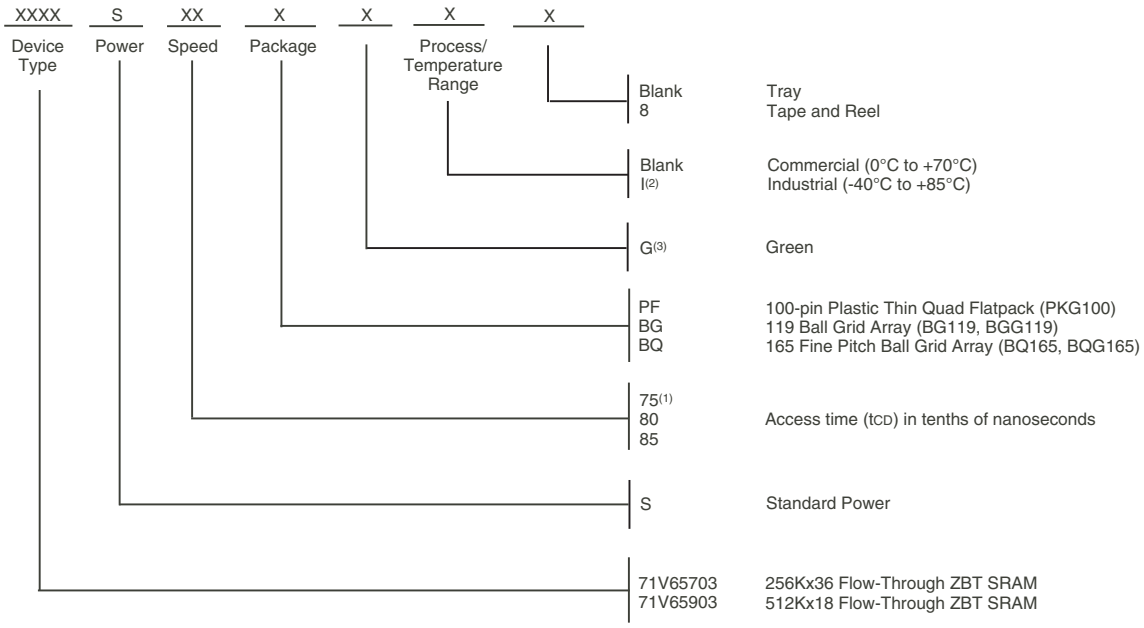
NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



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NOTES:
1. 71V65703 only.
2. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
3. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
7.5	71V65703S75BG	BG119	PBGA	C
	71V65703S75BG8	BG119	PBGA	C
	71V65703S75BGG	BGG119	PBGA	C
	71V65703S75BGG8	BGG119	PBGA	C
	71V65703S75BQ	BQ165	CABGA	C
	71V65703S75BQ8	BQ165	CABGA	C
	71V65703S75BQG	BQG165	CABGA	C
	71V65703S75BQG8	BQG165	CABGA	C
	71V65703S75PFG	PKG100	TQFP	C
	71V65703S75PFG8	PKG100	TQFP	C
	71V65703S75PFGI	PKG100	TQFP	I
	71V65703S75PFGI8	PKG100	TQFP	I
8.0	71V65703S80BG	BG119	PBGA	C
	71V65703S80BG8	BG119	PBGA	C
	71V65703S80BGG	BGG119	PBGA	C
	71V65703S80BGG8	BGG119	PBGA	C
	71V65703S80BQ	BQ165	CABGA	C
	71V65703S80BQ8	BQ165	CABGA	C
	71V65703S80BQG	BQG165	CABGA	C
	71V65703S80BQG8	BQG165	CABGA	C
	71V65703S80BQGI	BQG165	CABGA	I
	71V65703S80BQGI8	BQG165	CABGA	I
	71V65703S80BQI	BQ165	CABGA	I
	71V65703S80BQI8	BQ165	CABGA	I
	71V65703S80PFG	PKG100	TQFP	C
	71V65703S80PFG8	PKG100	TQFP	C
	71V65703S80PFGI	PKG100	TQFP	I
	71V65703S80PFGI8	PKG100	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
8.5	71V65703S85BG	BG119	PBGA	C
	71V65703S85BG8	BG119	PBGA	C
	71V65703S85BGG	BGG119	PBGA	C
	71V65703S85BGG8	BGG119	PBGA	C
	71V65703S85BGGI	BGG119	PBGA	I
	71V65703S85BGGI8	BGG119	PBGA	I
	71V65703S85BGI	BG119	PBGA	I
	71V65703S85BGI8	BG119	PBGA	I
	71V65703S85BQ	BQ165	CABGA	C
	71V65703S85BQ8	BQ165	CABGA	C
	71V65703S85BQG	BQG165	CABGA	C
	71V65703S85BQG8	BQG165	CABGA	C
	71V65703S85BQGI	BQG165	CABGA	I
	71V65703S85BQGI8	BQG165	CABGA	I
	71V65703S85BQI	BQ165	CABGA	I
	71V65703S85BQI8	BQ165	CABGA	I
	71V65703S85PFG	PKG100	TQFP	C
	71V65703S85PFG8	PKG100	TQFP	C
	71V65703S85PFGI	PKG100	TQFP	I
	71V65703S85PFGI8	PKG100	TQFP	I

Orderable Part Information (con't)

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
8.0	71V65903S80BG	BG119	PBGA	C
	71V65903S80BG8	BG119	PBGA	C
	71V65903S80BGI	BG119	PBGA	I
	71V65903S80BGI8	BG119	PBGA	I
	71V65903S80BQ	BQ165	CABGA	C
	71V65903S80BQ8	BQ165	CABGA	C
	71V65903S80BQG	BQG165	CABGA	C
	71V65903S80BQG8	BQG165	CABGA	C
	71V65903S80PFG	PKG100	TQFP	C
	71V65903S80PFG8	PKG100	TQFP	C
	71V65903S80PFGI	PKG100	TQFP	I
	71V65903S80PFGI8	PKG100	TQFP	I
8.5	71V65903S85BG	BG119	PBGA	C
	71V65903S85BG8	BG119	PBGA	C
	71V65903S85BGG	BGG119	PBGA	C
	71V65903S85BGG8	BGG119	PBGA	C
	71V65903S85BGGI	BGG119	PBGA	I
	71V65903S85BQ	BQ165	CABGA	C
	71V65903S85BQ8	BQ165	CABGA	C
	71V65903S85BQG	BQG165	CABGA	C
	71V65903S85BQG8	BQG165	CABGA	C
	71V65903S85PFG	PKG100	TQFP	C
	71V65903S85PFG8	PKG100	TQFP	C
	71V65903S85PFGI	PKG100	TQFP	I
	71V65903S85PFGI8	PKG100	TQFP	I

Datasheet Document History

12/31/99		Created new part number and datasheet from 71V657/59 to 71v65703/5903
04/20/00	Pg.5,6	Add JTAG reset pins to TQFP pin configuration; removed footnote
		Add clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 7	Add note to BGA pin configuration; corrected typo within pinout
	Pg. 21	InsertTQFP Package Diagram Outline
05/23/00		Add new package offering: 13mm x 15mm, 165 fine pitch ball grid array
	Pg. 23	Correction on 119 Ball Grid Array Package diagram Outline
07/28/00	Pg. 5-8	Remove JTAG pins from TQFP, BG119 and BQ165 pinouts, refer to IDT71V656xx and IDT71V658xx device errata sheet
	Pg. 7,8	Correct error in pinout, B2 on BG119 and B1 on BQ165 pinout
	Pg. 23	Update BG119 package diagram dimensions
11/04/00	Pg. 8	Add reference note to pin N5 on the BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$
	Pg. 15	Add Izz to DC Electrical Characteristics
12/04/02	Pg. 1-25	Changed datasheet from Preliminary to final release
	Pg. 5,6,15,16,25	Added I temp to datasheet
12/18/02	Pg. 1,2,5,6,7,8	Removed JTAG functionality for current die revision
	Pg. 7	Corrected pin configuration on the x36, 119 BGA. Switched pins I/O0 and I/OP1.
10/16/14	Pg. 1	Added green availability to Features and corrected a typo
	Pg. 15	DC Electrical Chars Table corrected typos for I_{DD} in the Industrial Temp range for the 8.0ns & 8.5ns speed grades
	Pg. 22	Removed IDT from and added green and T&R indicators to the ordering information Added (1) footnote annotation to 75 access speed in the ordering information table Added the corresponding footnote to the text "71V65703 only".
10/18/21	Pg. 1-27	Source file updated to reflect previous Corporate Marketing rebranding
	Pg. 5-8	Updated footnotes for DNU = Do not use pins
	Pg. 5-8 & 23	Updated package codes
	Pg. 7	Pin Configuration 512K x18, BG119, BGG119 - I/O numbering corrected
	Pg. 1 & 23	Updated Industrial temp range and green availability
	Pg. 24 & 25	Added Orderable Part Information tables