# **74ABT245**

# Octal transceiver with direction pin; 3-state

Rev. 5 — 9 July 2021

**Product data sheet** 

## 1. General description

The 74ABT245 is an 8-bit transceiver with 3-state outputs. The device features an output enable  $(\overline{OE})$  and send/receive (DIR) for direction control. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

### 2. Features and benefits

- Octal bidirectional bus interface
- 3-State buffers
- Supply voltage range from 4.5 to 5.5 V
- · BiCMOS high speed and output drive
- · Direct interface with TTL levels
- Output capability: +64 mA/–32 mA
- · Power-up 3-State
- Live insertion/extraction permitted
- · Inputs are disabled during 3-state mode
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

# 3. Ordering information

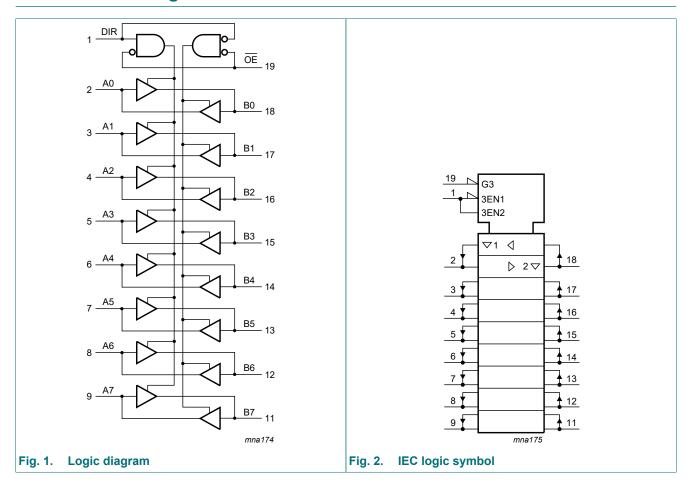
### **Table 1. Ordering information**

Type number	Package										
	Temperature range	Name	Description	Version							
74ABT245D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1							
74ABT245PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1							



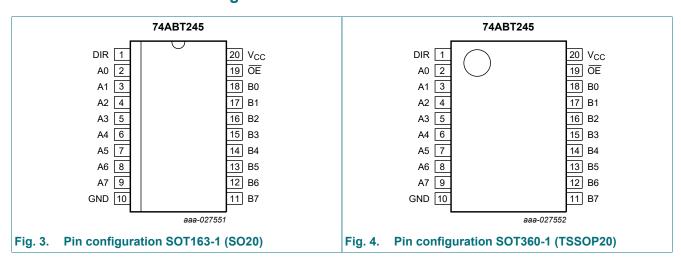
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## 4. Functional diagram



# 5. Pinning information

### 5.1. Pinning



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## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
ŌE	19	output enable input (active LOW)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Input		Input/output					
DE DIR		An	Bn				
L	L	output An = Bn	input				
L	Н	input	output Bn = An				
Н	X	Z	Z				

## 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
Tj	junction temperature	[2]	-	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

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# 8. Recommended operating conditions

### **Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH-level output current		-	-	-32	mA
I <sub>OL</sub>	LOW-level output current		-	-	64	mA
Δt/ΔV	input transition rise and fall rate		0	-	5	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

### 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T,	<sub>amb</sub> = 25	°C		<sub>nb</sub> = to +85 °C	Unit
			Min	Тур	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	-1.2	-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level	$V_{CC}$ = 4.5 V; $V_I$ = $V_{IL}$ or $V_{IH}$						
	output voltage	I <sub>OH</sub> = -3 mA	2.5	2.9	-	2.5	-	V
		I <sub>OH</sub> = -32 mA	2.0	2.4	-	2.0	-	V
		$V_{CC}$ = 5.0 V; $V_I$ = $V_{IL}$ or $V_{IH}$						
		I <sub>OH</sub> = -3 mA	3.0	3.4	-	3.0	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH};$ $I_{OL} = 64 \text{ mA}$	-	0.42	0.55	-	0.55	V
l <sub>l</sub>	input leakage current	Control pins; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	μΑ
		Data pins; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±5	±100	-	±100	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{O} \text{ or } V_{I} \le 4.5 \text{ V}$	-	±5.0	±100	-	±100	μΑ
I <sub>O(pu/pd)</sub>	power-up/ power-down output current	$V_{CC}$ = 2.0 V; $V_O$ = 0.5 V; [1] $V_I$ = GND or $V_{CC}$ ; $\overline{OE}$ = don't care	-	±5.0	±50	-	±50	μА
l <sub>OZ</sub>	OFF-state	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>						
	output current	output HIGH-state at V <sub>O</sub> = 2.7 V	-	5.0	50	-	50	μA
		output LOW-state at V <sub>O</sub> = 0.5 V	-	-5.0	-50	-	-50	μΑ
I <sub>CEX</sub>	output high leakage current	$V_{CC} = 5.5 \text{ V}; V_{O} = 5.5 \text{ V}; V_{I} = \text{GND or } V_{CC}$	-	5.0	50	-	50	μA
Io	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$ [2]	-40	-100	-180	-40	-180	mA

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Symbol	Parameter	Parameter Conditions		Ta	<sub>imb</sub> = 25	°C		<sub>nb</sub> = o +85 °C	Unit
				Min	Тур	Max	Min	Max	
I <sub>CC</sub>	supply current	$V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$							
		outputs HIGH-state		-	50	250	-	250	μA
		outputs LOW-state		-	24	30	-	30	mA
		outputs disabled		-	50	250	-	250	μΑ
$\Delta I_{CC}$	additional supply	per input pin; V <sub>CC</sub> = 5.5 V							
	current	outputs enabled; one input at 3.4 V and other inputs at V <sub>CC</sub> or GND	[3]	-	0.5	1.5	-	1.5	mA
		outputs disabled; one data input at 3.4 V and other inputs at V <sub>CC</sub> or GND	[3]	-	50	250	-	250	μА
		outputs disabled; one enable input at 3.4 V and other inputs at V <sub>CC</sub> or GND	[3]	-	0.5	1.5	-	1.5	mA
Cı	input capacitance	DIR; $\overline{OE}$ ; $V_I = 0 \text{ V or } V_{CC}$		-	4	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	outputs disabled; $V_0 = 0 \text{ V or } V_{CC}$		-	7	-	-	-	pF

<sup>[1]</sup> This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms. From  $V_{CC}$  = 2.1 V to  $V_{CC}$  = 5 V ± 10 % a transition time of up to 100  $\mu$ s is permitted.

# 10. Dynamic characteristics

### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

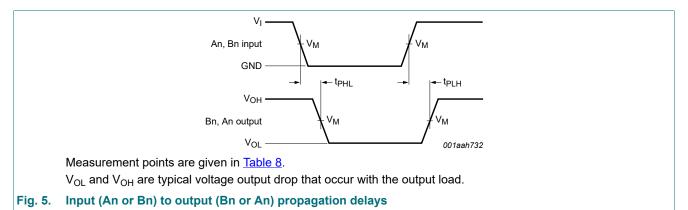
Symbol	Parameter	Conditions	T <sub>amb</sub> =	25 °C; V <sub>CC</sub>	; = 5.0 V	$T_{amb} = -40$ $V_{CC} = 5.0$	Unit	
			Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	An to Bn or Bn to An; see Fig. 5	1.0	2.2	4.1	1.0	4.6	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	An to Bn or Bn to An; see Fig. 5	1.0	2.9	4.2	1.0	4.6	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	OE to An or Bn; see Fig. 6	1.3	3.0	4.8	1.3	5.3	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	OE to An or Bn; see Fig. 6	2.3	4.0	5.8	2.3	6.3	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	OE to An or Bn; see Fig. 6	1.0	4.7	6.2	1.0	7.2	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	OE to An or Bn; see Fig. 6	1.0	4.1	5.8	1.0	6.3	ns

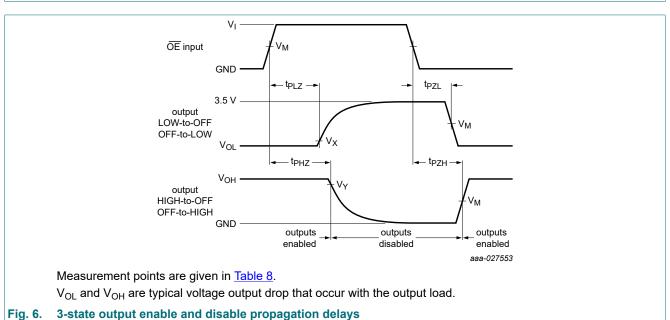
<sup>[2]</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>[3]</sup> This is the increase in supply current for each input at 3.4 V.

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#### 10.1. Waveforms and test circuit

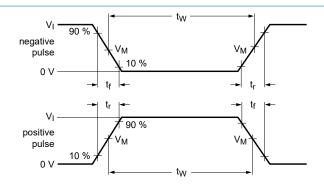


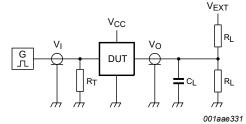


**Table 8. Measurement points** 

Input	Output								
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>						
1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V						

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Test data is given in Table 9.

Definitions test circuit:

 $R_L$  = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $V_{EXT}$  = Test voltage for switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

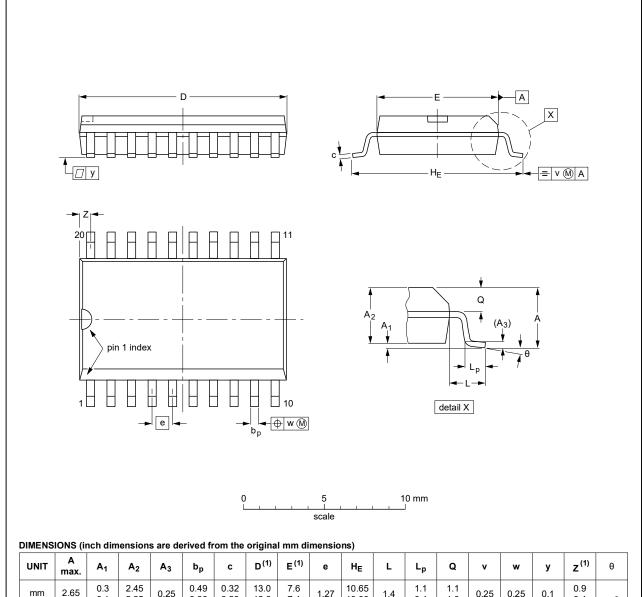
Input				Load		V <sub>EXT</sub>			
V <sub>I</sub> f <sub>i</sub> t <sub>W</sub>		t <sub>W</sub> t <sub>r</sub> , t <sub>f</sub>		CL	L R <sub>L</sub>		t <sub>PHZ</sub> , t <sub>PZH</sub> t <sub>PLZ</sub> , t <sub>PZL</sub>		
3.0 V	≤ 1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	7 V	open	

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# 11. Package outline

#### SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

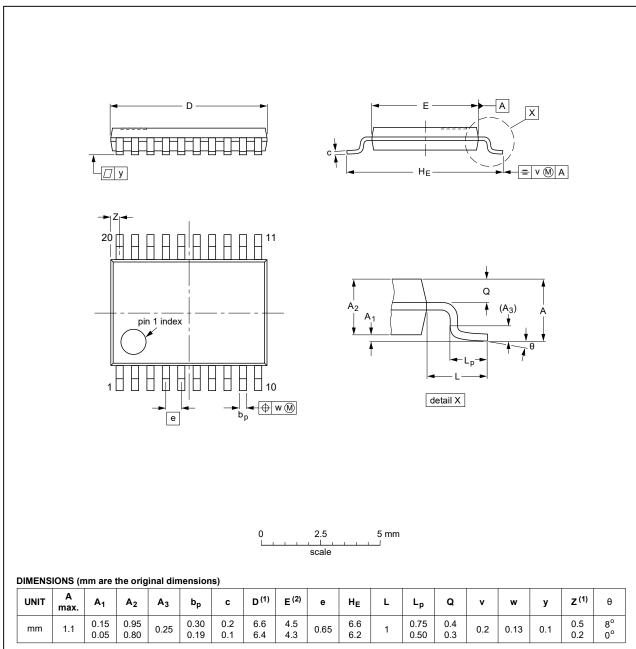
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013			<del>99-12-27</del> 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

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#### TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT360-1		MO-153				<del>99-12-27</del> 03-02-19

Fig. 9. Package outline SOT360-1 (TSSOP20)

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## 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ABT245 v.5	20210709	Product data sheet	-	74ABT245 v.4		
Modifications:	<ul> <li>Section 1 and Section 2 updated.</li> <li>Type number 74ABT245DB (SOT339-1 / SSOP20) removed.</li> </ul>					
74ABT245 v.4	20171006	Product data sheet	-	74ABT245 v.3		
Modifications:	e identity guidelines of propriate.					
74ABT245 v.3	20030206	Product data sheet	ECN 853-1447 29305	74ABT245 v.2		
Modifications:	Delete all references to N package. DIP20 package option discontinued.					
74ABT245 v.2	19980116	Product specification	ECN 853-1447 18867	74ABT245 v.1		
74ABT245 v.1	19960910	Product specification	-	-		

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#### Data sheet status

Document status [1][2]	Product status [3]	Definition		
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.		
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.		
Product [short] data sheet	Production	This document contains the product specification.		

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