

# 74AHC3G04-Q100; 74AHCT3G04-Q100

## Inverter

Rev. 3 — 4 August 2021

Product data sheet

## 1. General description

The 74AHC3G04-Q100; 74AHCT3G04-Q100 is a triple inverter. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- Symmetrical output impedance
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC3G04DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74AHC3G04DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AHCT3G04DC-Q100				

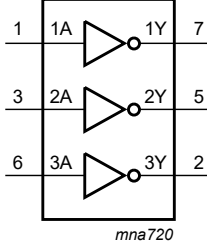
## 4. Marking

Table 2. Marking codes

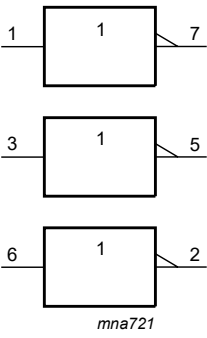
Type number	Marking code[1]
74AHC3G04DP-Q100	A04
74AHC3G04DC-Q100	A04
74AHCT3G04DC-Q100	C04

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

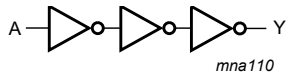
## 5. Functional diagram



**Fig. 1. Logic symbol**



**Fig. 2. IEC logic symbol**

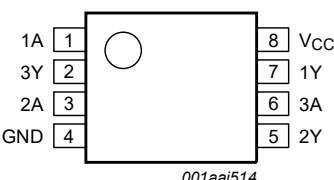


**Fig. 3. Logic diagram (one gate)**

## 6. Pinning information

### 6.1. Pinning

**74AHC3G04**  
**74AHCT3G04**



*001aaj514*

**Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)**

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level*

Input nA	Output nY
L	H
H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	$\pm 20$	mA
$I_O$	output current	$-0.5$ V $< V_O < V_{CC} + 0.5$ V	-	$\pm 25$	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96  $^{\circ}$ C.  
For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99  $^{\circ}$ C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74AHC3G04-Q100			74AHCT3G04-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V $\pm 0.3$ V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V $\pm 0.5$ V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit						
			Min	Typ	Max	Min	Max	Min	Max							
<b>74AHC3G04-Q100</b>																
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V						
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V						
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V						
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V						
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V						
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>														
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V						
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V						
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V						
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V						
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>														
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V						
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V						
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V						
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V						
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA						
		I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	µA				
				C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF		
						<b>74AHCT3G04-Q100</b>										
						V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V														
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V						
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V						
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V														
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V						
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V						

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = 3.4 V; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

GND = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC3G04-Q100</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 5 [1]								
		V <sub>CC</sub> = 3.0 V to 3.6 V [2]								
		C <sub>L</sub> = 15 pF	-	4.3	7.1	1.0	8.5	1.0	11.0	ns
		C <sub>L</sub> = 50 pF	-	6.1	10.6	1.0	12.0	1.0	14.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [3]								
		C <sub>L</sub> = 50 pF	-	4.5	7.5	1.0	8.5	1.0	9.5	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	9	-	-	-	-	-	pF
<b>74AHCT3G04-Q100</b>										
t <sub>pd</sub>	propagation delay	nA to nY; See Fig. 5; [1] [3]								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.4	6.7	1.0	7.5	1.0	8.5	ns
		C <sub>L</sub> = 50 pF	-	4.9	7.7	1.0	8.5	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	10	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2] Typical values are measured at V<sub>CC</sub> = 3.3 V.

[3] Typical values are measured at V<sub>CC</sub> = 5.0 V.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

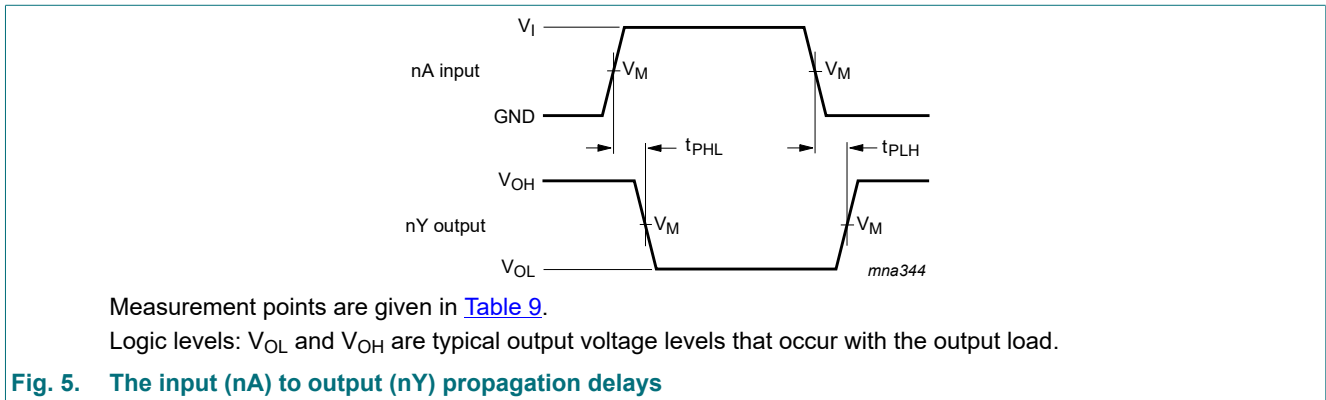
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

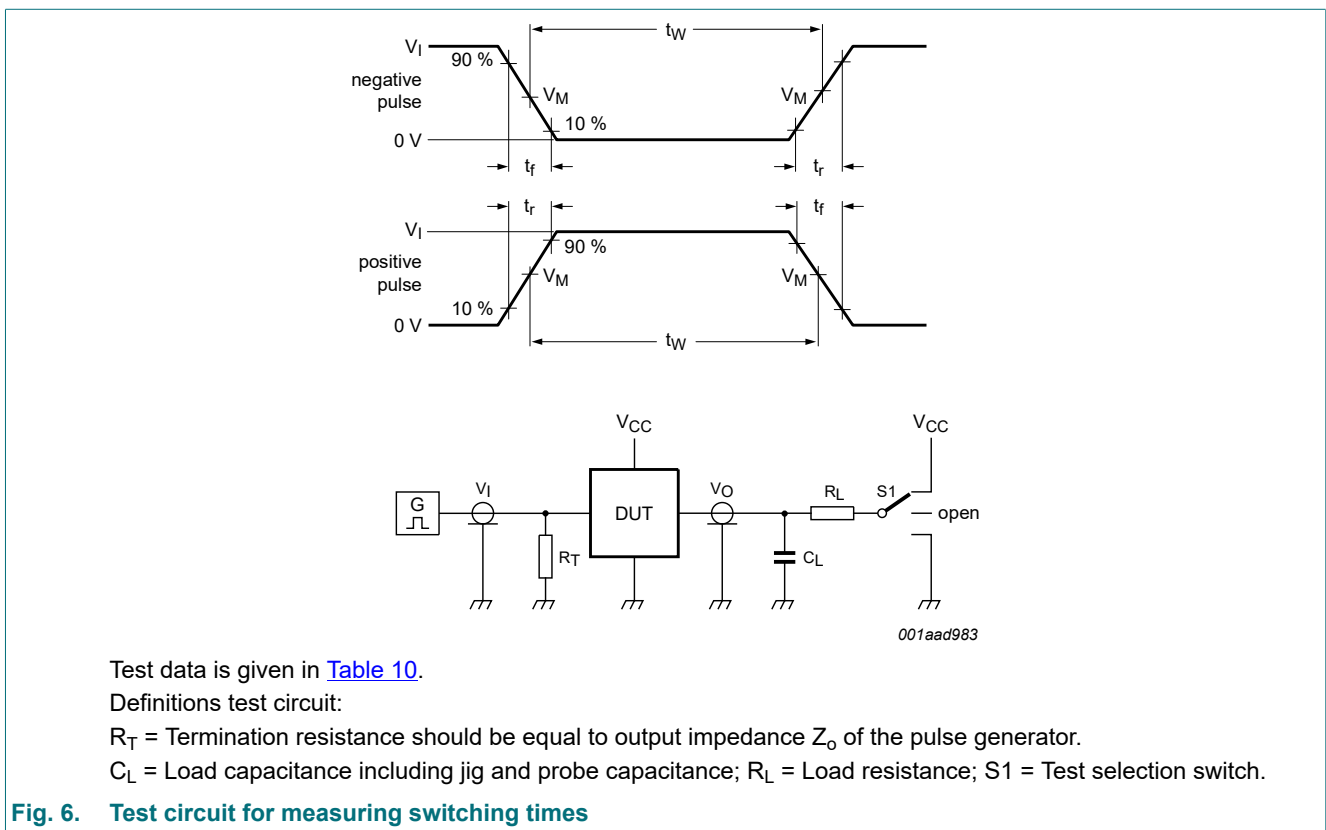
∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

### 11.1. Waveforms and test circuit



**Table 9. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC3G04-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74AHCT3G04-Q100	1.5 V	$0.5V_{CC}$



**Table 10. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC3G04-Q100	$V_{CC}$	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT3G04-Q100	3 V	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

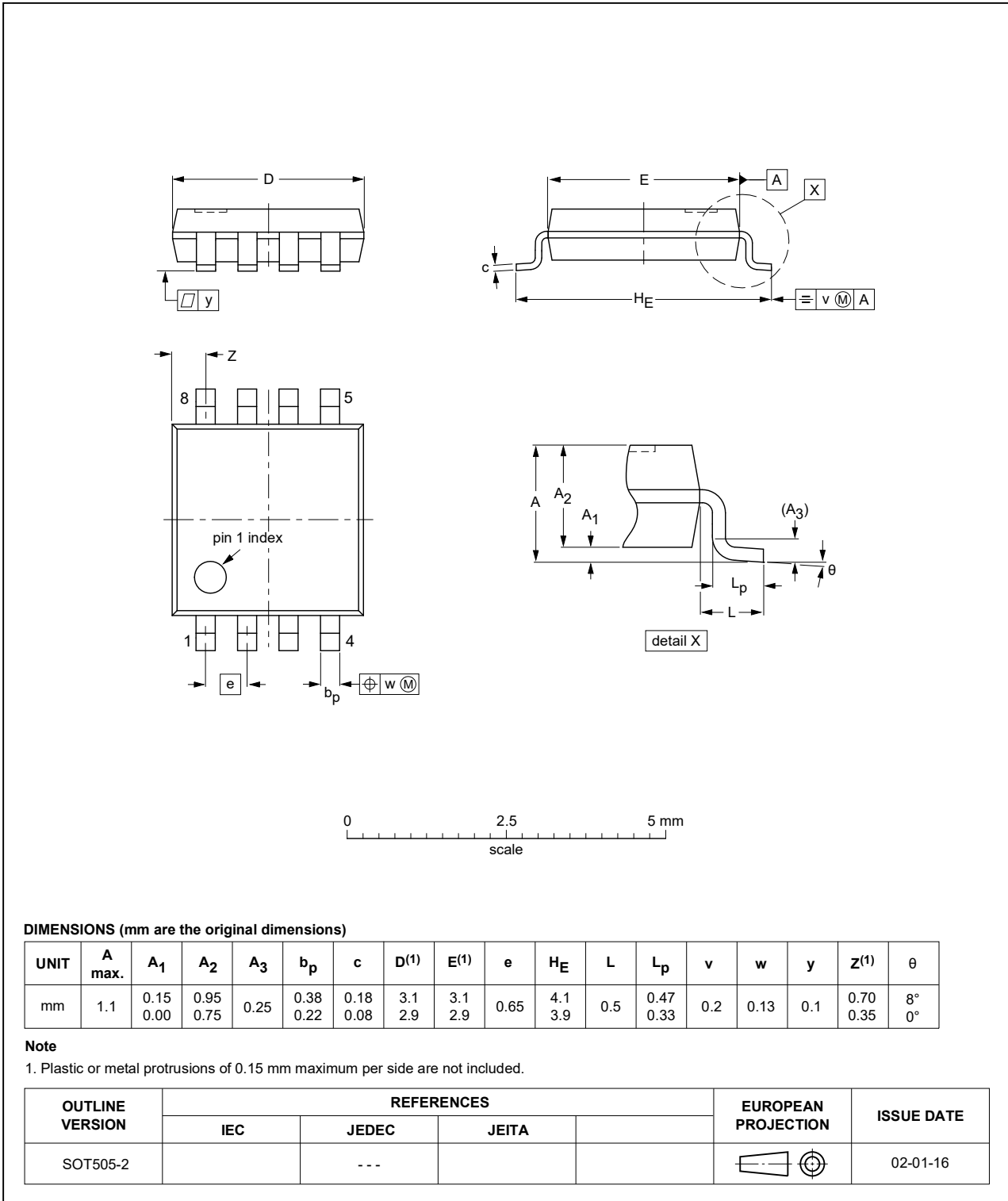


Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

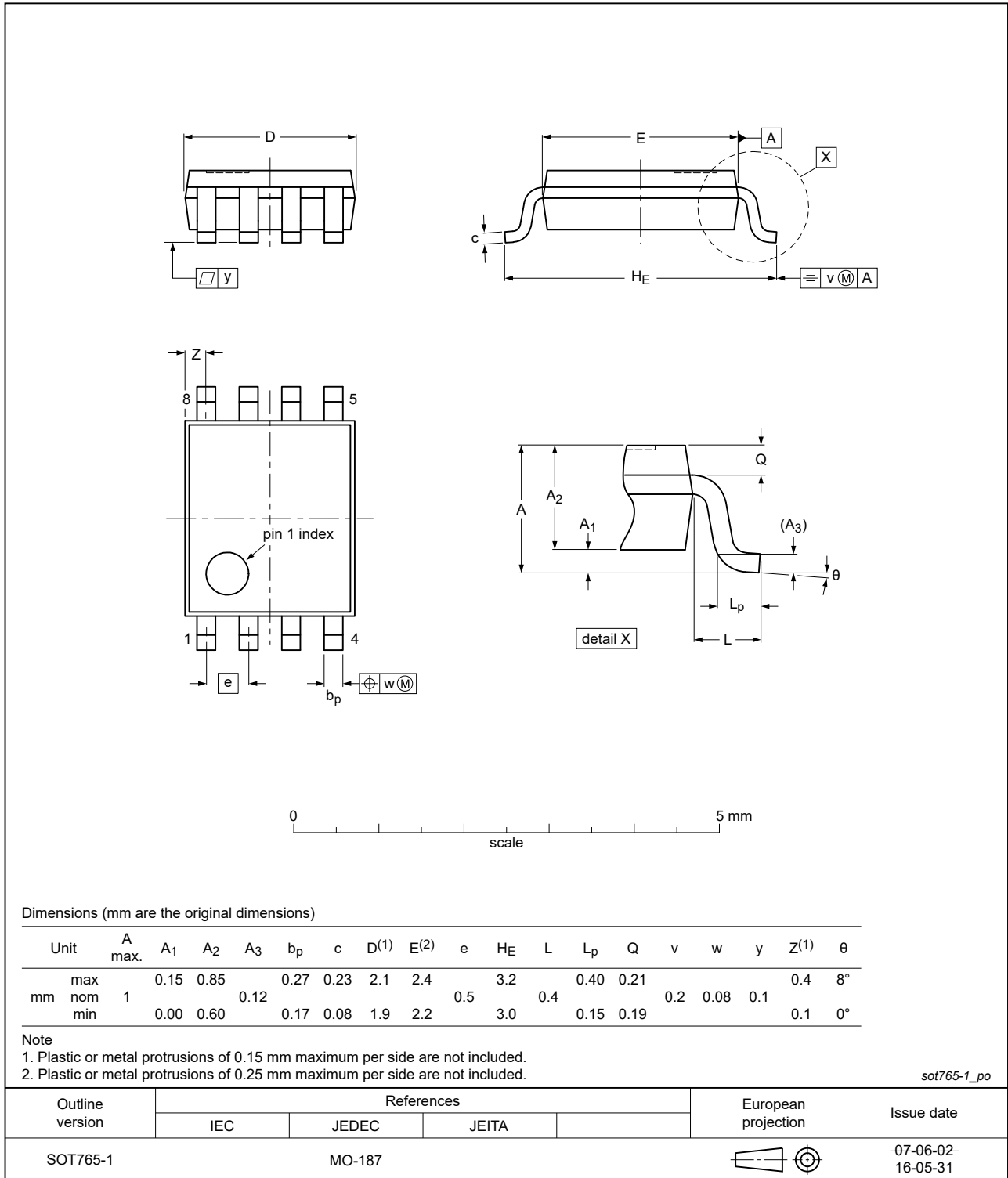


Fig. 8. Package outline SOT765-1 (VSSOP8)



## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT3G04_Q100 v.3	20210804	Product data sheet	-	74AHC_AHCT3G04_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHC_AHCT3G04_Q100 v.2	20181119	Product data sheet	-	74AHC_AHCT3G04_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type number 74AHCT3G04DP-Q100 removed.</li> </ul>			
74AHC_AHCT3G04_Q100 v.1	20130326	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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