

# 74AHCU04

Hex unbuffered inverter

Rev. 5 — 18 May 2020

Product data sheet

## 1. General description

The 74AHCU04 is high-speed Si-gate CMOS devices and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHCU04 is a general purpose hex unbuffered inverter. Each of the six inverters is a single stage.

## 2. Features and benefits

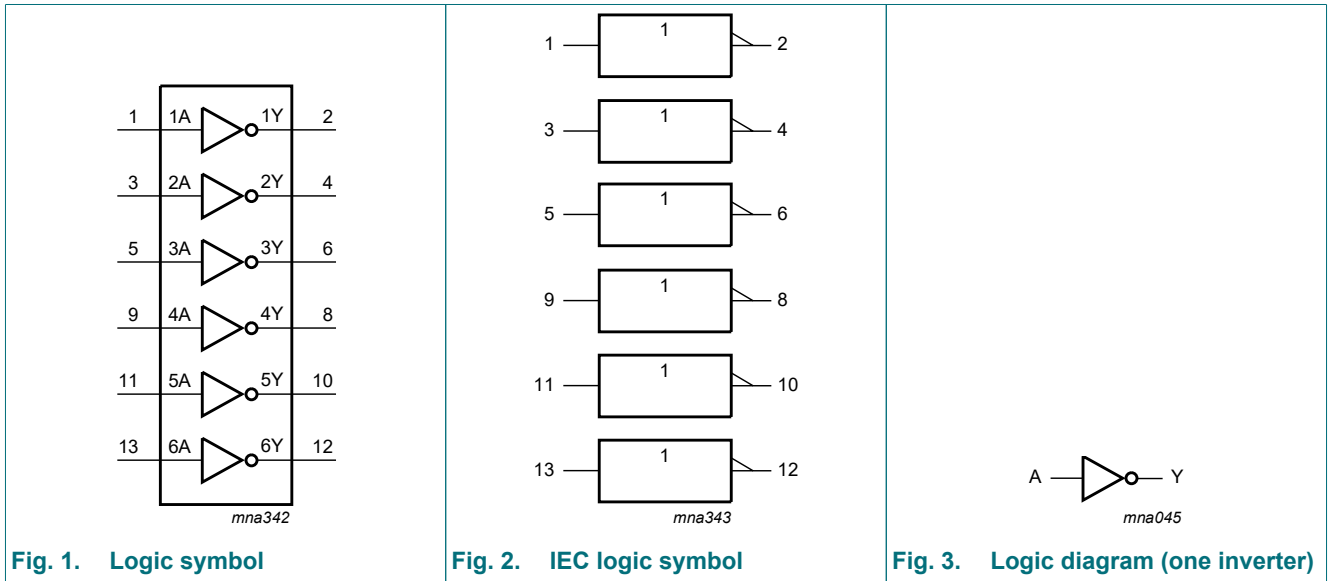
- Low power dissipation
- Balanced propagation delays
- Inputs accepts voltages higher than  $V_{CC}$
- ESD protection:
  - HBM JESD22-A114F: exceeds 2000 V
  - MM JESD22-A115-A: exceeds 200 V
  - CDM JESD22-C101C: exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

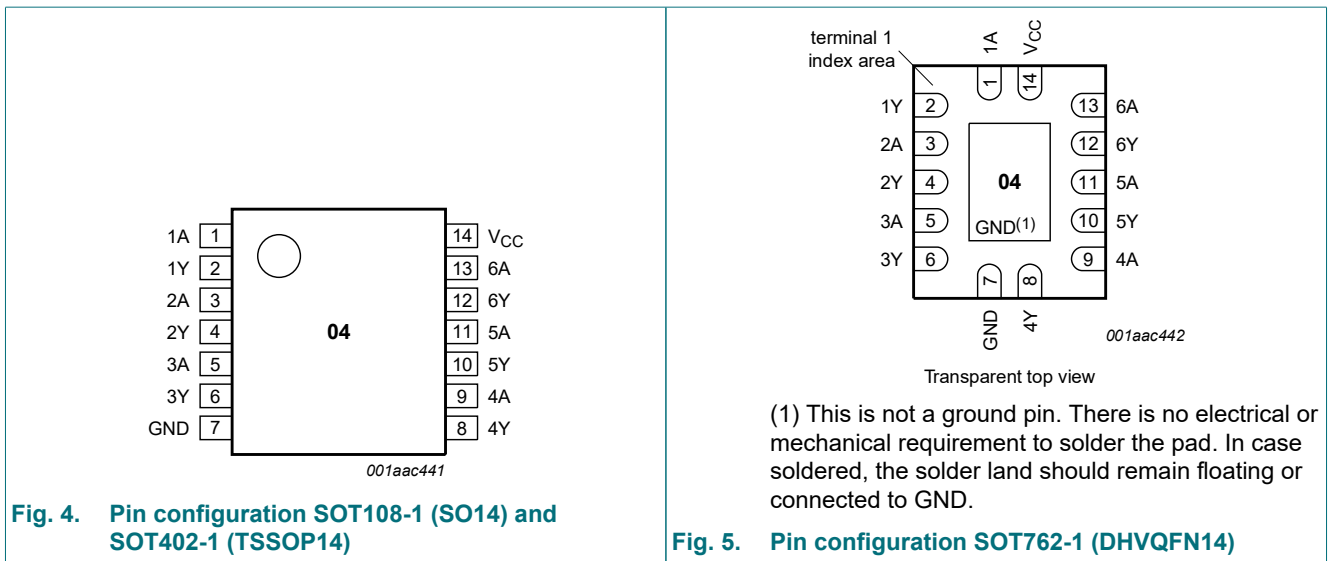
Type number	Package			
	Temperature range	Name	Description	Version
74AHCU04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCU04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCU04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



#### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level*

Input	Output
nA	nY
L	H
H	L

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-20	-	mA
$V_I$	input voltage	[1]	-0.5	+7.0	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	$\pm 20$	mA
$I_O$	output current	$-0.5$ V $< V_O < V_{CC} + 0.5$ V	-	$\pm 25$	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V $\pm 0.3$ V	-	-	100	ns/V
		$V_{CC} = 5.0$ V $\pm 0.5$ V	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V <sub>CC</sub> = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V <sub>CC</sub> = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V <sub>CC</sub> = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V <sub>CC</sub> = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.8	2.0	-	1.8	-	1.8	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.7	3.0	-	2.7	-	2.7	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.0	4.5	-	4.0	-	4.0	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.7	-	V		
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.2	-	0.2	-	0.2	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.3	-	0.3	-	0.3	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.5	-	0.5	-	0.5	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V		
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	μA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF

## 10. Dynamic characteristics

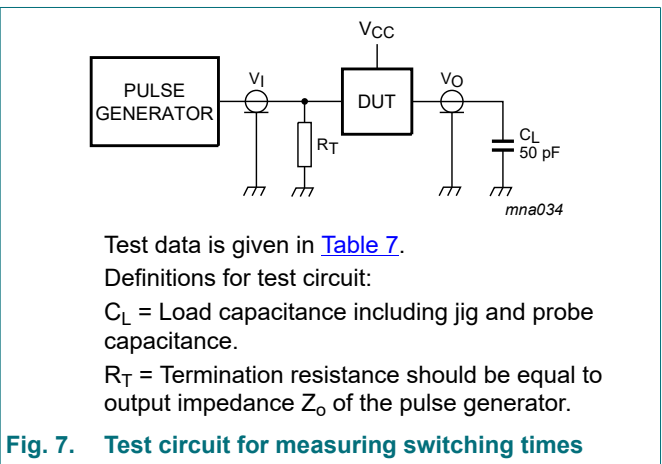
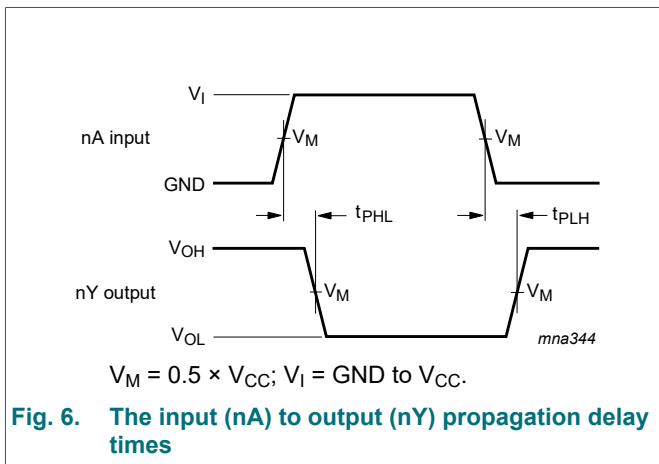
**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; For test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	nA to nY; see Fig. 6 [1]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; $C_L = 15\text{ pF}$ [2]	-	3.0	7.1	1.0	8.5	1.0	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; $C_L = 50\text{ pF}$ [2]	-	3.4	10.6	1.0	12.0	1.0	13.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; $C_L = 15\text{ pF}$ [3]	-	2.4	5.5	1.0	6.5	1.0	7.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ; $C_L = 50\text{ pF}$ [3]	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f_i = 1\text{ MHz}$ ; $V_i = GND\text{ to }V_{CC}$ [4]	-	9.1	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [2] Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .
- [3] Typical values are measured at  $V_{CC} = 5.0\text{ V}$ .
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 10.1. Waveforms



### 11. Typical transfer characteristics

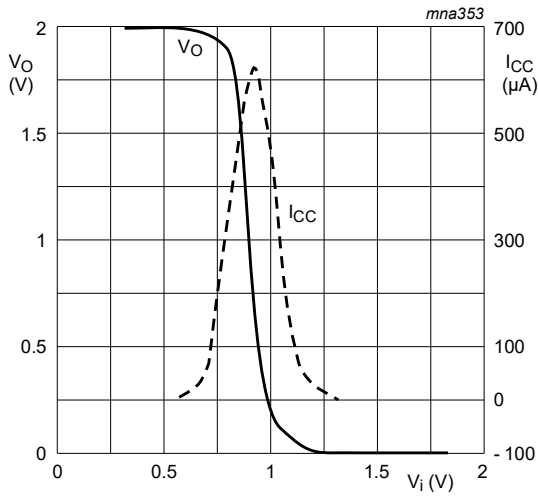


Fig. 8.  $V_{CC} = 2.0\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ °C}.$

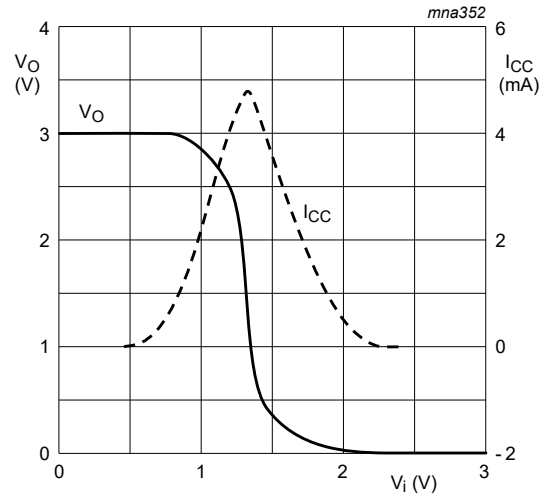


Fig. 9.  $V_{CC} = 3.0\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ °C}.$

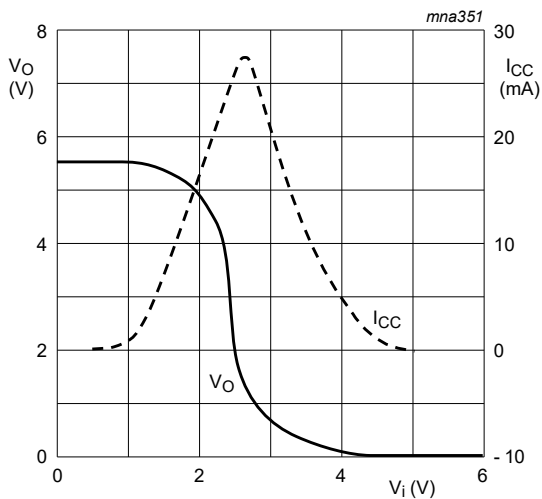
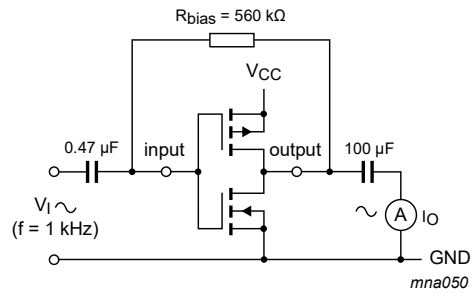


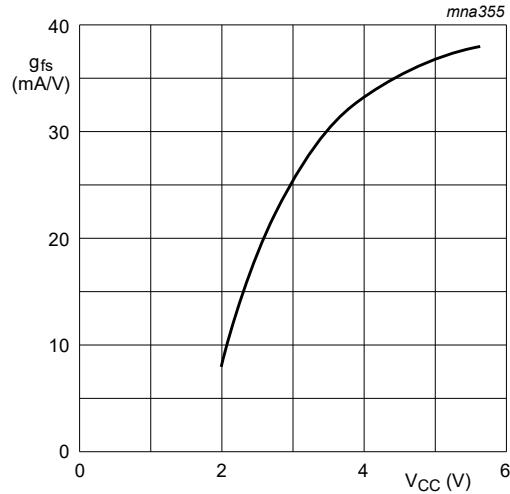
Fig. 10.  $V_{CC} = 5.5\text{ V}; I_O = 0\text{ A}$   
 $T_{amb} = 25\text{ °C}.$



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

$f_i = 1\text{ kHz}$  at  $V_O$  is constant

Fig. 11. Test set-up for measuring forward transconductance



T<sub>amb</sub> = 25 °C.

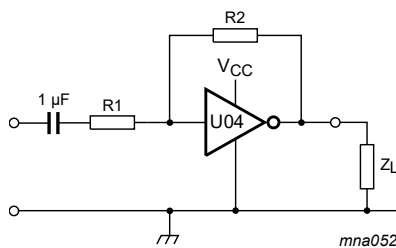
Fig. 12. Typical forward transconductance as a function of the supply voltage

## 12. Application information

Some applications are:

- Linear amplifier (see Fig. 13)
- In crystal oscillator design (see Fig. 14)

**Remark:** All values given are typical unless otherwise specified.



Maximum V<sub>o(p-p)</sub> = V<sub>CC</sub> - 1.5 V centered at 0.5 × V<sub>CC</sub>.

$$G_v = - \frac{G_{ol}}{1 + \frac{R1}{R2} (1 + G_{ol})}$$

G<sub>ol</sub> = open loop gain

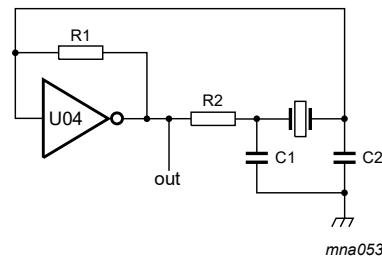
G<sub>v</sub> = voltage gain

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z<sub>L</sub> > 10 kΩ; G<sub>ol</sub> = 12 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig. 13. Used as a linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical)

R2 optimum value depends on the frequency and required stability against changes in V<sub>CC</sub> or average minimum I<sub>CC</sub> (I<sub>CC</sub> is typically 5 mA at V<sub>CC</sub> = 5 V and f<sub>i</sub> = 10 MHz).

Fig. 14. Crystal oscillator configuration

**Table 8. External components for resonator (f < 1 MHz)**

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	20 pF
16 kHz to 24.9 kHz	22 M $\Omega$	220 k $\Omega$	56 pF	10 pF
25 kHz to 54.9 kHz	22 M $\Omega$	100 k $\Omega$	56 pF	10 pF
55 kHz to 129.9 kHz	22 M $\Omega$	100 k $\Omega$	47 pF	5 pF
130 kHz to 199.9 kHz	22 M $\Omega$	47 k $\Omega$	47 pF	5 pF
200 kHz to 349.9 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF
350 kHz to 600 kHz	10 M $\Omega$	47 k $\Omega$	47 pF	5 pF

**Table 9. Optimum value for R2**

Frequency	R2	Optimum for
3 kHz	2.0 k $\Omega$	minimum required I <sub>CC</sub>
	8.0 k $\Omega$	minimum influence due to change in V <sub>CC</sub>
6 kHz	1.0 k $\Omega$	minimum required I <sub>CC</sub>
	4.7 k $\Omega$	minimum influence by V <sub>CC</sub>
10 kHz	0.5 k $\Omega$	minimum required I <sub>CC</sub>
	2.0 k $\Omega$	minimum influence by V <sub>CC</sub>
14 kHz	0.5 k $\Omega$	minimum required I <sub>CC</sub>
	1.0 k $\Omega$	minimum influence by V <sub>CC</sub>
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF



13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 17. Package outline SOT762-1 (DHVQFN14)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCU04 v.5	20200518	Product data sheet	-	74AHCU04 v.4
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>			
74AHCU04 v.4	20151207	Product data sheet	-	74AHCU04 v.3
Modifications:	<ul style="list-style-type: none"> <li>Descriptive title updated. Added "unbuffered" (errata).</li> </ul>			
74AHCU04 v.3	20071114	Product data sheet	-	74AHCU04 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3</a>: DHVQFN14 package added.</li> <li><a href="#">Section 7</a>: derating values added for DHVQFN14 package.</li> <li><a href="#">Section 13</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74AHCU04 v.2	19990927	Product specification	-	74AHCU04 v.1
74AHCU04 v.1	19990226	Product specification	-	-

## 16. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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