# **74ALVC245**

# Octal bus transceiver; 3-state

Rev. 3 — 30 April 2021

**Product data sheet** 

## 1. General description

The 74ALVC245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The 74ALVC245 features an output enable input ( $\overline{OE}$ ) for easy cascading and send/receive input (DIR) for direction control.  $\overline{OE}$  controls the outputs, so that the buses are effectively isolated.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.5 V)
  - JESD8B (2.7 V to 3.6 V)
- 3.6 V tolerant inputs/outputs
- CMOS low-power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

# 3. Ordering information

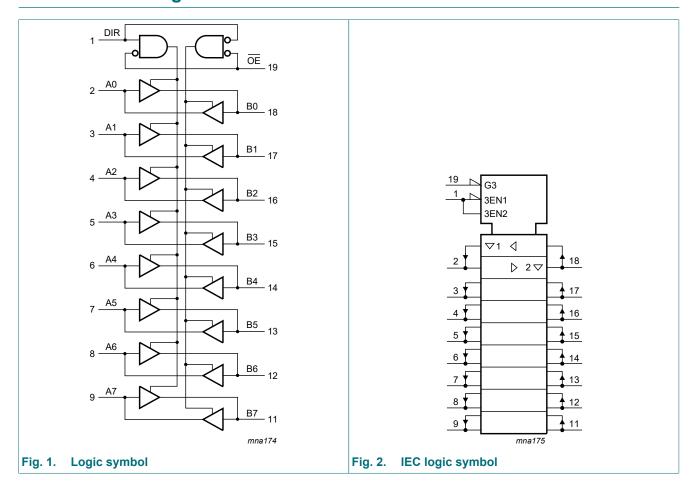
#### **Table 1. Ordering information**

Type number	Package									
	Temperature range	Name	Description	Version						
74ALVC245D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1						
74ALVC245PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1						
74ALVC245BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1						



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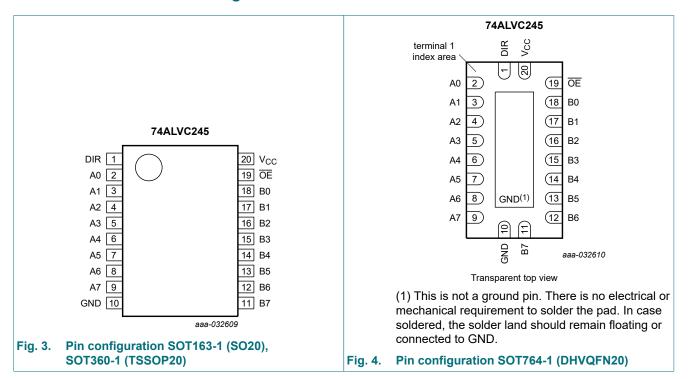
# 4. Functional diagram



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## 5. Pinning information

## 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Table 211 III decemption										
Symbol	Pin	Description								
DIR	1	direction control								
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output								
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output								
GND	10	ground (0 V)								
ŌE	19	output enable input (active LOW)								
V <sub>CC</sub>	20	supply voltage								

## 6. Functional description

### Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ Z = high-impedance \ OFF-state.$ 

Input		Input/output			
DE DIR		An	Bn		
L	L	A = B	input		
L	Н	input	B = A		
Н	X	Z	Z		

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# 7. Limiting values

## **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$	-	±50	mA
Vo	output voltage	output HIGH or LOW state [2]	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state [2]	-0.5	+4.6	V
		power-down mode; V <sub>CC</sub> = 0 V	-0.5	+4.6	V
I <sub>O</sub>	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb}$ = -40 °C to +85 °C	-	500	mW

<sup>[1]</sup> The minimum input voltage ratings may be exceeded if the input current ratings are observed.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	3.6	V
		power-down mode; V <sub>CC</sub> = 0 V	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	10	ns/V

<sup>[2]</sup> The output voltage ratings may be exceeded if the output current ratings are observed.

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## 9. Static characteristics

**Table 6. Static characteristics** 

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	Unit
			Min	Typ [1]	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.65 V	1.25	-	-	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_{O}$ = -100 $\mu$ A; $V_{CC}$ = 1.65 V to 3.6 V	-	-	0.2	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.65 V	-	-	0.3	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	-	-	0.4	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	-	-	0.4	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; [2] $V_{CC} = 3.6 \text{ V}$	-	±0.1	±10.0	μΑ
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 3.6 \text{ V}$	-	±0.1	±5.0	μA
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O}$ = 0 V to 3.6 V; $V_{CC}$ = 0 V	-	±0.1	±10.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 3.6$ V	-	0.2	10	μΑ
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	750	μΑ
Cı	input capacitance		-	3.5	-	pF
C <sub>I/O</sub>	input/output capacitance		-	3.5	-	pF

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All typical values are measured at  $V_{CC}$  = 3.3 V and  $T_{amb}$  = 25 °C. For transceivers, the parameter  $I_{OZ}$  includes the input leakage current.

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# 10. Dynamic characteristics

### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions		40 °C to +85 °	С	Unit
			Min	Typ [1]	Max	
t <sub>pd</sub>	propagation delay	An to Bn; Bn to An; see Fig. 5 [2]				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	2.7	6.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.1	3.5	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.0	3.6	ns
	V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	3.4	ns	
t <sub>en</sub>	enable time	OE to An; OE to Bn; see Fig. 6 [2]				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.0	8.6	ns
	V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.0	6.0	ns	
		V <sub>CC</sub> = 2.7 V	1.0	2.6	6.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	5.5	ns
t <sub>dis</sub>	disable time	OE to An; OE to Bn; see Fig. 6 [2]				
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.4	8.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.3	4.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.3	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.2	5.5	ns
C <sub>PD</sub>	power dissipation	per buffer; $V_I = GND$ to $V_{CC}$ ; $V_{CC} = 3.3 V$ [3]				
	capacitance	outputs enabled	-	25	-	pF
		outputs disabled	-	1	-	pF

<sup>[1]</sup> All typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 1.8 V, 2.5 V, 2.7 V and 3.3 V.

 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ . [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

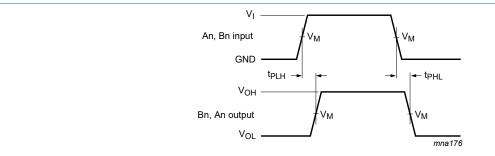
 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of the outputs.

<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

 $t_{\text{en}}$  is the same as  $t_{\text{PZL}}$  and  $t_{\text{PZH}}.$ 

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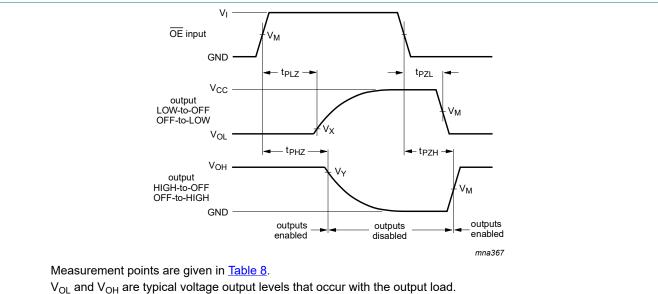
## 10.1. Waveforms and test circuit



Measurement points are given in Table 8.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Propagation delay input (An, Bn) to output (Bn, An) Fig. 5.

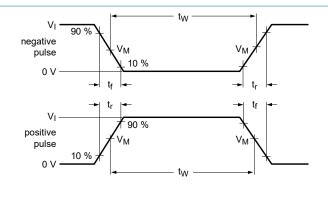


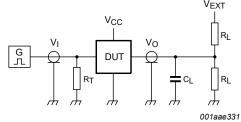
**Enable and disable times** Fig. 6.

**Table 8. Measurement points** 

Supply voltage	Input		Output				
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>		
1.65 V to 1.95 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V		
2.3 V to 2.7 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V		
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V		
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V		

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Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator

 $C_L$  = Load capacitance including jig and probe capacitance

R<sub>L</sub> = Load resistor

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

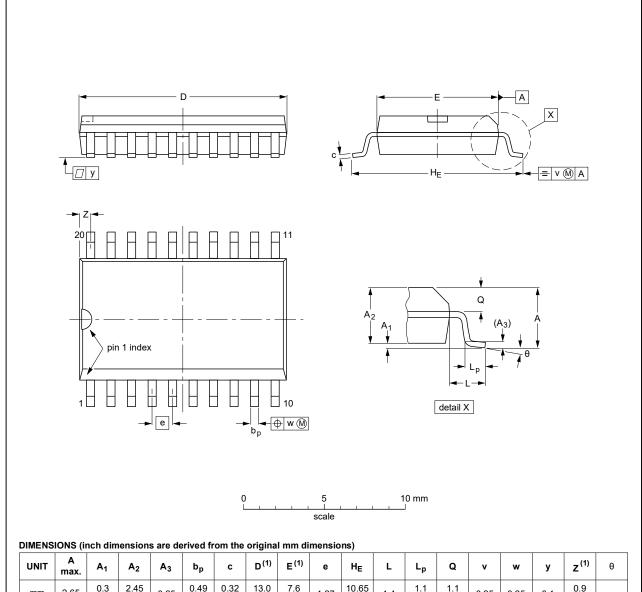
Supply voltage Input		Load		V <sub>EXT</sub>	V <sub>EXT</sub>			
V <sub>CC</sub>	VI	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND	
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND	

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# 11. Package outline

## SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

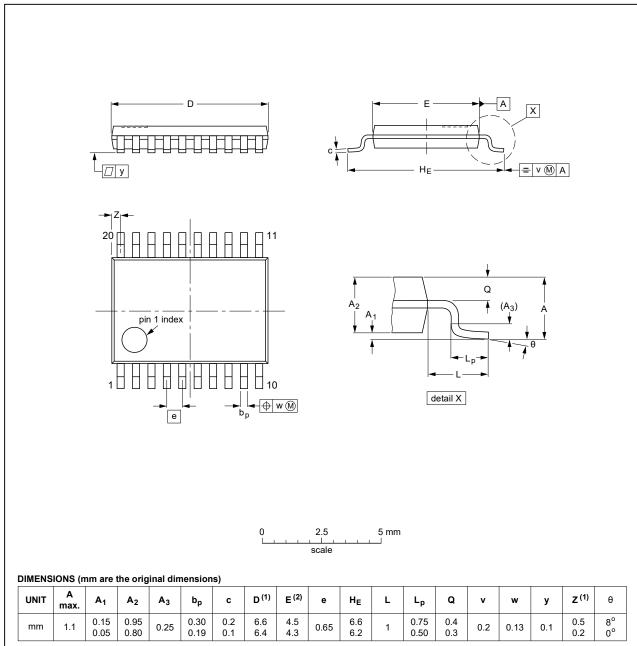
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013			<del>99-12-27</del> 03-02-19	

Fig. 8. Package outline SOT163-1 (SO20)

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## TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION ISSUE	ISSUE DATE
SOT360-1		MO-153				<del>99-12-27</del> 03-02-19

Fig. 9. Package outline SOT360-1 (TSSOP20)

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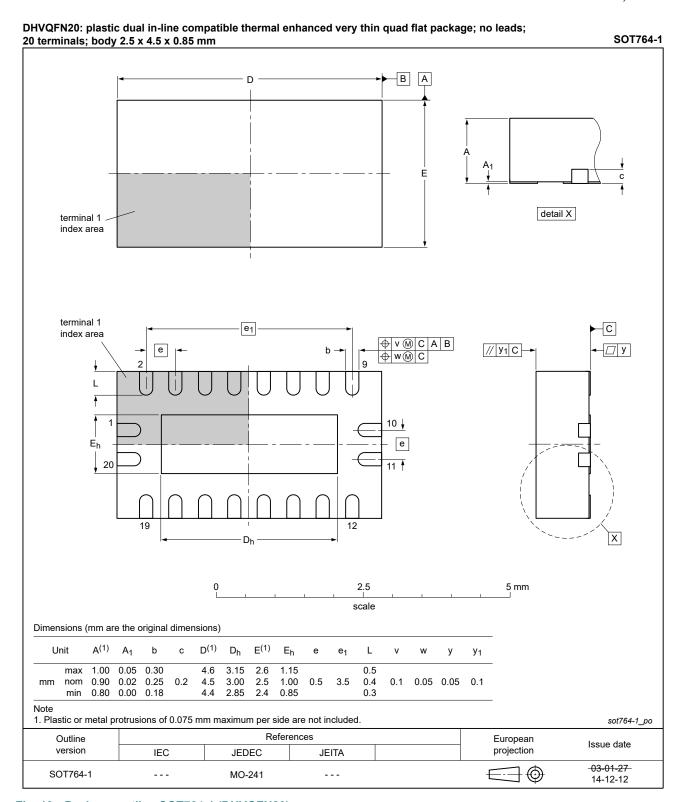


Fig. 10. Package outline SOT764-1 (DHVQFN20)

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## 12. Abbreviations

## **Table 10. Abbreviations**

Acronym	Description	
CMOS	Complementary Metal Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
НВМ	Human Body Model	
MM	Machine Model	
TTL	Transistor-Transistor Logic	

# 13. Revision history

## Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ALVC245 v.3	20210430	Product data sheet	-	74ALVC245 v.2		
Modifications:	guidelines c • Legal texts • Section 2: F • Section 7: C	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 2: Reference to JESD36 removed.</li> <li>Section 7: Derating values for P<sub>tot</sub> total power dissipation removed (errata).</li> <li>Package outline drawing SOT764-1 (DHVQFN20) updated.</li> </ul>				
74ALVC245 v.2	20080107	Product data sheet		74ALVC245 v.1		
Modifications:	guidelines c • Legal texts • Section 3: E • Section 7: d	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 3: DHVQFN20 package added.</li> <li>Section 7: derating values added for DHVQFN20 package.</li> <li>Section 11: outline drawing added for DHVQFN20 package.</li> </ul>				
74ALVC245 v.1	20030710	Product specification	-	-		

#### Octal bus transceiver; 3-state

## 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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