Low-power D-type flip-flop with set and reset; positive-edge trigger

Rev. 2 — 10 April 2017

Product data sheet

1 General description

The 74AUP1G74-Q100 provides a low-power, low-voltage single positive-edge triggered D-type flip-flop with individual data (D), clock (CP), set (\overline{SD}) and reset (\overline{RD}) inputs and complementary Q and \overline{Q} outputs. The \overline{SD} and \overline{RD} are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2 Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 Class 3A. Exceeds 5000 V
 - HBM JESD22-A114F Class 3A. Exceeds 5 000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Low static power consumption; $I_{CC} = 0.9 \ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- IOFF circuitry provides partial power-down mode operation

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3 Ordering information

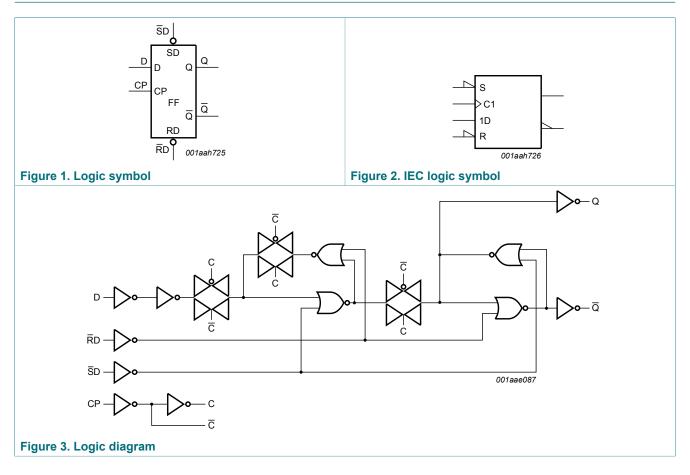
Table 1. Ordering information									
Type number	Package								
	Temperature range	Name	Description	Version					
74AUP1G74DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1					

4 Marking

Table 2. Marking codes	
Type number	Marking code ^[1]
74AUP1G74DC-Q100	p74

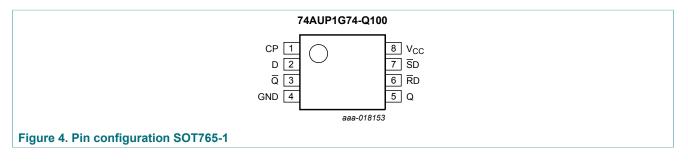
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5 Functional diagram



6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
СР	1	clock input
D	2	data input
Q	3	complement output
GND	4	ground (0 V)
Q	5	true output
RD	6	asynchronous reset input (active LOW)
SD	7	asynchronous set input (active LOW)
V _{CC}	8	supply voltage

7 Functional description

Table 4. Function table for asynchronous operation ^[1]								
				Output				
<u>S</u> D	RD	СР	D	Q	Q			
L	Н	x	х	Н	L			
Н	L	x	Х	L	Н			
L	L	х	Х	Н	Н			

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care.

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Table 5. Function table for synchronous operation ^[1]

Input				Output	
<u>S</u> D	RD	СР	D	Q _{n+1}	Q _{n+1}
Н	Н	1	L	L	Н
Н	Н	1	Н	Н	L

[1] H = HIGH voltage level;

L = LOW voltage level;

↑ = LOW-to-HIGH CP transition;

 Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Limiting values 8

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Мах	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage		[1]	-0.5	+4.6	V
Vo	output voltage	Active mode and Power-down mode	[1]	-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
Ι _{ΟΚ}	output clamping current	V _O < 0 V		-50	-	mA
I _O	output current	$V_{O} = 0 V$ to V_{CC}		-	±20	mA
I _{CC}	supply current			-	+50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250	mW

The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed. For VSSOP8 packages: above 110 $^{\circ}$ C the value of P_{tot} derates linearly with 8.0 mW/K. [1]

[2]

Recommended operating conditions 9

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6 V V _{CC} V 3.6 V +125 °C	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	-	200	ns/V

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10 Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
T _{amb} = 25	°C					
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	$c_{CC} = 0.9 \ V to 1.95 \ V$ $0.65 \times V_{CC}$ $ V$ $c_{CC} = 2.3 \ V to 2.7 \ V$ 1.6 $ V$ $c_{CC} = 3.0 \ V to 3.6 \ V$ 2.0 $ V$ $c_{CC} = 0.8 \ V$ $ 0.30 \times V_{CC} \ V$ V $c_{CC} = 0.9 \ V to 1.95 \ V$ $ 0.35 \times V_{CC} \ V$ V $c_{CC} = 2.3 \ V to 2.7 \ V$ $ 0.35 \times V_{CC} \ V$ V $c_{CC} = 3.0 \ V to 3.6 \ V$ $ 0.9 \ V$ V $c_{CC} = 3.0 \ V to 3.6 \ V$ $ 0.9 \ V$ V $c_{CC} = 3.0 \ V to 3.6 \ V$ $ 0.9 \ V$ V $c_{CC} = 3.0 \ V to 3.6 \ V$ $ 0.9 \ V$ V $c_{CC} = 1.1 \ W$ $0.75 \times V_{CC}$ $ V$ $l_0 = -1.1 \ mA; \ V_{CC} = 1.65 \ V$ 1.32 $ V$ $l_0 = -1.9 \ mA; \ V_{CC} = 2.3 \ V$ 2.05 $ V$ $l_0 = -2.3 \ mA; \ V_{CC} = 2.3 \ V$ $1.9 \ V$ $l_0 = -2.7 \ mA; \ V_{CC} = 3.0 \ V$ $2.66 \ V$ $l_0 = -2.7 \ mA; \ V_{CC} = 3.0 \ V$ $2.66 \ V$ $l_0 = -2.0 \ \muA; \ V_{CC} = 0.8 \ V \ to 3.6 \ V$ $ 0.1 \ V$ $l_0 = -2.0 \ mA; \ V_{CC} = 1.1 \ V$ $ 0.1 \ V$ $l_0 = 1.1 \ mA; \ V_{CC} = 1.1 \ V$ $ 0.1 \ V$ $l_0 = 1.1 \ mA; \ V_{CC} = 1.4 \ V$ $ 0.31 \ V$ <t< td=""></t<>				
		V _{CC} = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	$\begin{array}{c} - \\ - \\ 0.30 \times V_{CC} \\ 0.35 \times V_{CC} \\ 0.35 \times V_{CC} \\ 0.7 \\ 0.9 \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ - \\ $	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = -20 $\mu \text{A}; V_{\rm CC}$ = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	$0.75 \times V_{CC}$	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	2.05	-	-	V
		$I_{\rm O}$ = -3.1 mA; $V_{\rm CC}$ = 2.3 V	1.9	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.72	-	-	V
		$I_{\rm O}$ = -4.0 mA; $V_{\rm CC}$ = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = 20 $\mu \text{A}; V_{CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	- - - N - 0.30 × V _{CC} N - 0.35 × V _{CC} N - 0.7 N - 0.9 N - 0.9 N - - N - - N - - N - - N - - N - - N - - N - - N - - N - - N - - N - - N - - N - 0.1 N - 0.31 N - 0.31 N - 0.31 N - 0.31 N - 0.44 N - ±0.1 N - ±0.2 N	V	
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		$I_{\rm O}$ = 2.3 mA; $V_{\rm CC}$ = 2.3 V	-	-	0.31	V
		$I_{\rm O}$ = 3.1 mA; $V_{\rm CC}$ = 2.3 V	-	-	0.44	V
		$I_{\rm O}$ = 2.7 mA; $V_{\rm CC}$ = 3.0 V	-	-	0.31	V
		$I_{\rm O}$ = 4.0 mA; $V_{\rm CC}$ = 3.0 V	-	-	0.44	V
l	input leakage current	$V_{\rm I}$ = GND to 3.6 V; $V_{\rm CC}$ = 0 V to 3.6 V	-	-	±0.1	μA
OFF	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
∆I _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.2	μA
l _{cc}	supply current	V_1 = GND or V_{CC} ; I_0 = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA

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Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ [1] $V_{CC} = 3.3 \text{ V}; \text{ per pin}$	-	-	40	μA
CI	input capacitance	V_{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.6	-	pF
Co	output capacitance	$V_{O} = GND; V_{CC} = 0 V$	-	1.3	-	pF
$T_{amb} = -40$	0 °C to +85 °C		1		1	
VIH	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	$\begin{array}{c c c c c c } & - & - & 40 & \mu A \\ \hline - & 0.6 & - & \rho F \\ \hline - & 1.3 & - & \rho F \\ \hline - & 1.3 & - & \rho F \\ \hline - & 1.3 & - & \rho F \\ \hline - & 1.3 & - & 0.7 & V \\ \hline - & - & - & V \\ \hline - & - & - & V \\ \hline - & - & - & V \\ \hline - & - & 0.30 \times V_{CC} & V \\ \hline - & - & 0.35 \times V_{CC} & V \\ \hline - & - & 0.7 & V \\ \hline - & - & 0.9 & V \\ \hline - & - & 0.9 & V \\ \hline \end{array}$	V	
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = -20 µA; V_{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.7 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.67	-	-	V
		I_{O} = -4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I_{O} = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V_1 or V_0 = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μA
I _{CC}	supply current	V_1 = GND or V_{CC} ; I_0 = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	μA

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Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 V; I_{O} = 0 A;$ ^[1] $V_{CC} = 3.3 V; per pin$	-	-	50	μA
$T_{amb} = -40$	0 °C to +125 °C			1	1	
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		$I_{\rm O}$ = -20 $\mu \text{A}; V_{\rm CC}$ = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	$0.6 \times V_{CC}$	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		$I_{\rm O}$ = -2.3 mA; $V_{\rm CC}$ = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		$I_{\rm O}$ = -2.7 mA; $V_{\rm CC}$ = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
l	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	$V_{1} \text{ or } V_{O} = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.75	μA
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	1.4	μA
∆l _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}; \text{ per pin}$ [1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

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11 Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Ta	imb = 25 °	°C		-40 °C 35 °C	T _{amb} = to +1	-40 °C 25 °C	Unit
			Min	Typ ^[1]	Мах	Min	Мах	Min	Мах	
C _L = 5 pF		· · · · · · · · · · · · · · · · · · ·				1				_
t _{pd}	propagation	CP to Q, \overline{Q} ; see <u>Figure 5</u> . ^[2]								
	delay	V _{CC} = 0.8 V	-	25.4	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.9	6.7	14.0	2.6	14.2	2.6	14.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.4	4.5	7.6	2.3	8.3	2.3	8.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.5	5.7	1.7	6.5	1.7	6.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	2.6	3.8	1.4	4.4	1.4	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.2	3.1	1.2	3.4	1.2	3.7	ns
		\overline{SD} to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	19.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.7	5.6	11.0	2.5	11.4	2.5	11.5	ns
		V _{CC} = 1.4 V to 1.6 V	2.4	4.0	6.3	2.2	6.9	2.2	7.3	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	3.3	4.9	1.7	5.6	1.7	5.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.9	2.7	3.7	1.7	4.0	1.7	4.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.5	3.2	1.5	3.6	1.5	3.8	ns
		$\overline{R}D$ to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	19.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	5.5	11.0	2.5	11.3	2.5	11.5	I I <td< td=""></td<>
		V _{CC} = 1.4 V to 1.6 V	2.3	3.9	6.3	2.2	6.8	2.2	7.3	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.2	5.0	1.8	5.6	1.8	5.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.9	2.6	3.6	1.7	4.1	1.7	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.4	3.3	1.5	3.6	1.5	3.8	ns
f _{max}	maximum	CP; see <u>Figure 5</u> .								
	frequency	V _{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	8.6 ns 6.8 ns 4.7 ns 3.7 ns 1.1.7 ns 7.3 ns 5.9 ns 4.2 ns 3.8 ns 11.5 ns 3.8 ns 11.5 ns 7.3 ns 13.8 ns 11.5 ns 7.3 ns 11.5 ns 7.3 ns 3.8 ns 11.5 ns 3.8 ns 3.8 ns 3.8 ns 3.8 ns 3.8 ns 3.8 ns 1.1.5 ns 3.8 ns 3.8 ns 1.1.5 ns 1.1.5 ns 1.1.5 ns 1.1.5 ns 1.1.5 ns 1.1.5 ns <tr td=""> ns</tr>	MHz
		V _{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	MHz	
		V _{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C _L = 10 p	F									
pd	propagation	CP to Q, \overline{Q} ; see <u>Figure 5</u> . ^[2]								
	delay	V _{CC} = 0.8 V	-	28.9	-	-	-	-	-	ns

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Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Ta	mb = 25 °	°C	T _{amb} = to +8	-40 °C 35 °C		-40 °C 25 °C	Unit
			Min	Typ ^[1]	Max	Min	Мах	Min	Max	
		V _{CC} = 1.1 V to 1.3 V	3.1	7.5	15.8	2.9	16.1	2.9	16.1	ns
		V _{CC} = 1.4 V to 1.6 V	2.7	5.1	8.7	2.4	9.4	2.4	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.1	6.5	2.2	7.2	2.2	7.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	3.2	4.6	1.8	5.3	1.8	5.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.8	3.8	1.6	4.1	1.6	4.4	ns
		\overline{SD} to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	23.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.9	6.5	12.9	2.8	13.3	2.8	13.5	ns
		V _{CC} = 1.4 V to 1.6 V	2.7	4.6	7.5	2.3	7.9	2.3	8.3	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	3.9	5.6	2.3	6.3	2.3	6.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.3	3.2	4.4	2.0	4.8	2.0	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	2.2	3.0	3.9	1.9	4.2	1.9	4.4	ns
		$\overline{R}D$ to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	22.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.8	6.4	12.8	2.7	13.2	2.7	13.4	ns
		V _{CC} = 1.4 V to 1.6 V	2.6	4.5	7.5	2.3	8.1	2.3	8.4	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	3.3	5.8	2.3	6.3	2.3	6.7	ns
		V_{CC} = 2.3 V to 2.7 V	2.2	3.2	4.4	2.0	4.9	2.0	5.2	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	2.9	4.0	1.9	4.3	1.9	4.5	ns
f _{max}	maximum	CP; see <u>Figure 5</u> .								
	frequency	V _{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz
C _L = 15 p	F	11		1	1		I			
t _{pd}	propagation	CP to Q, \overline{Q} ; see <u>Figure 5</u> . ^[2]								
	delay	V _{CC} = 0.8 V	-	32.4	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.5	8.3	17.6	3.3	17.8	3.3	18.0	ns
		V _{CC} = 1.4 V to 1.6 V	3.2	5.6	9.5	2.8	10.5	2.8	11.1	ns
		V _{CC} = 1.65 V to 1.95 V	2.7	4.6	7.2	2.5	8.1	2.5	8.6	ns
		V _{CC} = 2.3 V to 2.7 V	2.4	3.6	5.2	2.2	5.8	2.2	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	2.2	3.2	4.4	2.0	4.9	2.0	5.2	ns
		\overline{SD} to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								

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Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	T _{amb} = 25 °C		°C	T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
		V _{CC} = 0.8 V	-	26.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.3	7.3	14.7	3.1	15.2	3.1	15.4	ns
		V _{CC} = 1.4 V to 1.6 V	3.2	5.2	8.3	2.9	9.0	2.9	9.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.8	4.3	6.4	2.5	7.1	2.5	7.5	ns
		V_{CC} = 2.3 V to 2.7 V	2.8	3.7	5.1	2.2	5.5	2.2	5.8	ns
		V _{CC} = 3.0 V to 3.6 V	2.5	3.5	4.6	2.4	5.0	2.4	5.2	ns
		$\overline{R}D$ to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	26.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.2	7.2	14.5	3.1	15.0	3.1	15.2	ns
		V _{CC} = 1.4 V to 1.6 V	3.1	5.1	8.4	2.7	9.2	2.7	9.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.7	4.3	6.5	2.6	7.3	2.6	7.7	ns
		V_{CC} = 2.3 V to 2.7 V	2.6	3.6	5.0	2.4	5.5	2.4	5.8	ns
		V _{CC} = 3.0 V to 3.6 V	2.4	3.4	4.6	2.3	5.0	2.3	5.2	ns
f _{max}	maximum	CP; see <u>Figure 5</u> .								
	frequency	V _{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C _L = 30 p	F	1			1		1	1		
t _{pd}	propagation	CP to Q, \overline{Q} ; see <u>Figure 5</u> . ^[2]								
	delay	V _{CC} = 0.8 V	-	42.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.2	10.6	22.5	4.0	23.0	4.0	23.3	ns
		V _{CC} = 1.4 V to 1.6 V	3.7	7.2	12.0	3.7	13.3	3.7	14.0	ns
		V _{CC} = 1.65 V to 1.95 V	3.5	5.8	9.2	3.4	10.4	3.4	11.0	ns
		V_{CC} = 2.3 V to 2.7 V	3.3	4.7	6.6	3.0	7.3	3.0	7.8	ns
		V _{CC} = 3.0 V to 3.6 V	3.0	4.3	5.8	2.8	6.8	2.8	7.3	ns
		\overline{SD} to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]								
		V _{CC} = 0.8 V	-	37.0	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.0	9.5	19.8	3.8	20.8	3.8	21.1	ns
		V _{CC} = 1.4 V to 1.6 V	3.8	6.7	10.9	3.7	12.0	3.7	12.7	ns
		V _{CC} = 1.65 V to 1.95 V	3.7	5.6	8.4	3.5	9.3	3.5	9.9	ns
		V_{CC} = 2.3 V to 2.7 V	3.7	4.8	6.6	3.2	7.2	3.2	7.6	ns
		V _{CC} = 3.0 V to 3.6 V	3.4	4.6	6.0	3.1	6.8	3.1	7.1	ns

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74AUP1G74-Q100

Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	neter Conditions		er Conditions T _{amb} = 25 °C		°C	T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max		
		$\overline{R}D$ to Q, \overline{Q} ; see <u>Figure 6</u> . ^[2]									
		V _{CC} = 0.8 V	-	36.4	-	-	-	-	-	ns	
		V _{CC} = 1.1 V to 1.3 V	3.9	9.4	19.5	3.8	20.2	3.8	20.5	ns	
		V _{CC} = 1.4 V to 1.6 V	3.6	6.6	10.9	3.7	12.0	3.7	12.6	ns	
		V _{CC} = 1.65 V to 1.95 V	3.5	5.5	8.5	3.5	9.5	3.5	10.1	ns	
		V_{CC} = 2.3 V to 2.7 V	3.5	4.7	6.5	3.2	7.1	3.2	7.6	ns	
		V _{CC} = 3.0 V to 3.6 V	3.3	4.4	6.1	3.1	7.1	3.1	7.5	ns	
f _{max}	maximum	CP; see <u>Figure 5</u> .									
	frequency	V _{CC} = 0.8 V	-	28	-	-	-	-	-	MHz	
		V _{CC} = 1.1 V to 1.3 V	-	145	-	70	-	70	-	MHz	
		V _{CC} = 1.4 V to 1.6 V	-	185	-	120	-	110	-	MHz	
		V _{CC} = 1.65 V to 1.95 V	-	270	-	150	-	120	-	MHz	
		V_{CC} = 2.3 V to 2.7 V	-	290	-	190	-	170	-	MHz	
		V _{CC} = 3.0 V to 3.6 V	-	315	-	200	-	190	-	MHz	
C _L = 5 pF	, 10 pF, 15 pF	and 30 pF		1	1	1	1	1	1		
t _{su}	set-up time	D to CP HIGH; see <u>Figure 5</u> .									
		V _{CC} = 0.8 V	_	3.4	_	_	_	-	-	ns	
		V _{CC} = 1.1 V to 1.3 V	-	0.6	-	1.2	-	1.2	-	ns	
		V _{CC} = 1.4 V to 1.6 V	-	0.3	-	0.6	-	0.6	-	ns	
		V _{CC} = 1.65 V to 1.95 V	-	0.4	-	0.5	-	0.5	-	ns	
		V _{CC} = 2.3 V to 2.7 V	-	0.2	-	0.4	-	0.4	-	ns	
		V _{CC} = 3.0 V to 3.6 V	-	0.3	-	0.4	-	0.4	-	ns	
		D to CP LOW; see <u>Figure 5</u> .									
		V _{CC} = 0.8 V	-	3.0	-	-	-	-	-	ns	
		V _{CC} = 1.1 V to 1.3 V	-	0.5	-	1.2	-	1.2	-	ns	
		V _{CC} = 1.4 V to 1.6 V	-	0.3	-	0.7	-	0.7	-	ns	
		V _{CC} = 1.65 V to 1.95 V	-	0.4	-	0.7	-	0.7	-	ns	
		V _{CC} = 2.3 V to 2.7 V	-	0.5	-	0.7	-	0.7	-	ns	
		V _{CC} = 3.0 V to 3.6 V	-	0.6	-	0.8	-	0.8	-	ns	
t _h	hold time	D to CP; see <u>Figure 5</u> .									
		V _{CC} = 0.8 V	-	-1.9	-	-	-	-	-	ns	
		V _{CC} = 1.1 V to 1.3 V	-	-0.3	-	0.5	-	0.5	-	ns	
		V _{CC} = 1.4 V to 1.6 V	-	-0.2	-	0.2	-	0.2	-	ns	

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74AUP1G74-Q100

Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Ta	amb = 25	°C	T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Мах	Min	Max	
		V _{CC} = 1.65 V to 1.95 V	-	-0.2	-	0.1	-	0.1	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	-0.2	-	0.1	-	0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	-0.2	-	0.1	-	0.1	-	ns
t _{rec}	recovery	RD; see Figure 6								
	time	V _{CC} = 1.1 V to 1.3 V	-	-0.5	-	-0.9	-	-0.9	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	-0.2	-	-0.6	-	-0.6	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	-0.2	-	-0.4	-	-0.4	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	-0.1	-	-0.1	-	-0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	-0.1	-	-0.1	-	-0.1	-	ns
		SD; see <u>Figure 6</u> .								
		V _{CC} = 1.1 V to 1.3 V	-	-0.5	-	-0.3	-	-0.3	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	-0.4	-	-0.1	-	-0.1	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	-0.3	-	0	-	0	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	-0.2	-	0.1	-	0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	-0.1	-	0.1	-	0.1	-	ns
t _W	pulse width	CP HIGH or LOW; see <u>Figure 5</u> .								
		V _{CC} = 1.1 V to 1.3 V	-	2.1	-	2.7	-	2.7	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	1.1	-	1.5	-	1.5	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.9	-	1.6	-	1.6	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.6	-	1.7	-	1.7	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.6	-	1.9	-	1.9	-	ns
		SD or RD LOW; see <u>Figure 6</u> .								
		V _{CC} = 1.1 V to 1.3 V	-	4.2	-	11.3	-	11.5	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	2.3	-	6.2	-	6.4	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	1.8	-	4.8	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	1.2	-	3.3	-	3.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	1.1	-	2.6	-	2.8	-	ns
C _{PD}	power dissipation	$f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{\text{CC}}$ ^[3]								
	capacitance	V _{CC} = 0.8 V	-	2.8	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.9	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	3.0	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	3.0	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.5	-	-	-	-	-	pF

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Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Ta	T _{amb} = 25 °C				T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ ^[1]	Мах	Min	Мах	Min	Мах	
		V_{CC} = 3.0 V to 3.6 V	-	3.9	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$

f_i = input frequency in MHz;

 f_o = output frequency in MHz;

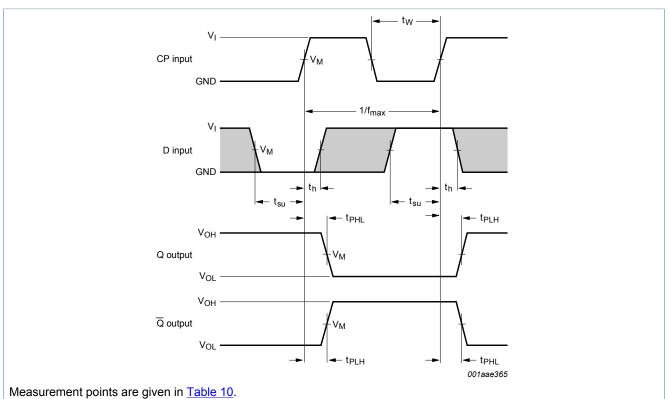
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.

11.1 Waveforms and test circuit

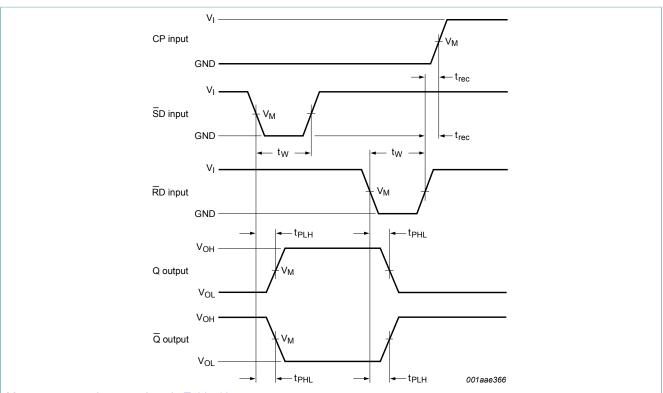


The shaded areas indicate when the input is permitted to change for predictable output performance. V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. The clock input (CP) to output (Q, \overline{Q}) propagation delays, the data input (D) to clock input (CP) set-up and hold times and the clock input (CP) pulse width and maximum frequency

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Low-power D-type flip-flop with set and reset; positive-edge trigger



Measurement points are given in <u>Table 10</u>.

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. The set input (\overline{SD}) and reset input (\overline{RD}) to output (\overline{Q} , \overline{Q}) propagation delays, the set input (\overline{SD}) and reset input (\overline{RD}) pulse widths and the reset input (\overline{RD}) to clock input (CP) recovery time

Table 10. Measurement points

Supply voltage	Output	Input		
V _{cc}	V _M	V _M	VI	$\mathbf{t_r} = \mathbf{t_f}$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{CC}	≤ 3.0 ns

Low-power D-type flip-flop with set and reset; positive-edge trigger

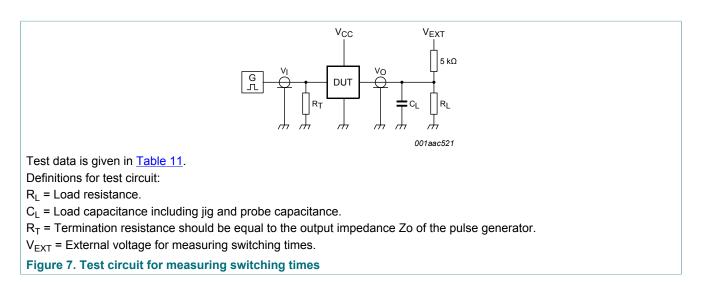


Table 11. Test data

Supply voltage	Load	V _{EXT}			
V _{cc}	CL	R _L ^[1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V _{CC}

[1] For measuring enable and disable times $R_L = 5 k\Omega$.

For measuring propagation delays, setup and hold times and pulse width R_L = 1 M Ω .

Low-power D-type flip-flop with set and reset; positive-edge trigger

12 Package outline

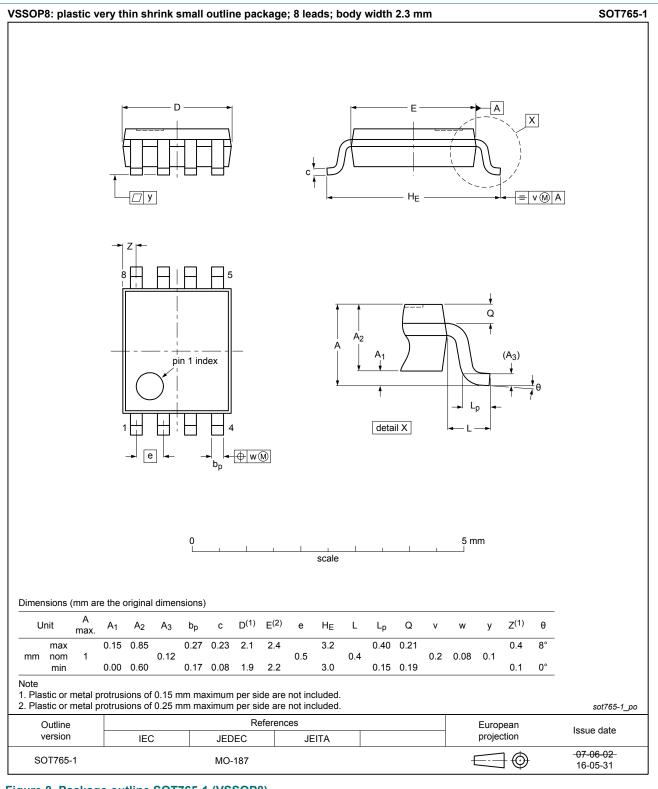


Figure 8. Package outline SOT765-1 (VSSOP8)

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13 Abbreviations

Table 12. Abbreviations					
Acronym	Description				
CDM	Charged Device Model				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
НВМ	Human Body Model				
MIL	Military				
ММ	Machine Model				

14 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74AUP1G74_Q100 v.2	20170410	Product data sheet	-	74AUP1G74_Q100 v.1		
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 					
74AUP1G74_Q100 v.1	20150527	Product data sheet	-	-		

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

Please consult the most recently issued document before initiating or completing a design. [1]

The term 'short data sheet' is explained in section "Definitions".

[2] [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

15.2 Definitions

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74AUP1G74 Q100 **Product data sheet**

Low-power D-type flip-flop with set and reset; positive-edge trigger

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