

74AUP1G80

Low-power D-type flip-flop; positive-edge trigger

Rev. 6 — 22 February 2022

Product data sheet

1. General description

The 74AUP1G80 is a single positive-edge triggered D-type flip-flop. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and its complement will appear at the \bar{Q} output. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G80GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G80GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G80GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74AUP1G80GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AUP1G80GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AUP1G80GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3

4. Marking

Table 2. Marking

Type number	Marking code [1]
74AUP1G80GW	pT
74AUP1G80GM	pT
74AUP1G80GF	pT
74AUP1G80GN	pT
74AUP1G80GS	pT
74AUP1G80GX	pT

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

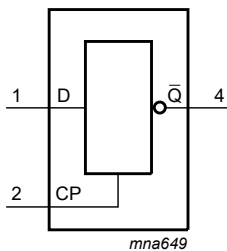


Fig. 1. Logic symbol

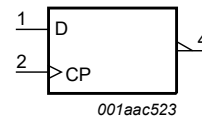


Fig. 2. IEC logic symbol

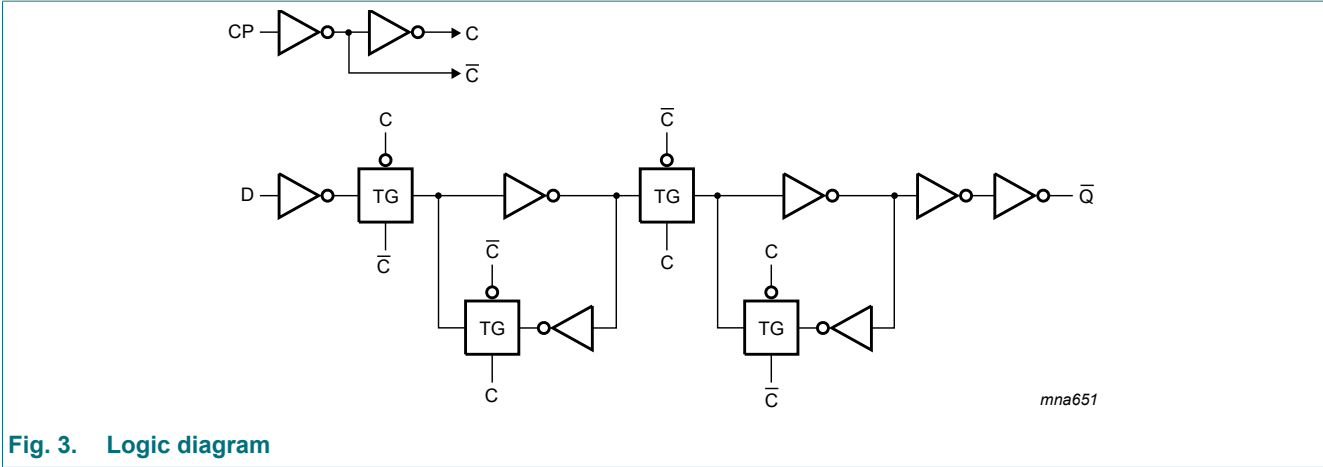


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

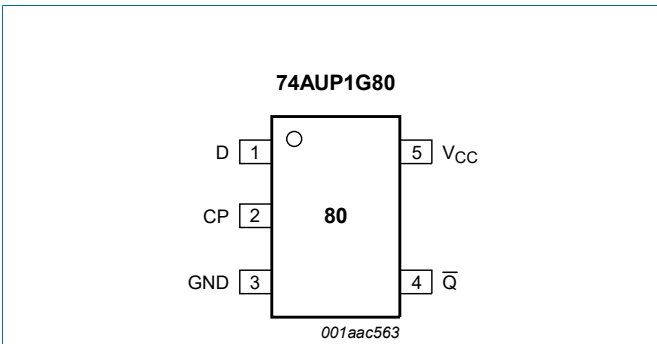


Fig. 4. Pin configuration SOT353-1 (TSSOP5)

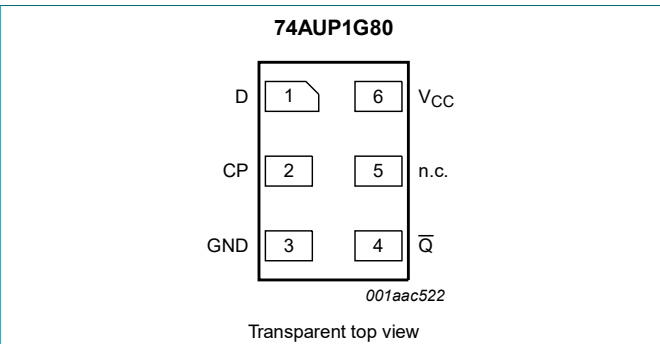


Fig. 5. Pin configuration SOT886 (XSON6)

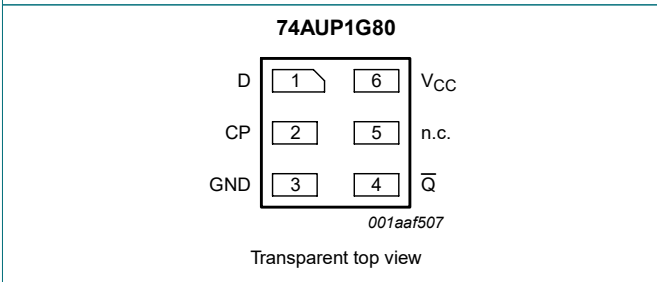


Fig. 6. Pin configuration SOT891, SOT1115 and SOT1202 (XSON6)

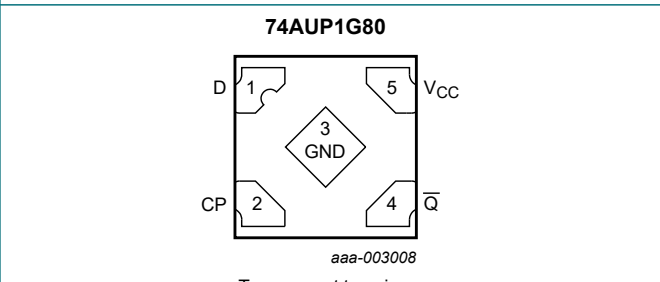


Fig. 7. Pin configuration SOT1226-3 (X2SON5)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
D	1	1	data input
CP	2	2	clock pulse input
GND	3	3	ground (0 V)
\bar{Q}	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; \uparrow = LOW-to-HIGH CP transition; X = don't care;

\bar{q} = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

Input		Output
CP	D	\bar{Q}
\uparrow	L	H
\uparrow	H	L
L	X	\bar{q}

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	+20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT891 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode and Power-down mode	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8\text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8\text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 0.8\text{ V to }3.6\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1\text{ mA}$; $V_{CC} = 1.1\text{ V}$	$0.75 \times V_{CC}$	-	-	V
		$I_O = -1.7\text{ mA}$; $V_{CC} = 1.4\text{ V}$	1.11	-	-	V
		$I_O = -1.9\text{ mA}$; $V_{CC} = 1.65\text{ V}$	1.32	-	-	V
		$I_O = -2.3\text{ mA}$; $V_{CC} = 2.3\text{ V}$	2.05	-	-	V
		$I_O = -3.1\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -2.7\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.72	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 0.8\text{ V to }3.6\text{ V}$	-	-	0.1	V
		$I_O = 1.1\text{ mA}$; $V_{CC} = 1.1\text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7\text{ mA}$; $V_{CC} = 1.4\text{ V}$	-	-	0.31	V
		$I_O = 1.9\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	-	0.31	V
		$I_O = 2.3\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.31	V
		$I_O = 3.1\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.44	V
		$I_O = 2.7\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.31	V
	$I_O = 4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.44	V	

Low-power D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.1	μA
I_{OFF}	power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.2	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.2	μA
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$ [1]	-	-	40	μA
C_I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$	-	1.5	-	pF
C_O	output capacitance	$V_O = \text{GND}; V_{CC} = 0 \text{ V}$	-	3.0	-	pF
$T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8 \text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8 \text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	V
		$I_O = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.30	-	-	V
		$I_O = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_O = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_O = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 20 \mu\text{A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.1	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
I_I	input leakage current	$V_I = \text{GND to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	± 0.5	μA
		$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	± 0.5	μA
ΔI_{OFF}	additional power-off leakage current	$V_I \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	± 0.6	μA
I_{CC}	supply current	$V_I = \text{GND or } V_{CC}; I_O = 0 \text{ A}; V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.9	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$ [1]	-	-	50	μA

Low-power D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Fig. 10)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t _{pd}	propagation delay	CP to \bar{Q} ; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	20.9	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.9	6.0	12.9	2.6	14.3	2.6	15.7	ns
		V _{CC} = 1.4 V to 1.6 V	1.9	4.2	7.6	2.0	8.9	2.0	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.4	5.9	1.6	7.0	1.6	7.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.6	4.3	1.2	5.6	1.2	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	2.2	3.6	1.0	4.4	1.0	4.8	ns
f _{max}	maximum frequency	CP; see Fig. 9								
		V _{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C_L = 10 pF										
t _{pd}	propagation delay	CP to \bar{Q} ; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	24.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.3	6.9	14.9	3.0	16.5	3.0	18.1	ns
		V _{CC} = 1.4 V to 1.6 V	2.6	4.8	8.8	2.3	10.3	2.3	11.3	ns
		V _{CC} = 1.65 V to 1.95 V	2.3	3.9	6.8	2.0	8.1	2.0	8.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.9	3.1	5.1	1.7	6.3	1.7	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.7	4.4	1.4	4.9	1.4	5.4	ns
f _{max}	maximum frequency	CP; see Fig. 9								
		V _{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz
C_L = 15 pF										
t _{pd}	propagation delay	CP to \bar{Q} ; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	28.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.0	7.6	16.7	3.4	18.6	3.4	20.5	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.3	9.8	2.6	11.5	2.6	12.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	4.4	7.6	2.3	9.1	2.3	10.0	ns
		V _{CC} = 2.3 V to 2.7 V	2.2	3.5	5.7	2.0	6.9	2.0	7.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	3.1	5.0	1.8	5.5	1.8	6.1	ns

Low-power D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	CP; see Fig. 9								
		V _{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C_L = 30 pF										
t _{pd}	propagation delay	CP to Q̄; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	38.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.9	9.8	20.7	4.4	24.7	4.4	27.2	ns
		V _{CC} = 1.4 V to 1.6 V	4.0	6.8	12.7	3.5	15.0	3.5	16.5	ns
		V _{CC} = 1.65 V to 1.95 V	3.5	5.6	9.9	2.2	11.9	2.2	13.0	ns
		V _{CC} = 2.3 V to 2.7 V	3.1	4.5	7.5	2.8	9.3	2.8	10.2	ns
		V _{CC} = 3.0 V to 3.6 V	2.9	4.1	6.4	2.7	7.5	2.7	8.3	ns
f _{max}	maximum frequency	CP; see Fig. 9								
		V _{CC} = 0.8 V	-	28	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t _{su(H)}	set-up time HIGH	D to CP; see Fig. 9								
		V _{CC} = 0.8 V	-	2.5	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.5	-	2.2	-	2.2	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.3	-	1.1	-	1.1	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.3	-	0.8	-	0.8	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.2	-	0.6	-	0.6	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.2	-	0.4	-	0.4	-	ns
t _{su(L)}	set-up time LOW	D to CP; see Fig. 9								
		V _{CC} = 0.8 V	-	1.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.3	-	2.0	-	2.0	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.2	-	1.3	-	1.3	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.2	-	1.1	-	1.1	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.3	-	0.8	-	0.8	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.3	-	0.7	-	0.7	-	ns

Low-power D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t _h	hold time	D to CP; see Fig. 9								
		V _{CC} = 0.8 V	-	-2.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	-0.4	-	0.2	-	0.2	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	-0.3	-	0.1	-	0.1	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	-0.2	-	0	-	0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	-0.2	-	0	-	0	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	-0.3	-	0	-	0	-	ns
t _w	pulse width	CP HIGH or LOW; see Fig. 9								
		V _{CC} = 0.8 V	-	5.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	1.0	-	3.0	-	3.0	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.8	-	2.0	-	2.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.6	-	2.0	-	2.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.5	-	2.0	-	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	-	0.5	-	2.0	-	2.0	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 0.8 V	-	1.8	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	1.8	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	1.9	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.0	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	2.4	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	2.9	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1. Waveforms

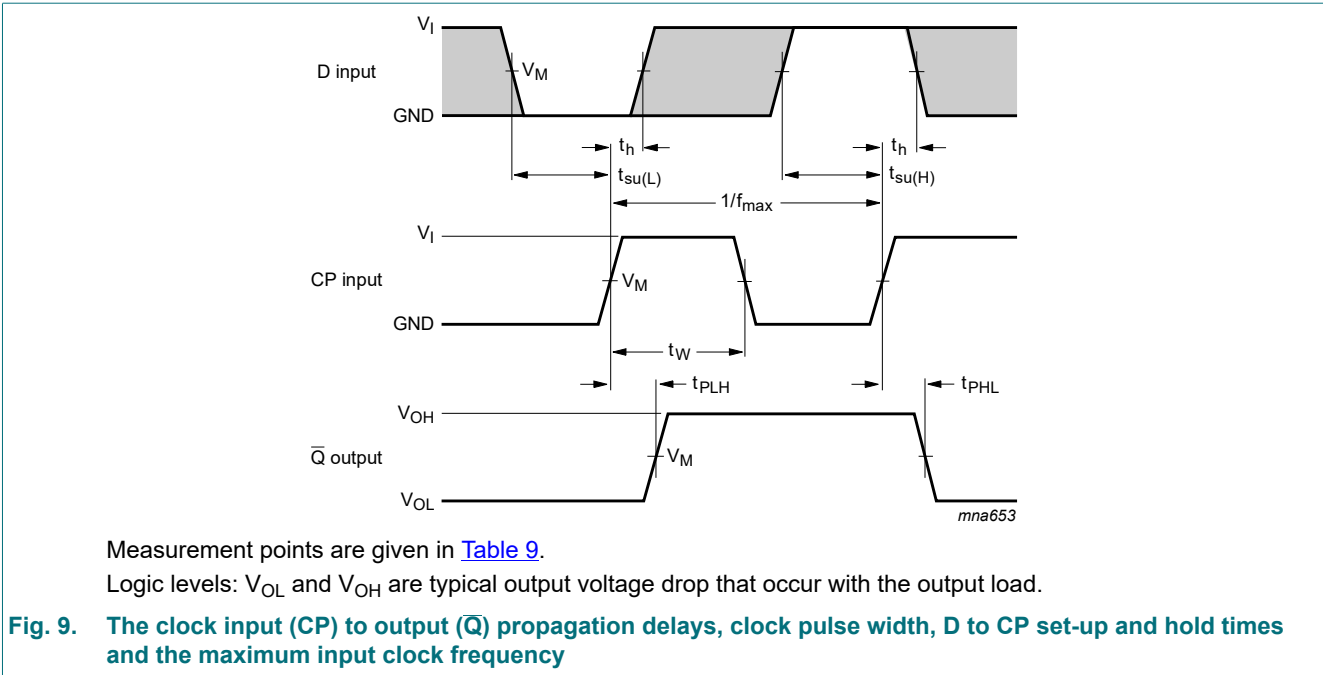
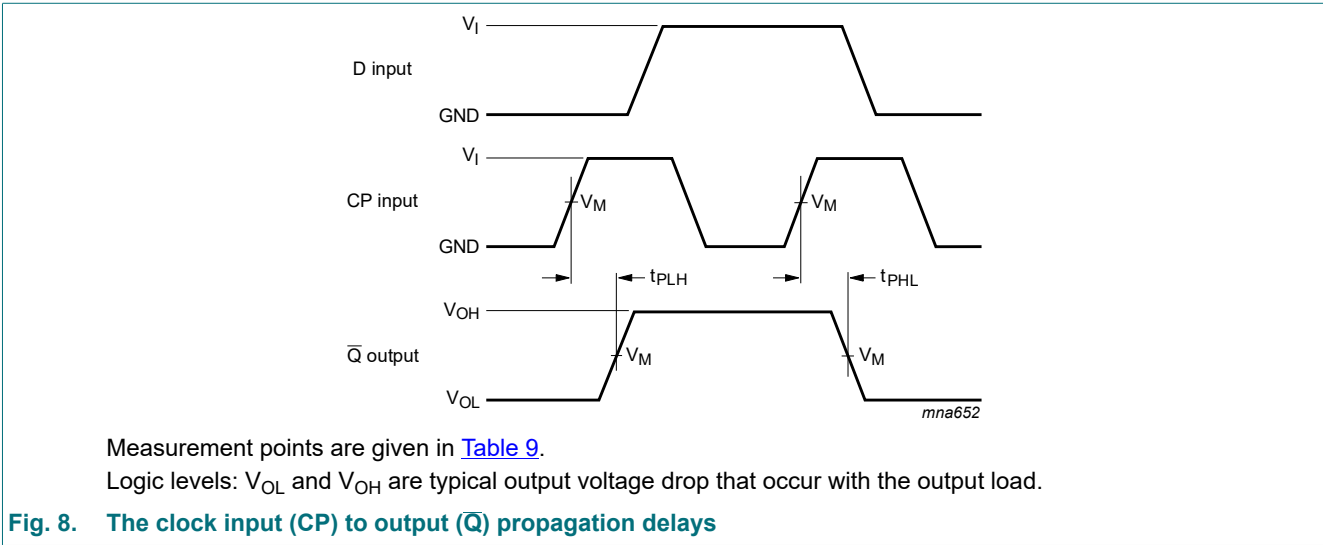


Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns

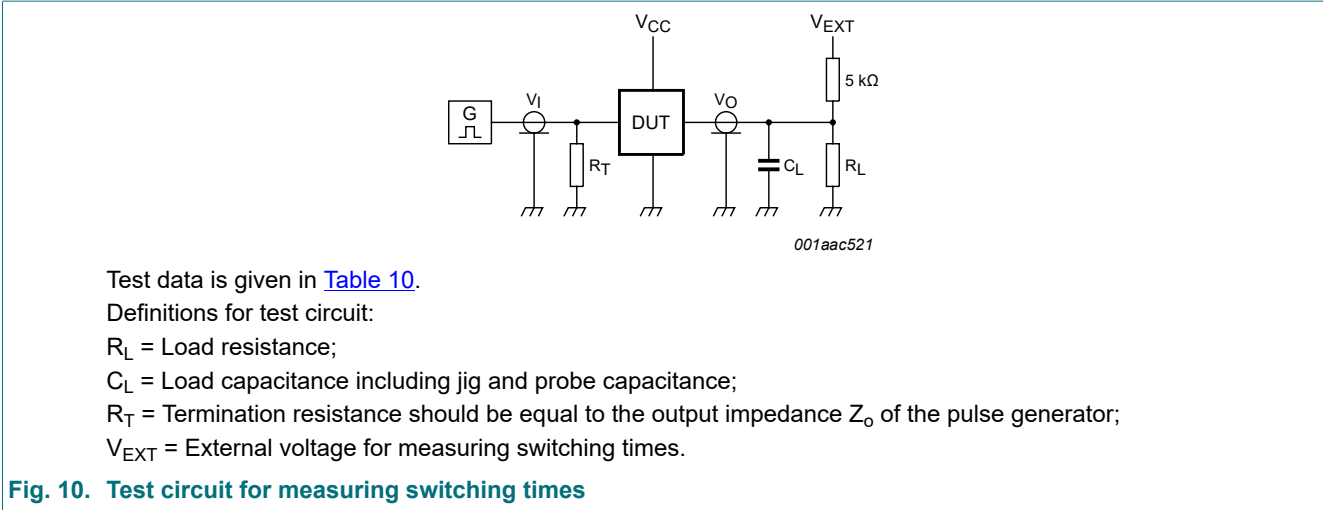


Fig. 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 \text{ k}\Omega$.
 For measuring propagation delays, setup and hold times and pulse width $R_L = 1 \text{ M}\Omega$.

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

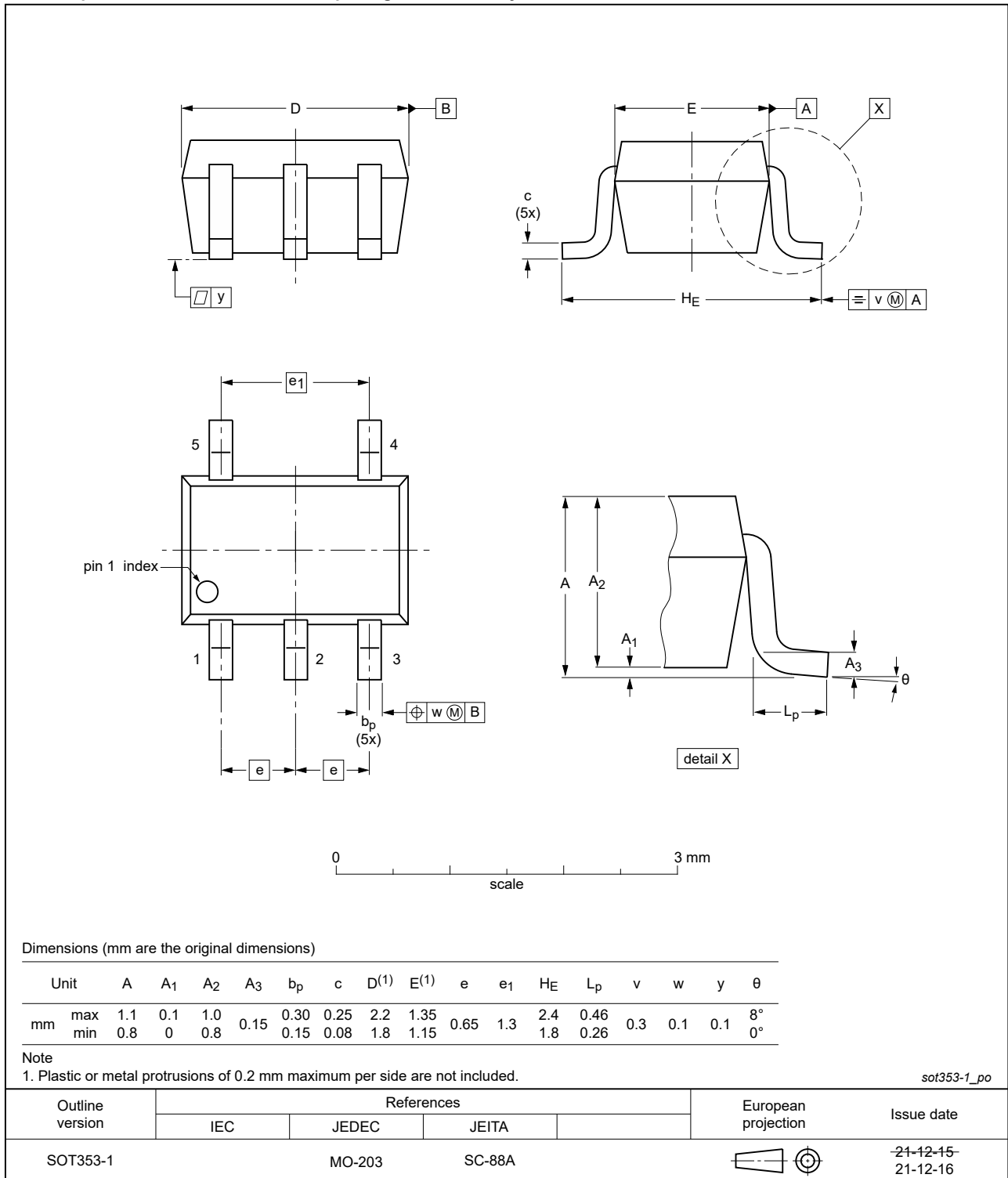


Fig. 11. Package outline SOT353-1 (TSSOP5)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

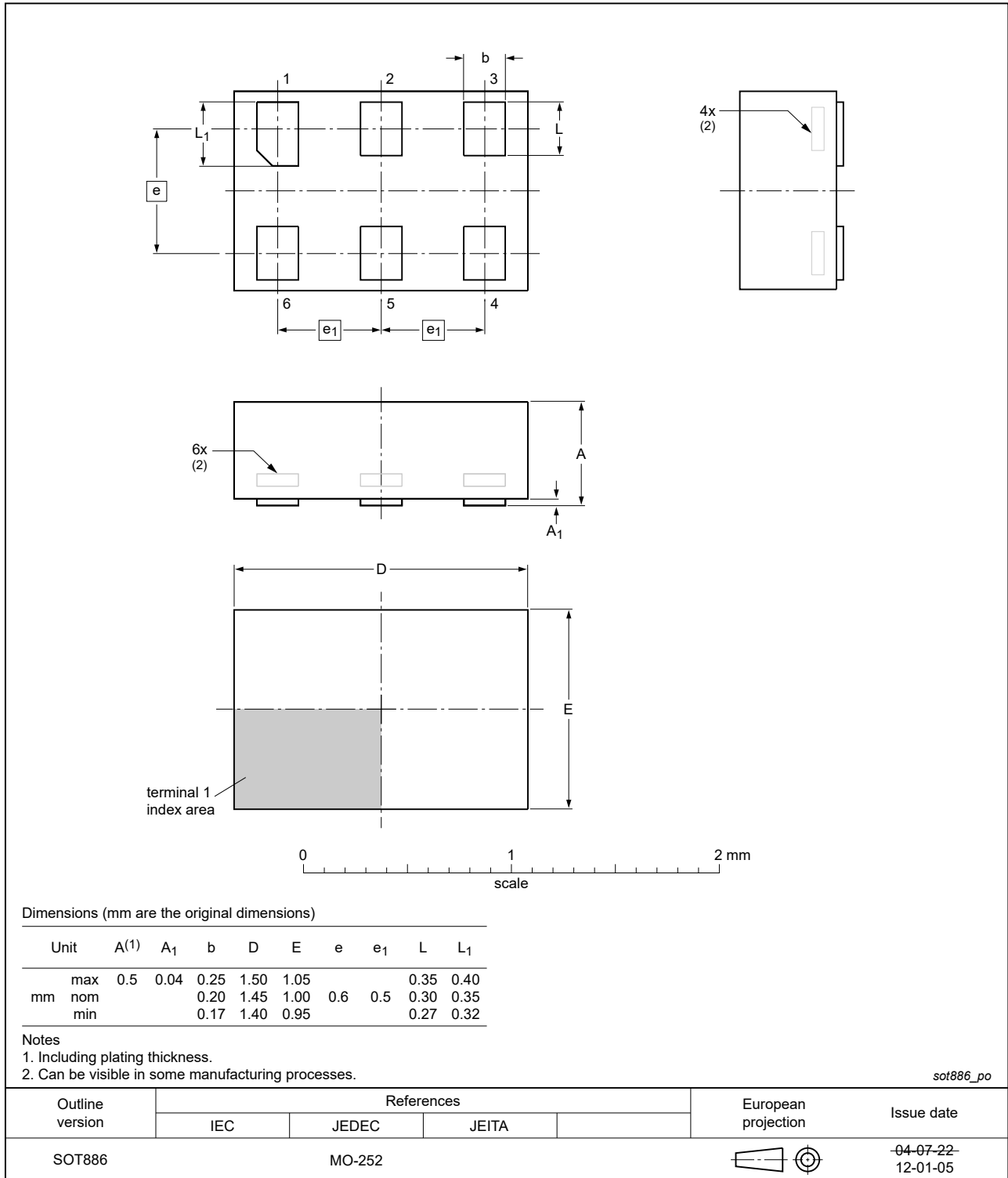


Fig. 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

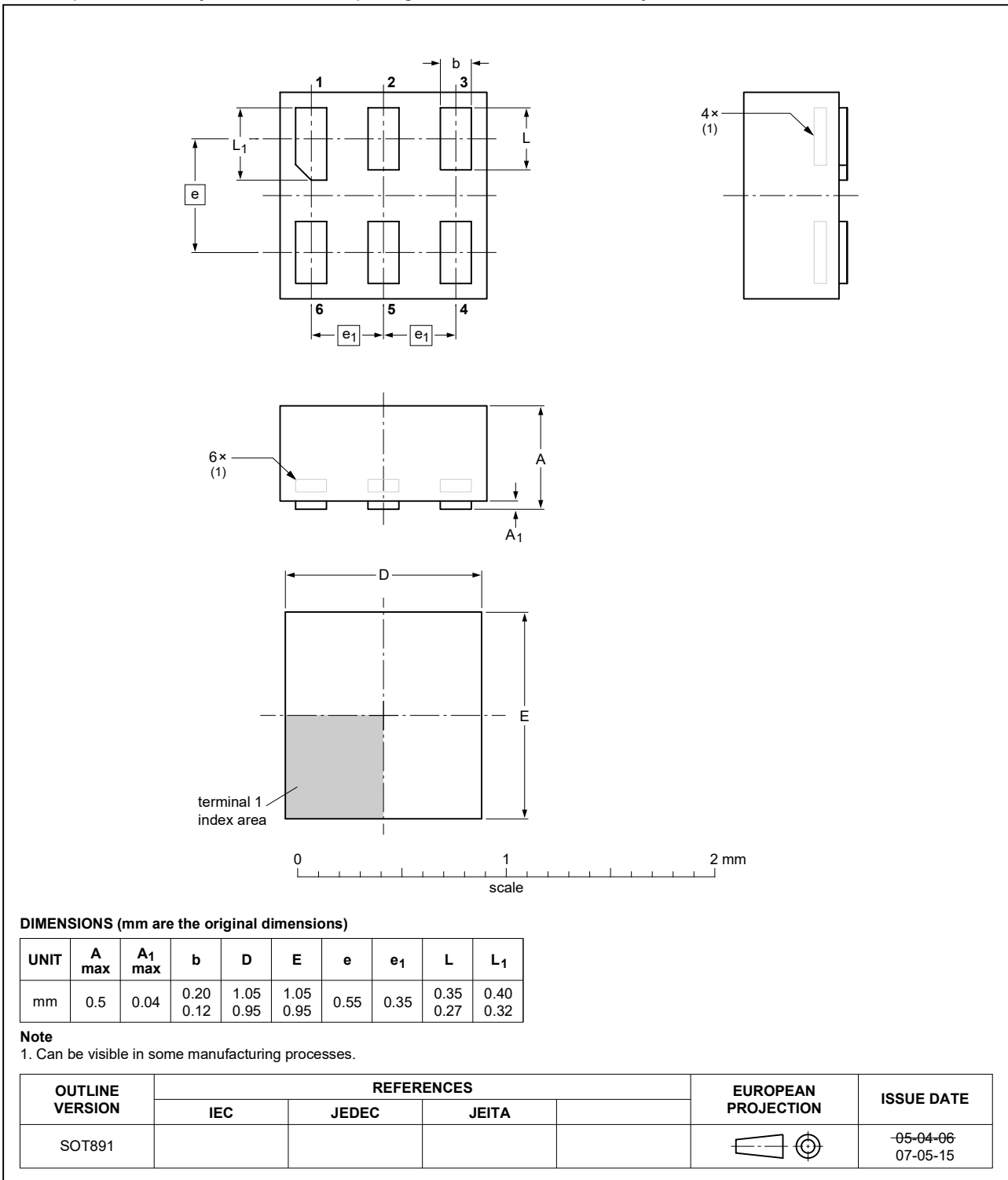


Fig. 13. Package outline SOT891 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115

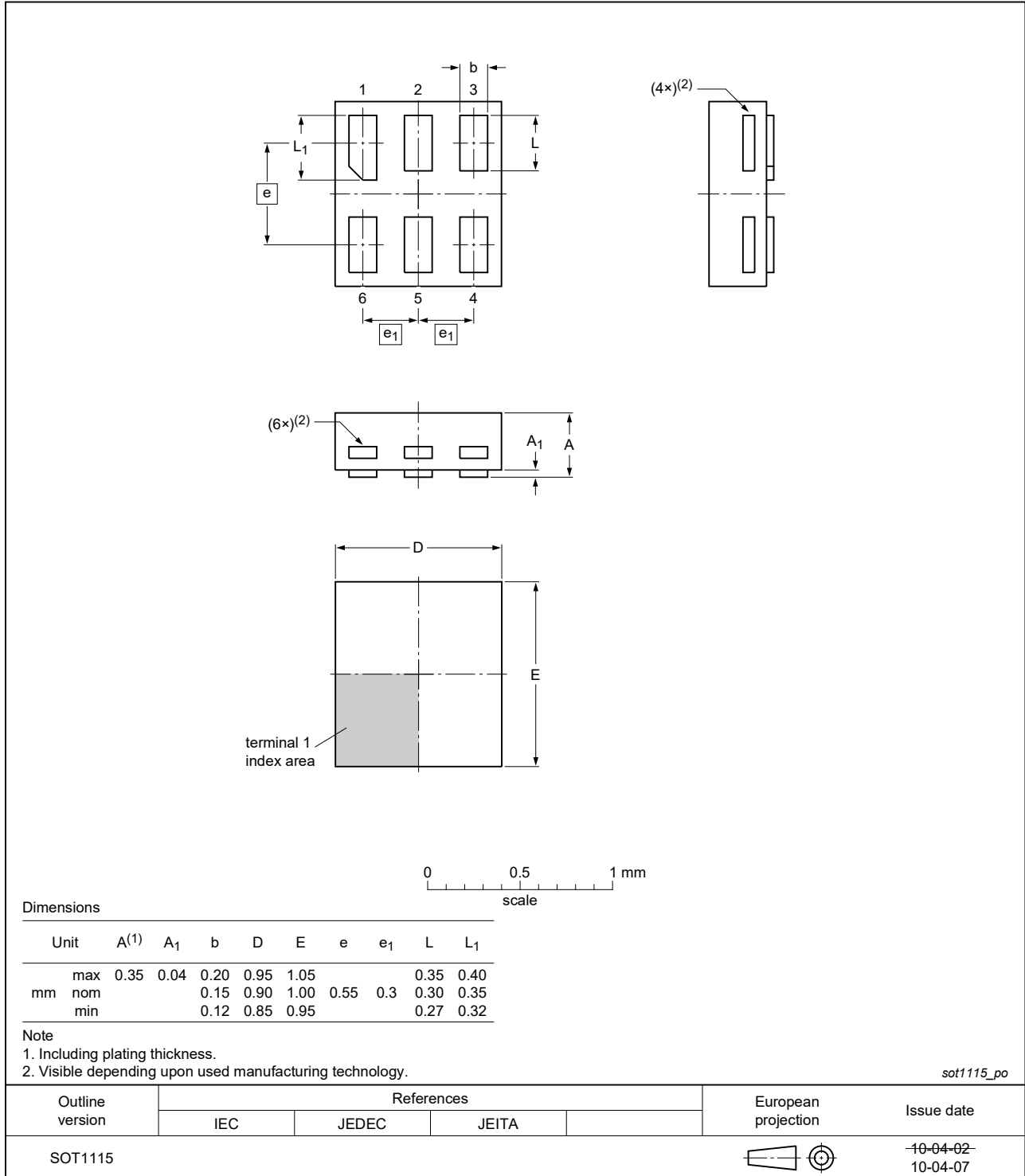


Fig. 14. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Fig. 15. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;
5 terminals; body 0.8 x 0.8 x 0.32 mm

SOT1226-3



Fig. 16. Package outline SOT1226-3 (X2SON5)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G80 v.6	20220222	Product data sheet	-	74AUP1G80 v.5
Modifications:	<ul style="list-style-type: none"> Package SOT1226 (X2SON5) changed to SOT1226-3 (X2SON5). 			
74AUP1G80 v.5	20220207	Product data sheet	-	74AUP1G80 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 11: Package outline drawing for SOT353-1 has changed. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. 			
74AUP1G80 v.4	20120628	Product data sheet	-	74AUP1G80 v.3
Modifications:	<ul style="list-style-type: none"> Added type number 74AUP1G80GX (SOT1226). Package outline drawing of SOT886 (Fig. 12) modified. 			
74AUP1G80 v.3	20111129	Product data sheet	-	74AUP1G80 v.2
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74AUP1G80 v.2	20100915	Product data sheet	-	74AUP1G80 v.1
74AUP1G80 v.1	20061020	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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