74CBTLVD3245

8-bit level-shifting bus switch with output enable Rev. 4 — 22 January 2016 Pro-

Product data sheet

General description

The 74CBTLVD3245 is an 8-pole, single-throw bus switch. The device features a single output enable input (OE) that controls eight switch channels. The switches are disabled when OE is HIGH. Schmitt trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features and benefits 2.

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- \blacksquare 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

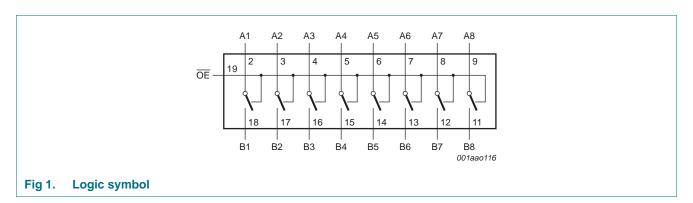


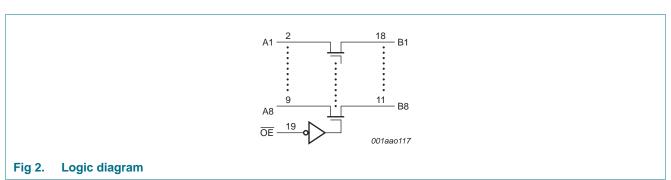
3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74CBTLVD3245PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1				
74CBTLVD3245BQ	–40 °C to +125 °C		plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm	SOT764-1				

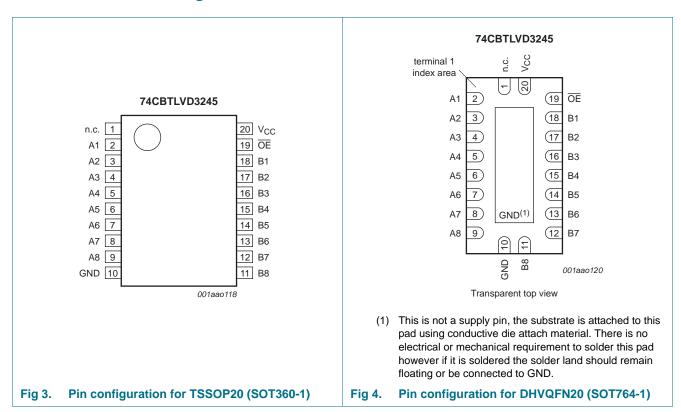
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A1 to A8	2, 3, 4, 5, 6, 7, 8, 9	data input/output (A port)
GND	10	ground (0 V)
B1 to B8	18, 17, 16, 15, 14, 13, 12, 11	data input/output (B port)
ŌĒ	19	output enable input (active LOW)
V _{CC}	20	positive supply voltage

6. Functional description

Table 3. Function selection[1]

Input OE	Input/output
OE	An, Bn
L	An = Bn
Н	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

	B	0	201			
Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage	[1	<u>]</u>	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _{I/O} < -0.5 V		-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V		-50	-	mA
I _{SW}	switch current	$V_{SW} = 0 \text{ V to } V_{CC}$		-	±128	mA
I _{CC}	supply current			-	+100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	2]	-	500	mW

^[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		3.0	3.6	V
VI	input voltage		0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	0	200	ns/V

^[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions $T_{amb} = -40 \text{ °C to } +8$		+85 °C	T _{amb} = -40 °0	40 °C to +125 °C		
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
II	input leakage current	pin \overline{OE} ; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1	-	±20	μΑ
V _{pass}	pass voltage	V _I = V _{CC} ; see <u>Figure 7</u> to <u>Figure 11</u>	-	-	-	-	-	V

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^[2] For SSOP20 and TSSOP20 packages: above 60 $^{\circ}$ C the value of P_{tot} derates linearly at 5.5 mW/K. For DHVQFN20 packages: above 60 $^{\circ}$ C the value of P_{tot} derates linearly at 4.5 mW/K.

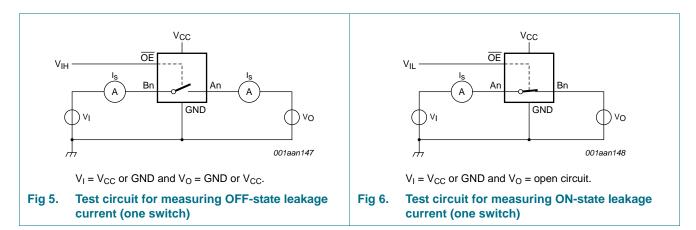
Table 6. Static characteristics ... continued

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Т	amb =	-40 °C to	+85 °C	T _{amb} = -40 °C	C to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
I _{S(OFF)}	OFF-state leakage current	$V_{CC} = 3.6 \text{ V}$; see Figure 5		-	-	±1	-	±20	μΑ
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see <u>Figure 6</u>		-	-	±1	-	±20	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V		-	-	±10	-	±50	μΑ
I _{CC}	supply current	$V_I = V_{CC}$; $I_O = 0$ A; $V_{CC} = 3.6$ V; $V_{SW} = GND$ or V_{CC}		-	-	20	-	50	μΑ
		$V_I = GND$; $I_O = 0$ A; $V_{CC} = 3.6$ V; $V_{SW} = GND$ or V_{CC}		-	-	100	-	150	μΑ
Δl _{CC}	additional supply current	pin \overline{OE} ; $V_1 = V_{CC} - 0.6 \text{ V}$; $V_{SW} = \text{GND or } V_{CC}$; $V_{CC} = 3.6 \text{ V}$	[2]	-	-	300	-	2000	μΑ
C _I	input capacitance	pin OE; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V		-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	$V_{CC} = 3.3 \text{ V}; V_{I} = 0 \text{ V to } 3.3 \text{ V}$		-	2.5	-	-	-	pF
C _{S(ON)}	ON-state capacitance	$V_{CC} = 3.3 \text{ V}; V_I = 0 \text{ V to } 3.3 \text{ V}$		-	9.0	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] One input at 3 V, other inputs at V_{CC} or GND.

9.1 Test circuits



9.2 Typical pass voltage graphs

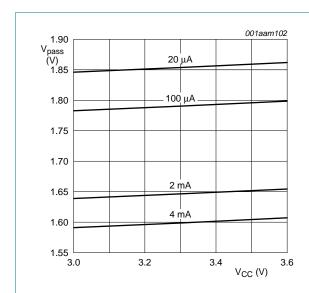


Fig 7. Pass voltage versus supply voltage; $T_{amb} = 125$ °C (typical)

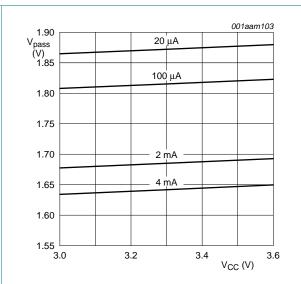


Fig 8. Pass voltage versus supply voltage; T_{amb} = 85 °C (typical)

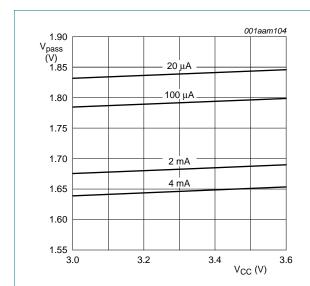


Fig 9. Pass voltage versus supply voltage; T_{amb} = 25 °C (typical)

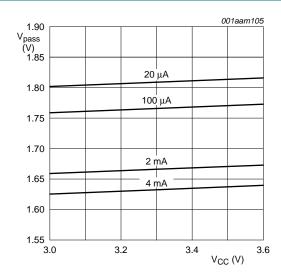
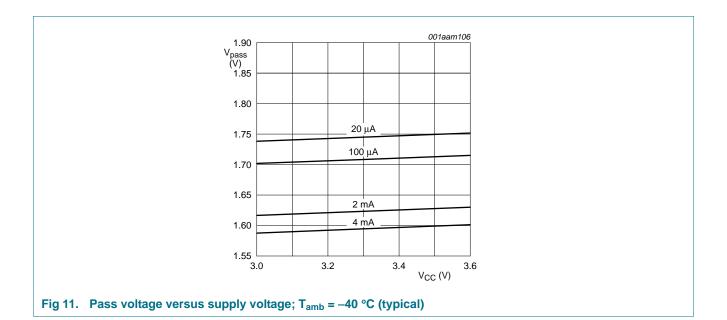


Fig 10. Pass voltage versus supply voltage; $T_{amb} = 0$ °C (typical)



9.3 ON resistance

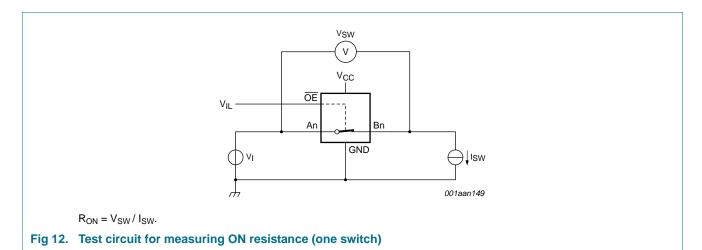
Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 12.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T _{amb} = -40 °0	Unit	
			Min	Typ[1]	Max	Min	Max	
R _{ON}	ON resistance	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}^{2}$						
		$I_{SW} = 64 \text{ mA}; V_I = 0 \text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{SW} = 24 \text{ mA}; V_I = 0 \text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{SW} = 15 \text{ mA}; V_I = 1.2 \text{ V}$	-	4.7	10.0	-	12.0	Ω

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.4 ON resistance test circuit



10. Dynamic characteristics

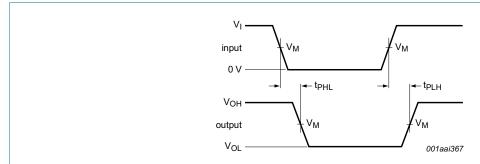
Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Figure 15

Symbol	Parameter	Conditions	T _{amb} = -	T_{amb} = -40 °C to +85 °C			$T_{amb} = -40$ °C to +125 °C		
			Min	Typ[1]	Max	Min	Max		
t _{pd} propagation delay		An to Bn or Bn to An; see Figure 13							
		V _{CC} = 3.0 V to 3.6 V	-	-	0.11	-	0.22	ns	
t _{en} enable time		OE to An or Bn; [4] see Figure 14							
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	5.0	1.5	6.0	ns	
t _{dis}	disable time	OE to An or Bn; see Figure 14							
		V _{CC} = 3.0 V to 3.6 V	0.8	3.4	7.0	0.8	8.0	ns	

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC} .
- [2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL} .
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

11. Waveforms



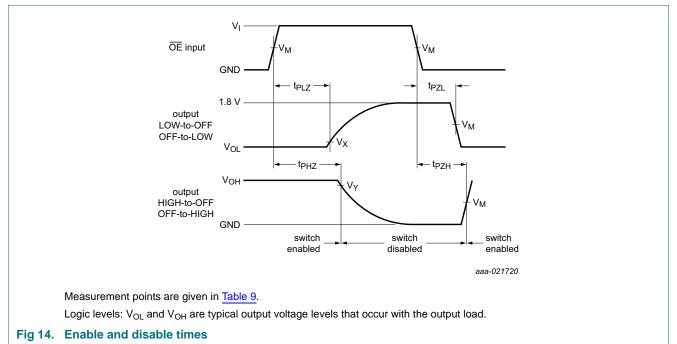
Measurement points are given in Table 9.

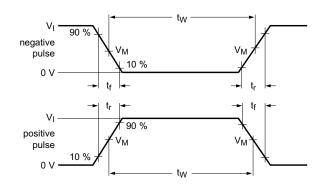
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

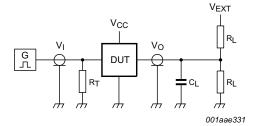
Fig 13. The data input (An, Bn) to output (Bn, An) propagation delay times

Table 9. Measurement points

Supply voltage	Input			Output		
V _{cc}	V _M	VI	$t_r = t_f$	V _M	V _X	V _Y
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.9 V	V _{OL} + 0.15 V	V _{OH} – 0.15 V







Test data is given in Table 10.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 15. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V _{EXT}			
V _{CC}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
3.0 V to 3.6 V	30 pF	1 kΩ	open	GND	3.6 V	

11.1 Additional dynamic characteristics

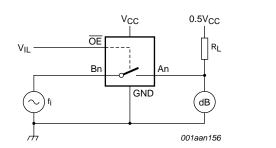
Table 11. Additional dynamic characteristics

GND = 0 V.

Symbol	Parameter	Conditions		T _{amb} = 25 °C			Unit
				Min	Тур	Max	
f _(-3dB)	-3 dB frequency response	$V_{CC} = 3.3 \text{ V}; R_L = 50 \Omega; \text{ see } \frac{\text{Figure 16}}{\text{Figure 16}}$	[1]	-	575	-	MHz

[1] f_i is biased at 0.5 V_{CC} .

11.2 Test circuit



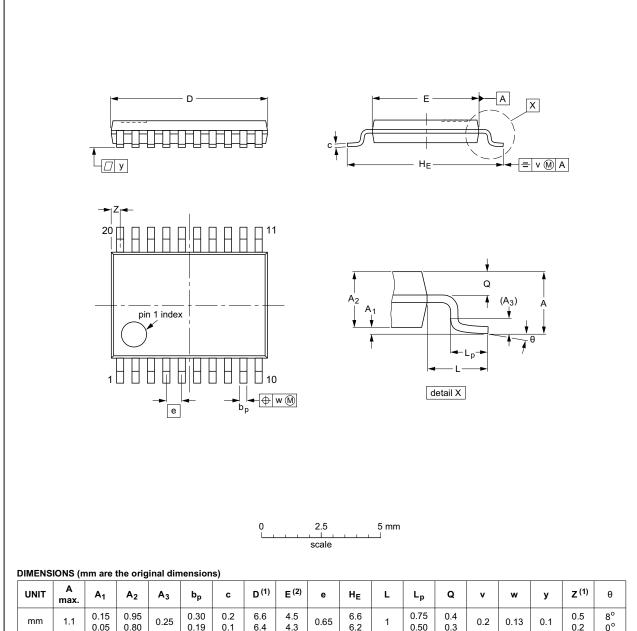
 $\label{eq:definition} \mbox{Adjust } f_i \mbox{ voltage to obtain 0 dBm level at output. Increase } f_i \mbox{ frequency until dB meter reads } -3 \mbox{ dB}.$

Fig 16. Test circuit for measuring the frequency response when channel is in ON-state

12. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT360-1		MO-153				99-12-27 03-02-19

Fig 17. Package outline SOT360-1 (TSSOP20)

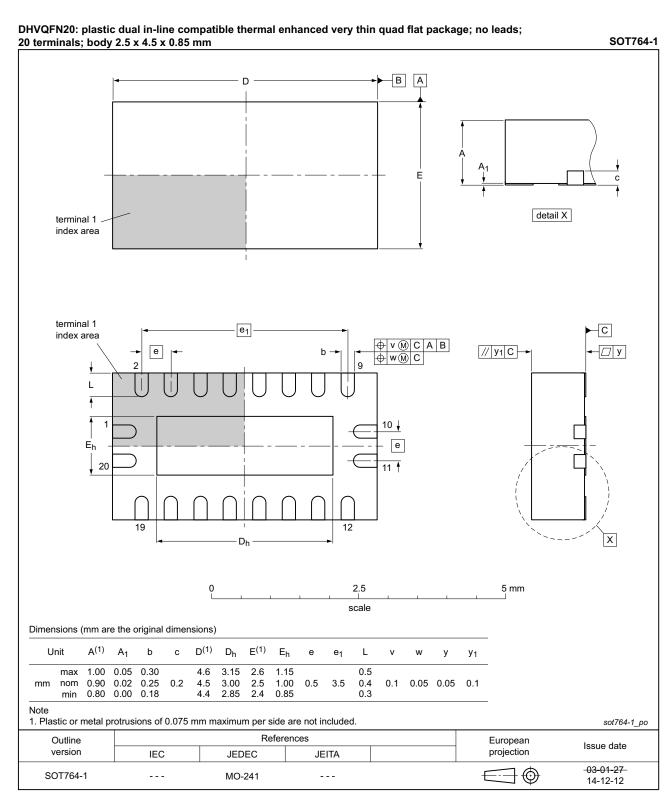


Fig 18. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description			
CDM	Charged Device Model			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
HBM	Human Body Model			
MM	Machine Model			

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74CBTLVD3245 v.4	20160122	Product data sheet	-	74CBTLVD3245 v.3				
Modifications:	Type number 74CBTLVD3245DS removed.							
	• Figure 14 updated.							
74CBTLVD3245 v.3	20111216	Product data sheet	-	74CBTLVD3245 v.2				
Modifications:	Legal pages updated.							
74CBTLVD3245 v.2	20111012	Product data sheet	-	74CBTLVD3245 v.1				
74CBTLVD3245 v.1	20110506	Product data sheet	-	-				

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition					
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.					
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.					
Product [short] data sheet	Production	This document contains the product specification.					

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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