

Description

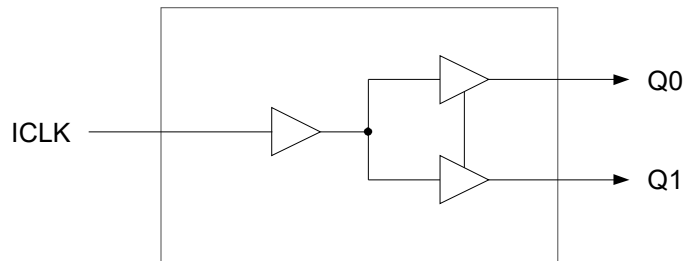
The 74FCT38072S is a low skew, single input to two output, clock buffer. The 74FCT38072S has best in class additive phase Jitter of sub 50 fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

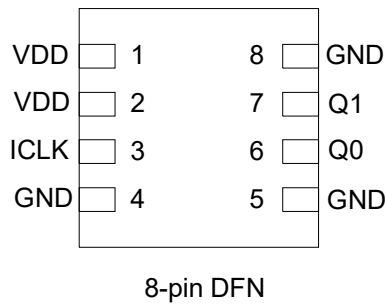
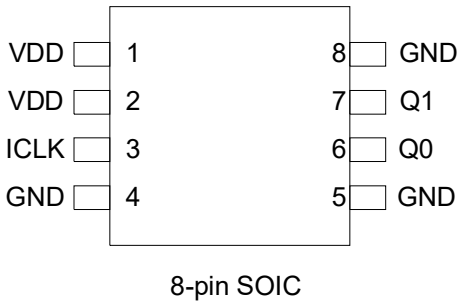
Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-pin SOIC and 8-pin DFN, Pb-free
- Input/Output clock frequency up to 200 MHz
- Low power CMOS technology
- Operating voltages of 1.8V to 3.3V
- Extended temperature range (-40° to +105°C)

Block Diagram



Pin Assignments



Pin Descriptions

| Pin Number ¹ | Pin Name | Pin Type | Pin Description |
|-------------------------|----------|----------|--------------------------------------|
| 1 | VDD | Power | Connect to +1.8V, +2.5 V, or +3.3 V. |
| 2 | VDD | Power | Connect to +1.8V, +2.5 V, or +3.3 V. |
| 3 | ICLK | Input | Clock input. |
| 4 | GND | Power | Connect to ground. |
| 5 | GND | Power | Connect to ground. |
| 6 | Q0 | Output | Clock output 0. |
| 7 | Q1 | Output | Clock output 1. |
| 8 | GND | Power | Connect to ground. |

1. VDD on pin 1 and 2 is the same internal signal and must be connected to the same power rail on the PCB.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μF should be connected between VDD pin and GND pin, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 74FCT38072S is capable of, careful attention must be paid to board layout. Essentially, both outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 74FCT38072S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 3.465V |
| Outputs | -0.5 V to VDD+0.5 V |
| ICLK | 3.465V |
| Ambient Operating Temperature (extended) | -40 to +105°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|--------|-------|
| Ambient Operating Temperature (extended) | -40 | | +105 | °C |
| Power Supply Voltage (measured in respect to GND) | +1.71 | | +3.465 | V |

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 1.71 | | 1.89 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | VDD | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -10 mA | 1.3 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 10mA | | | 0.35 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 15 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | ICLK | | 5 | | pF |

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 2.375 | | 2.625 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | VDD | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -16 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 16 mA | | | 0.5 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 18 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | ICLK | | 5 | | pF |

VDD=3.3 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 3.15 | | 3.45 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | VDD | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.2 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.7 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 22 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | ICLK | | 5 | | pF |

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.36 to 1.44 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 1.44 to 0.36 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | Note 1 | 1.5 | 2.5 | 4 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz-20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 200 | ps |

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.5 to 2.0 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.5 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | Note 1 | 1.8 | 2.5 | 4.5 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz-20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 200 | ps |

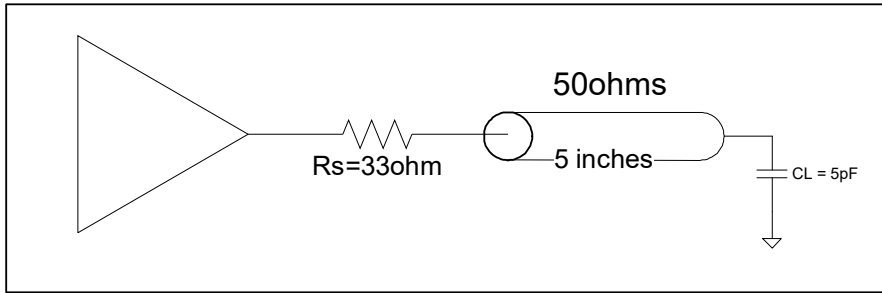
VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.66 to 2.64 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.64 to 0.66 V, C _L =5 pF | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | Note 1 | 1.5 | 2.5 | 4 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration Range: 12kHz-20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 200 | ps |

Notes:

1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult Renesas for tight duty cycle clock generators.

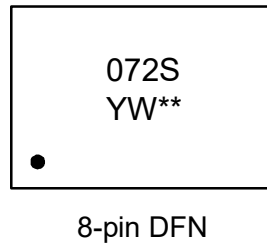
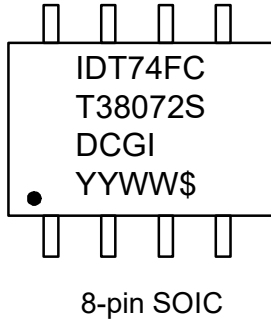
Test Load and Circuit



Thermal Characteristics (8SOIC)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|----------------------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 1 m/s air flow | | 140 | | $^{\circ}\text{C/W}$ |
| | θ_{JA} | 3 m/s air flow | | 120 | | $^{\circ}\text{C/W}$ |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | $^{\circ}\text{C/W}$ |

Marking Diagrams



Notes:

1. “**” is the lot number.
2. “YYWW” or “YW” are the last digits of the year and week that the part was assembled.
3. “G” denotes RoHS compliant package.
4. “\$” denotes the mark code.
5. “I” denotes extended temperature range device.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/8-soic-package-outline-drawing-0150-body-width-0050-pitch-dcg8d1

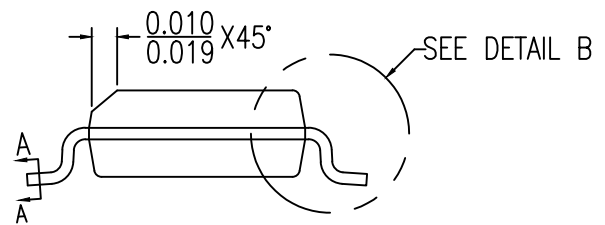
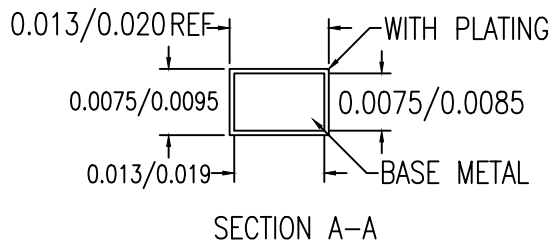
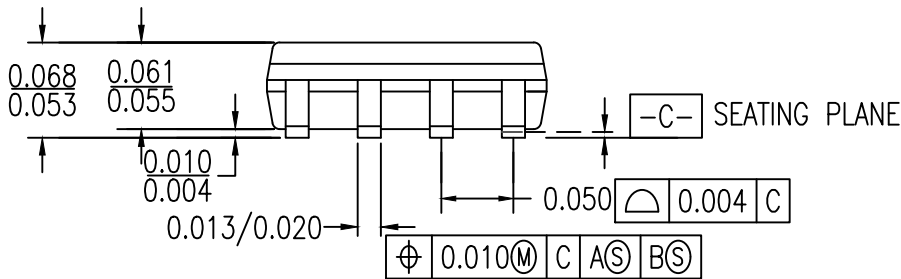
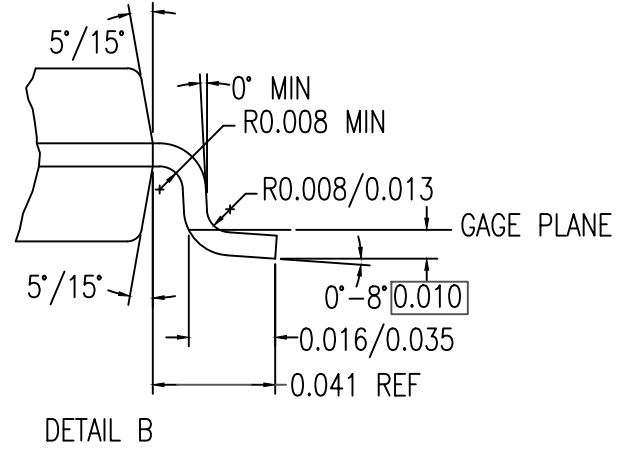
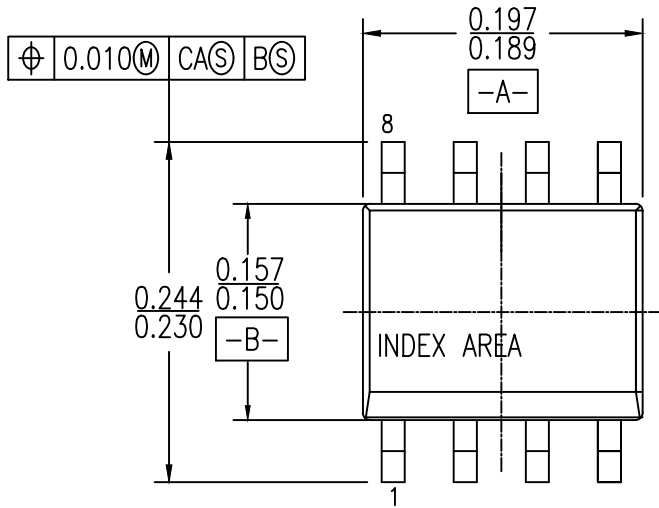
Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|------------|----------------|
| 74FCT38072SDCGI | see page 6 | Tubes | 8-pin SOIC | -40 to +105 °C |
| 74FCT38072SDCGI8 | | Tape and Reel | 8-pin SOIC | -40 to +105 °C |
| 74FCT38072SCMGI | | Cut Tape | 8-pin DFN | -40 to +105 °C |
| 74FCT38072SCMGI8 | | Tape and Reel | 8-pin DFN | -40 to +105 °C |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

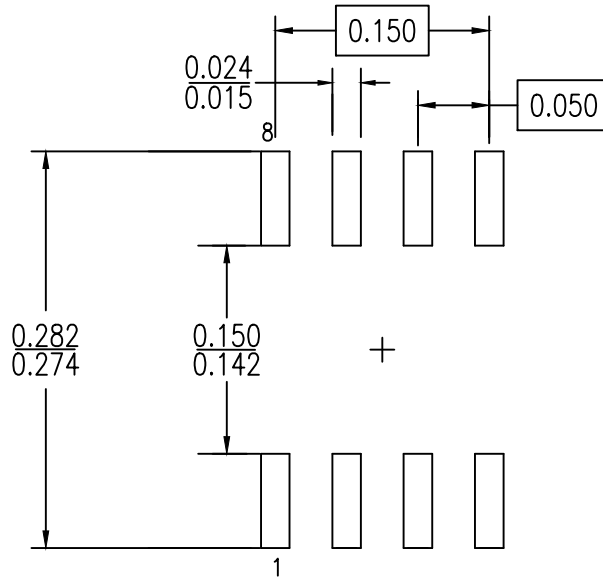
Revision History

| Revision Date | Description of Change |
|----------------|---|
| May 4, 2020 | <ul style="list-style-type: none"> Added a footnote to Pin Descriptions Updated the Package Outline Drawings; however, no technical changes were made |
| March 18, 2015 | Initial release. |



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES

| Package Revision History | | |
|--------------------------|---------|-------------------------------|
| Date Created | Rev No. | Description |
| July 27, 2018 | Rev 01 | Dedicate to Package DCG8 Only |
| Feb 24, 2016 | Rev 00 | Initial Release |