

74HC75

Quad bistable transparent latch

Rev. 5 — 17 March 2021

Product data sheet

1. General description

The 74HC75 is a quad bistable transparent latch with complementary outputs. Two latches are simultaneously controlled by one of two active HIGH enable inputs (LE12 and LE34). When LEnn is HIGH, the data enters the latches and appears at the nQ outputs. The nQ outputs follow the data inputs (nD) as long as LEnn is HIGH (transparent). The data on the nD inputs one set-up time prior to the HIGH-to-LOW transition of the LEnn will be stored in the latches. The latched outputs remain stable as long as the LEnn is LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Complementary Q and \bar{Q} outputs
- V_{CC} and GND on the center pins
- CMOS input levels
- ESD protection:
 - HBM EIA/JESD22-A114F exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC75D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74HC75PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

4. Functional diagram

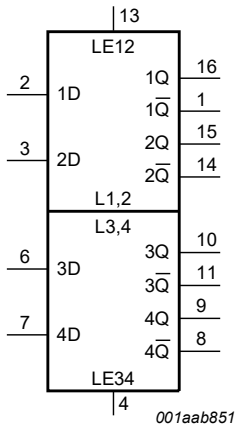


Fig. 1. Logic symbol

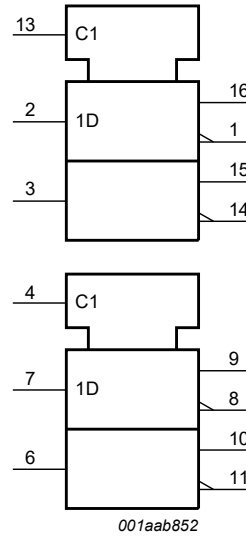


Fig. 2. IEC logic symbol

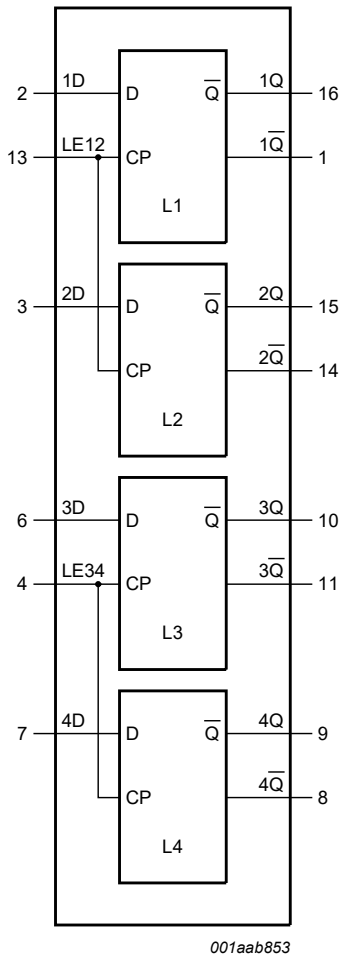


Fig. 3. Functional diagram

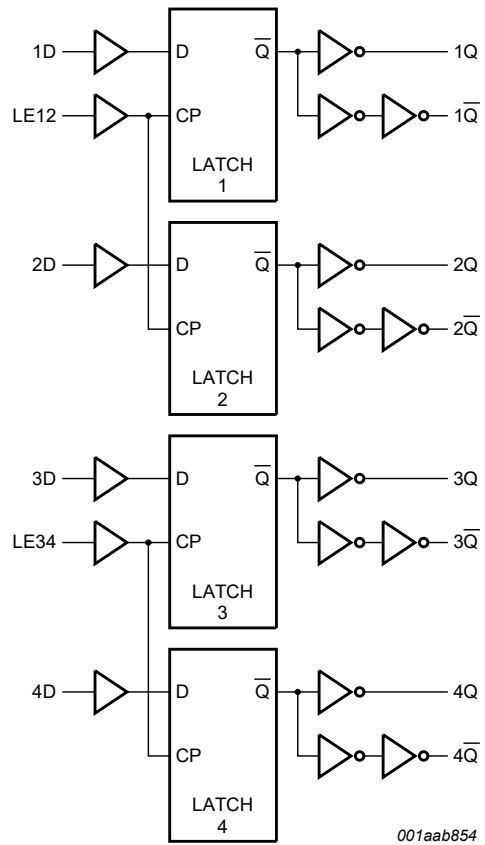


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

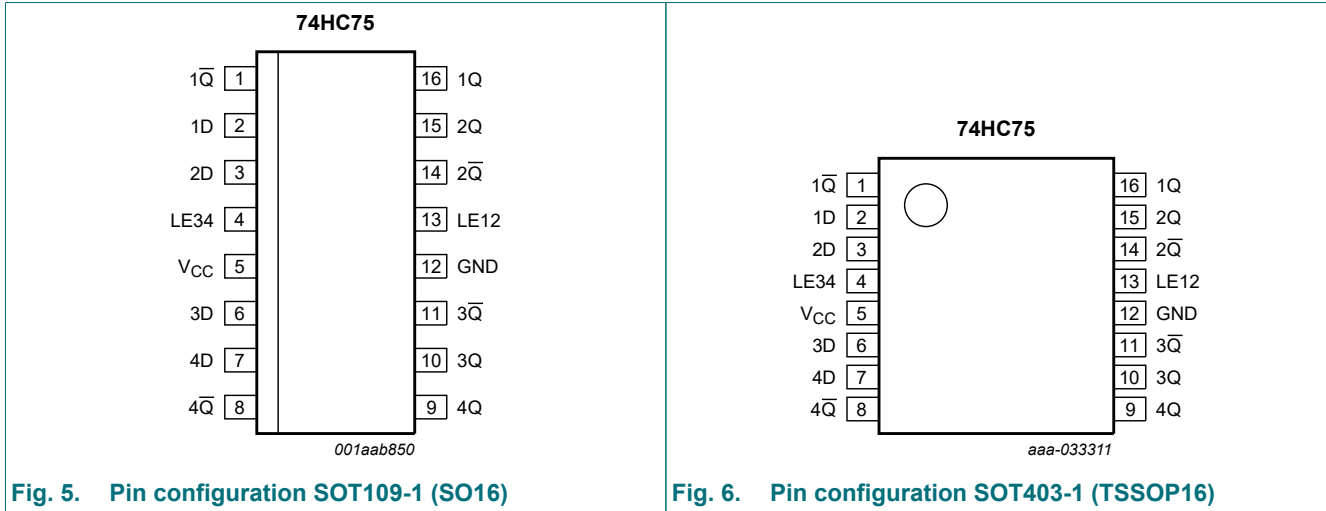


Fig. 5. Pin configuration SOT109-1 (SO16)

Fig. 6. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|---------------|--|
| 1Q, 2Q, 3Q, 4Q | 1, 14, 11, 8 | complementary latch output |
| 1D, 2D, 3D, 4D | 2, 3, 6, 7 | data input |
| LE34 | 4 | latch enable input for latches 3 and 4 (active HIGH) |
| V _{CC} | 5 | positive supply voltage |
| GND | 12 | ground (0 V) |
| LE12 | 13 | latch enable input for latches 1 and 2 (active HIGH) |
| 1Q, 2Q, 3Q, 4Q | 16, 15, 10, 9 | latch output |

6. Function description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW LEnn transition.

| Operating mode | Input | | Output | |
|----------------|-------|----|--------|-----|
| | LEnn | nD | nQ | nQ̄ |
| Data enabled | H | L | L | H |
| | H | H | H | L |
| Data latched | L | X | q | q̄ |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1] | - | ± 20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ | - | ± 25 | mA |
| I_{CC} | supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------------------|-----|------|----------|------|
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|--------------------------|-------------------------|------|-----|------|------|
| $T_{amb} = 25\text{ °C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0\text{ V}$ | 1.5 | 1.2 | - | V |
| | | $V_{CC} = 4.5\text{ V}$ | 3.15 | 2.4 | - | V |
| | | $V_{CC} = 6.0\text{ V}$ | 4.2 | 3.2 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0\text{ V}$ | - | 0.8 | 0.5 | V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 2.1 | 1.35 | V |
| | | $V_{CC} = 6.0\text{ V}$ | - | 2.8 | 1.8 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------|---|------|------|------|------|
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 µA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | V |
| | | I _O = -20 µA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | V |
| | | I _O = -20 µA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | V |
| | | I _O = -4 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.48 | 5.81 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 µA; V _{CC} = 2.0 V | - | 0 | 0.1 | V |
| | | I _O = 20 µA; V _{CC} = 4.5 V | - | 0 | 0.1 | V |
| | | I _O = 20 µA; V _{CC} = 6.0 V | - | 0 | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | µA |
| C _I | input capacitance | | - | 3.5 | - | pF |
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -20 µA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 µA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 µA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 4.5 V | 3.84 | - | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.34 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 20 µA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 µA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 µA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 4.5 V | - | - | 0.33 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | - | 0.33 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 80 | µA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|------|-----|------|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | V |
| | | V _{CC} = 4.5 V | 3.15 | - | - | V |
| | | V _{CC} = 6.0 V | 4.2 | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | - | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | - | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 4.5 V | 3.7 | - | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.2 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | - | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 4.5 V | - | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 160 | μA |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; unless otherwise specified, for test circuit see [Fig. 11](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------------------|---|-----|-----|-----|------|
| $T_{\text{amb}} = 25\text{ °C}$ | | | | | | |
| t_{pd} | propagation delay | nD to nQ; see Fig. 7 [1] | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | - | 33 | 110 | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | - | 12 | 22 | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | - | 10 | 19 | ns |
| | | $V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$ | - | 11 | - | ns |
| | | nD to n \bar{Q} ; see Fig. 8 [1] | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | - | 39 | 120 | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | - | 14 | 24 | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | - | 11 | 20 | ns |
| | | $V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$ | - | 11 | - | ns |
| | | LEnn to nQ; see Fig. 10 [1] | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | - | 33 | 120 | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | - | 12 | 24 | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | - | 10 | 20 | ns |
| | | $V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$ | - | 11 | - | ns |
| | | LEnn to n \bar{Q} ; see Fig. 10 [1] | | | | |
| $V_{\text{CC}} = 2.0\text{ V}$ | - | 39 | 125 | ns | | |
| $V_{\text{CC}} = 4.5\text{ V}$ | - | 14 | 25 | ns | | |
| $V_{\text{CC}} = 6.0\text{ V}$ | - | 11 | 21 | ns | | |
| $V_{\text{CC}} = 5.0\text{ V}$; $C_L = 15\text{ pF}$ | - | 11 | - | ns | | |
| t_t | transition time | nQ, n \bar{Q} ; see Fig. 7 and Fig. 8 [2] | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | - | 19 | 75 | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | - | 7 | 15 | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | - | 6 | 13 | ns |
| t_{W} | pulse width | LEnn HIGH; see Fig. 10 | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | 80 | 17 | - | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | 16 | 6 | - | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | 14 | 5 | - | ns |
| t_{su} | set-up time | nD to LEnn; see Fig. 9 | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | 60 | 14 | - | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | 12 | 5 | - | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | 10 | 4 | - | ns |
| t_h | hold time | nD to LEnn; see Fig. 9 | | | | |
| | | $V_{\text{CC}} = 2.0\text{ V}$ | 3 | -8 | - | ns |
| | | $V_{\text{CC}} = 4.5\text{ V}$ | 3 | -3 | - | ns |
| | | $V_{\text{CC}} = 6.0\text{ V}$ | 3 | -2 | - | ns |
| C_{PD} | power dissipation capacitance | per latch; $V_I = GND$ to V_{CC} [3] | - | 42 | - | pF |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------|--|-----|-----|-----|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| t _{pd} | propagation delay | nD to nQ; see Fig. 7 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 140 | ns |
| | | V _{CC} = 4.5 V | - | - | 28 | ns |
| | | V _{CC} = 6.0 V | - | - | 24 | ns |
| | | nD to nQ̄; see Fig. 8 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 150 | ns |
| | | V _{CC} = 4.5 V | - | - | 30 | ns |
| | | V _{CC} = 6.0 V | - | - | 26 | ns |
| | | LEnn to nQ; see Fig. 10 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 150 | ns |
| | | V _{CC} = 4.5 V | - | - | 30 | ns |
| | | V _{CC} = 6.0 V | - | - | 26 | ns |
| | | LEnn to nQ̄; see Fig. 10 [1] | | | | |
| V _{CC} = 2.0 V | - | - | 155 | ns | | |
| V _{CC} = 4.5 V | - | - | 31 | ns | | |
| V _{CC} = 6.0 V | - | - | 26 | ns | | |
| t _t | transition time | nQ, nQ̄; see Fig. 7 and Fig. 8 [2] | | | | |
| | | V _{CC} = 2.0 V | - | - | 95 | ns |
| | | V _{CC} = 4.5 V | - | - | 19 | ns |
| | | V _{CC} = 6.0 V | - | - | 16 | ns |
| t _w | pulse width | LEnn HIGH; see Fig. 10 | | | | |
| | | V _{CC} = 2.0 V | 100 | - | - | ns |
| | | V _{CC} = 4.5 V | 20 | - | - | ns |
| | | V _{CC} = 6.0 V | 17 | - | - | ns |
| t _{su} | set-up time | nD to LEnn; see Fig. 9 | | | | |
| | | V _{CC} = 2.0 V | 75 | - | - | ns |
| | | V _{CC} = 4.5 V | 15 | - | - | ns |
| | | V _{CC} = 6.0 V | 13 | - | - | ns |
| t _h | hold time | nD to LEnn; see Fig. 9 | | | | |
| | | V _{CC} = 2.0 V | 3 | - | - | ns |
| | | V _{CC} = 4.5 V | 3 | - | - | ns |
| | | V _{CC} = 6.0 V | 3 | - | - | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-------------------|--|-----|-----|-----|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| t _{pd} | propagation delay | nD to nQ; see Fig. 7 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 165 | ns |
| | | V _{CC} = 4.5 V | - | - | 33 | ns |
| | | V _{CC} = 6.0 V | - | - | 28 | ns |
| | | nD to nQ̄; see Fig. 8 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 180 | ns |
| | | V _{CC} = 4.5 V | - | - | 36 | ns |
| | | V _{CC} = 6.0 V | - | - | 31 | ns |
| | | LEnn to nQ; see Fig. 10 [1] | | | | |
| | | V _{CC} = 2.0 V | - | - | 180 | ns |
| | | V _{CC} = 4.5 V | - | - | 36 | ns |
| | | V _{CC} = 6.0 V | - | - | 31 | ns |
| t _t | transition time | nQ, nQ̄; see Fig. 7 and Fig. 8 [2] | | | | |
| | | V _{CC} = 2.0 V | - | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | - | 19 | ns |
| t _w | pulse width | LEnn HIGH; see Fig. 10 | | | | |
| | | V _{CC} = 2.0 V | 120 | - | - | ns |
| | | V _{CC} = 4.5 V | 24 | - | - | ns |
| t _{su} | set-up time | nD to LEnn; see Fig. 9 | | | | |
| | | V _{CC} = 2.0 V | 90 | - | - | ns |
| | | V _{CC} = 4.5 V | 18 | - | - | ns |
| t _h | hold time | nD to LEnn; see Fig. 9 | | | | |
| | | V _{CC} = 2.0 V | 3 | - | - | ns |
| | | V _{CC} = 4.5 V | 3 | - | - | ns |
| | | V _{CC} = 6.0 V | 3 | - | - | ns |

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

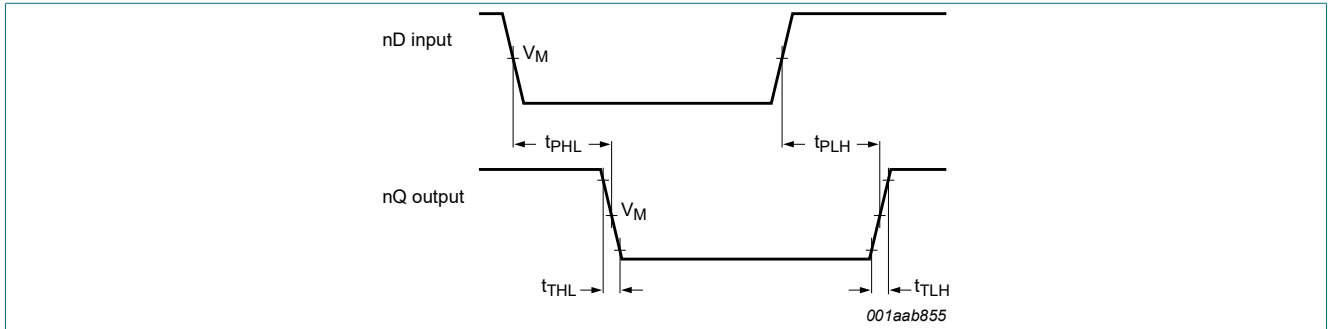
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

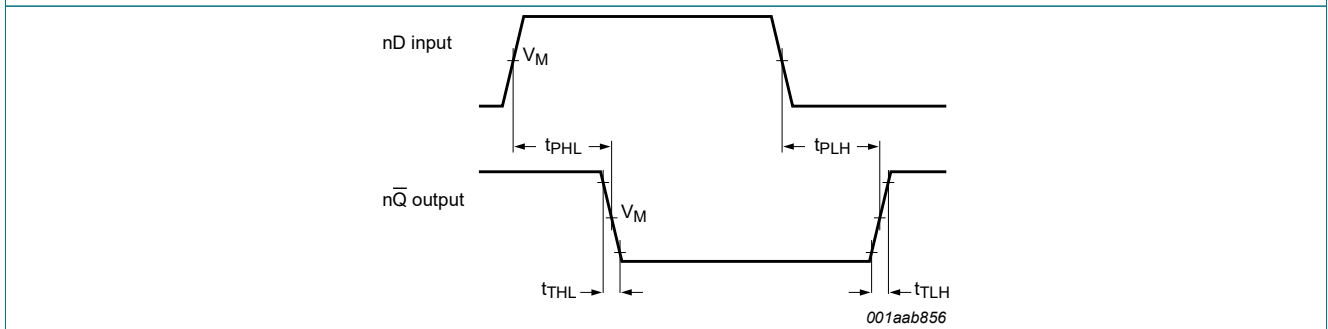
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



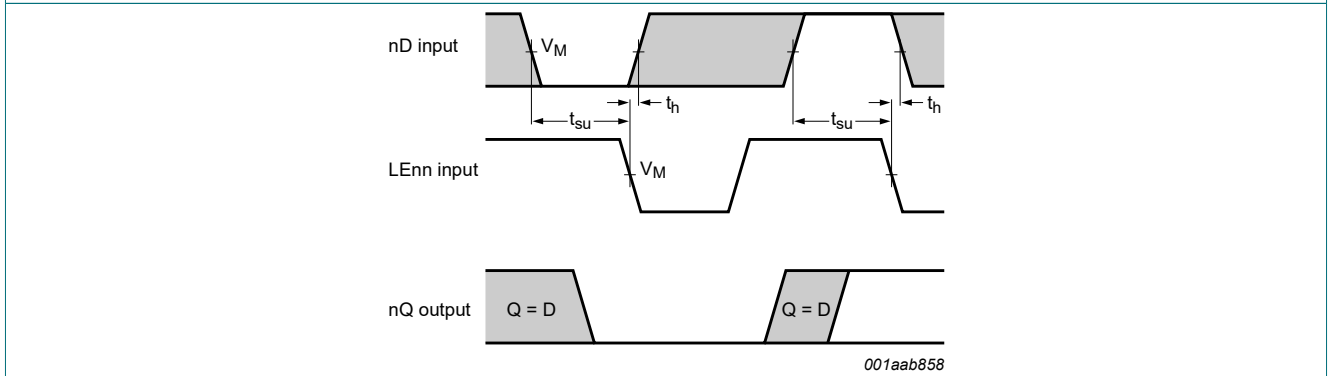
$V_M = 0.5 \times V_I$

Fig. 7. Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times



$V_M = 0.5 \times V_I$

Fig. 8. Waveforms showing the data input (nD) to output (nQ) propagation delays and the output transition times



The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 0.5 \times V_I$

Fig. 9. Waveforms showing the data set-up and hold times for nD input to LEnn input

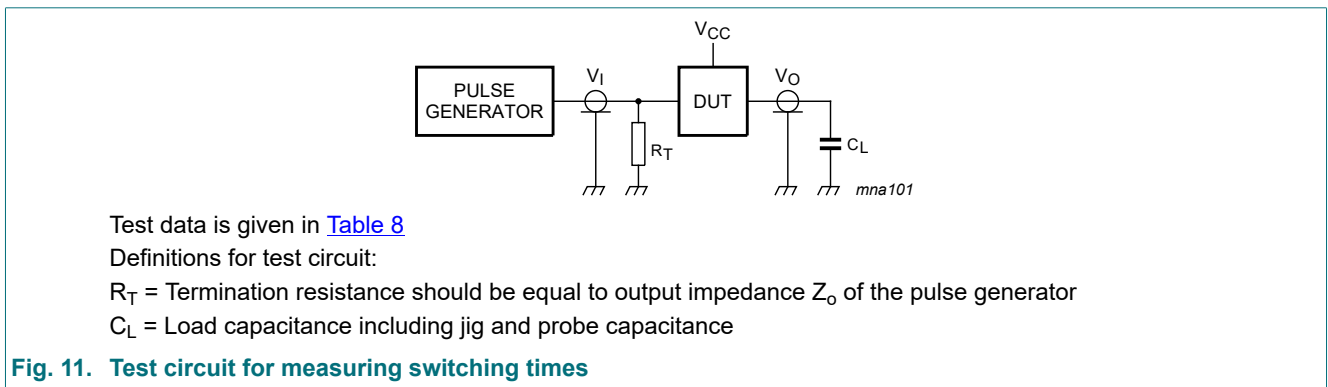
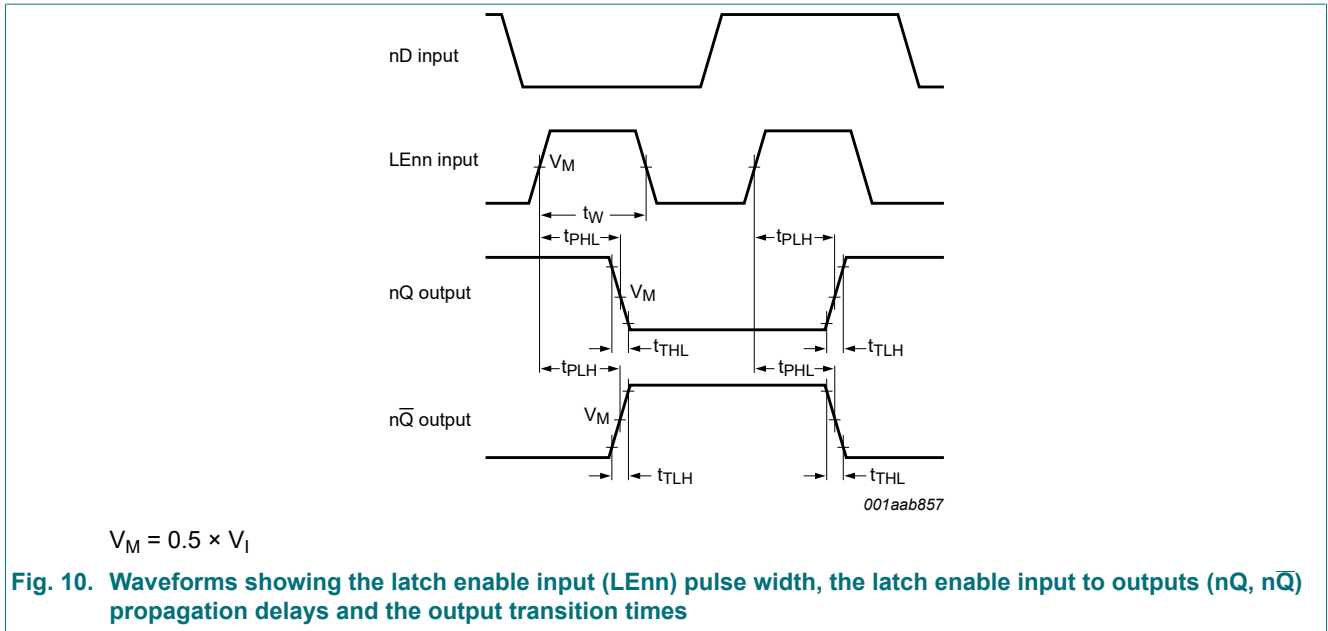


Table 8. Test data

| Supply | Input | Load |
|----------|----------|-------|
| V_{CC} | V_I | C_L |
| 2.0 V | V_{CC} | 50 pF |
| 4.5 V | V_{CC} | 50 pF |
| 6.0 V | V_{CC} | 50 pF |
| 5.0 V | V_{CC} | 15 pF |

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

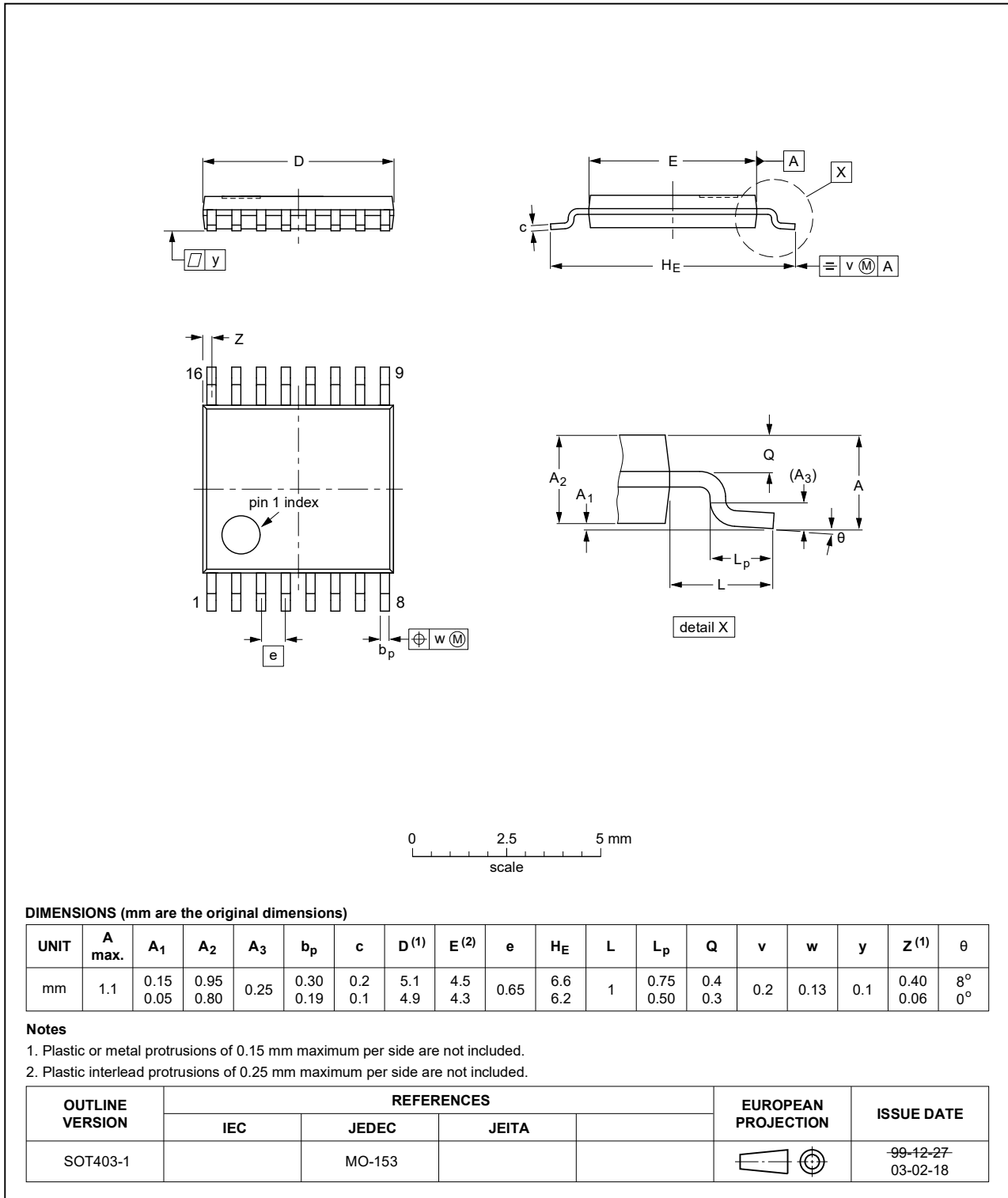


Fig. 13. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 9. Abbreviations

| Acronym | Abbreviation |
|---------|--|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |

13. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|---|-----------------------|---------------|--------------------|
| 74HC75 v.5 | 20210317 | Product data sheet | - | 74HC75 v.4 |
| Modifications: | <ul style="list-style-type: none"> • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74HC75DB (SOT338-1 / SSOP16) removed. | | | |
| 74HC75 v.4 | 20160224 | Product data sheet | - | 74HC75 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Type number 74HC75N (SOT38-4) removed. | | | |
| 74HC75 v.3 | 20041112 | Product data sheet | - | 74HC_HCT75_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT75. • Inserted family specification. | | | |
| 74HC_HCT75_CNV v.2 | 19970918 | Product specification | - | 74HC_HCT75 v.1 |
| 74HC_HCT75 v.1 | 19901201 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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