

74HC393; 74HCT393

Dual 4-bit binary ripple counter

Rev. 8 — 22 October 2021

Product data sheet

1. General description

The 74HC393; 74HCT393 is a dual 4-stage binary ripple counter. Each counter features a clock input (\overline{nCP}), an overriding asynchronous master reset input (\overline{nMR}) and 4 buffered parallel outputs ($\overline{nQ0}$ to $\overline{nQ3}$). The counter advances on the HIGH-to-LOW transition of \overline{nCP} . A HIGH on \overline{nMR} clears the counter stages and forces the outputs LOW, independent of the state of \overline{nCP} . Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC393: CMOS level
 - For 74HCT393: TTL level
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V.
- Two 4-bit binary counters with individual clocks
- Divide by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC393D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT393D				
74HC393PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT393PW				
74HC393BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT393BQ				

4. Functional diagram

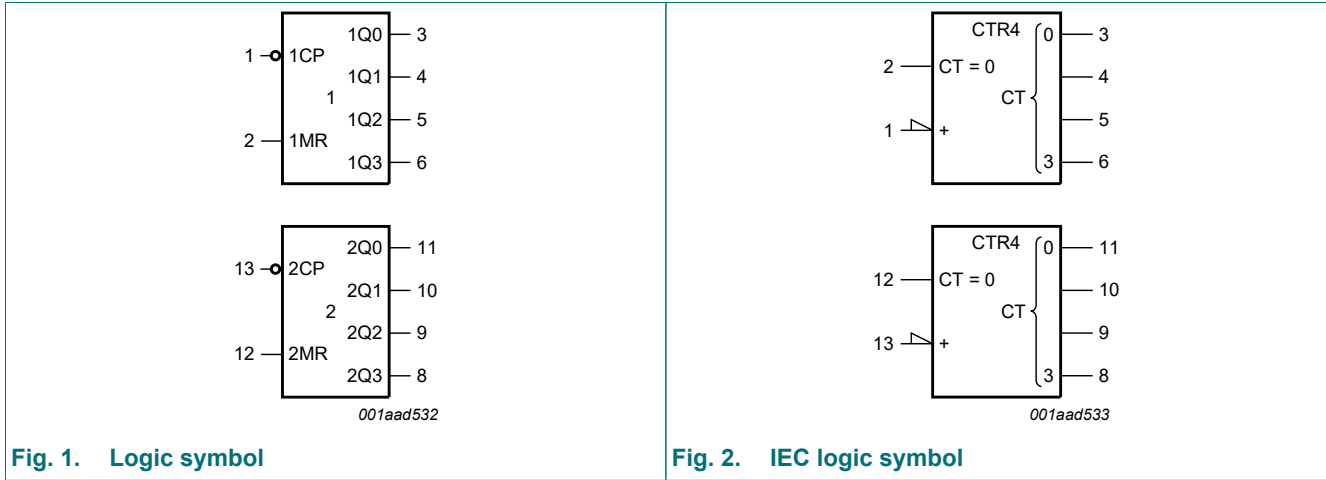


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

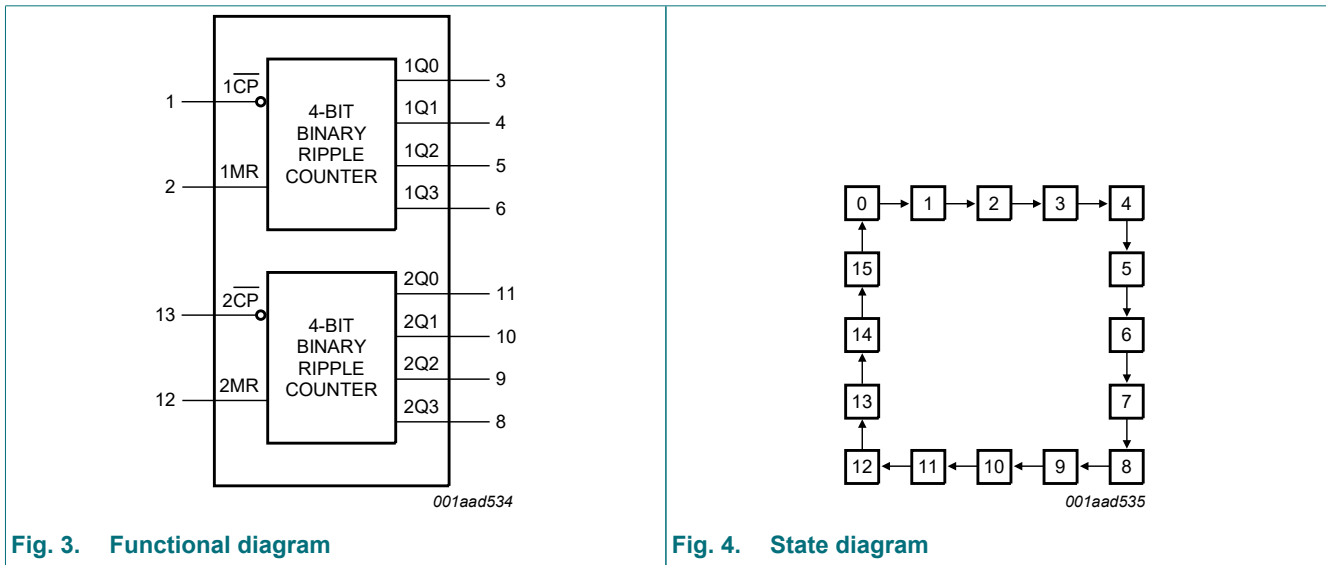


Fig. 3. Functional diagram

Fig. 4. State diagram

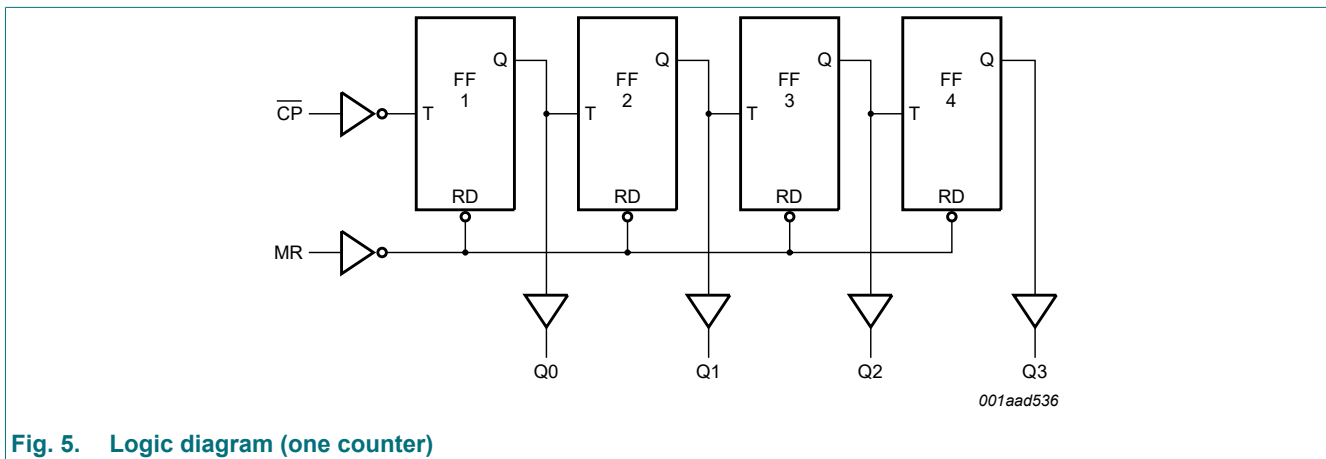
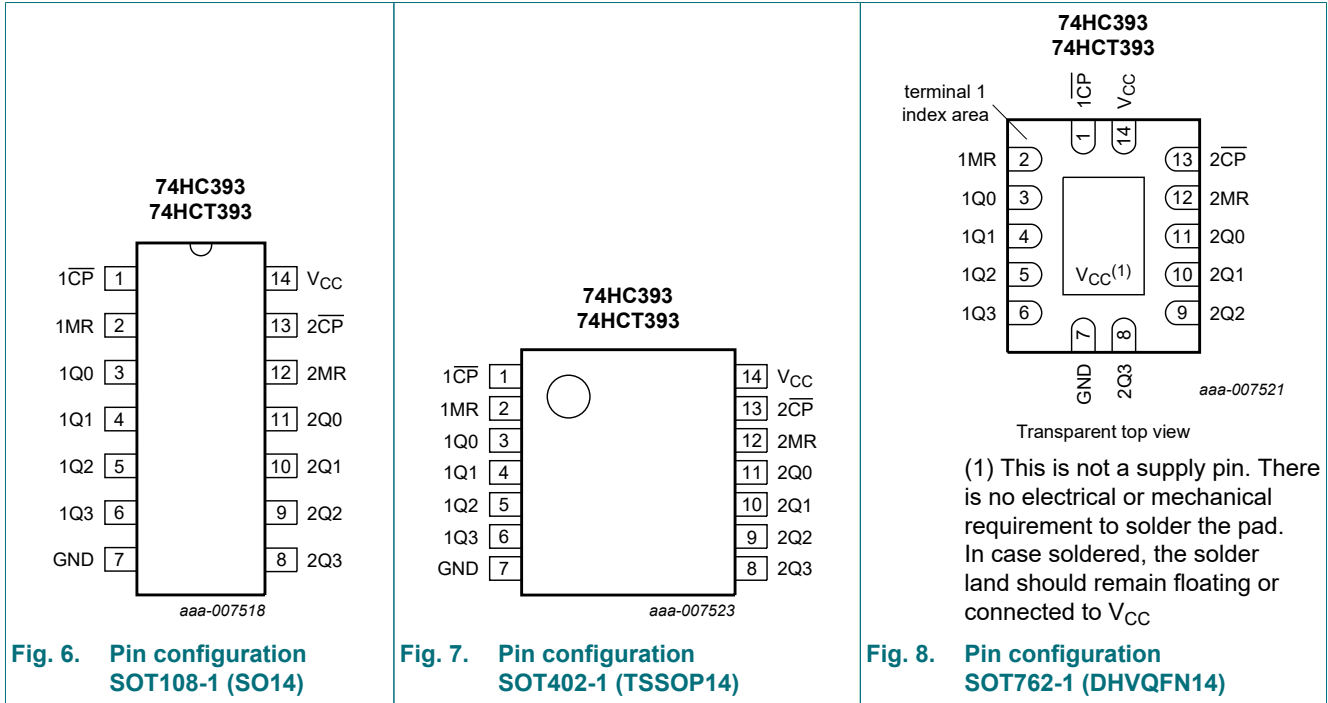


Fig. 5. Logic diagram (one counter)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP	1	clock input (HIGH-to-LOW, edge-triggered)
1MR	2	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 4, 5, 6	flip-flop output
GND	7	ground (0 V)
2Q3, 2Q2, 2Q1, 2Q0	8, 9, 10, 11	flip-flop output
2MR	12	asynchronous master reset input (active HIGH)
2CP	13	clock input (HIGH-to-LOW, edge-triggered)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Count sequence for one counter

H = HIGH voltage level; L = LOW voltage level.

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	± 50	mA
I_{GND}	ground current		-	± 50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

- [1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
 For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
 For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC393			74HCT393			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC393										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
		$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	pF	

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT393										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; nCP	-	40	144	-	180	-	196	µA
		per input pin; nMR	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 11.

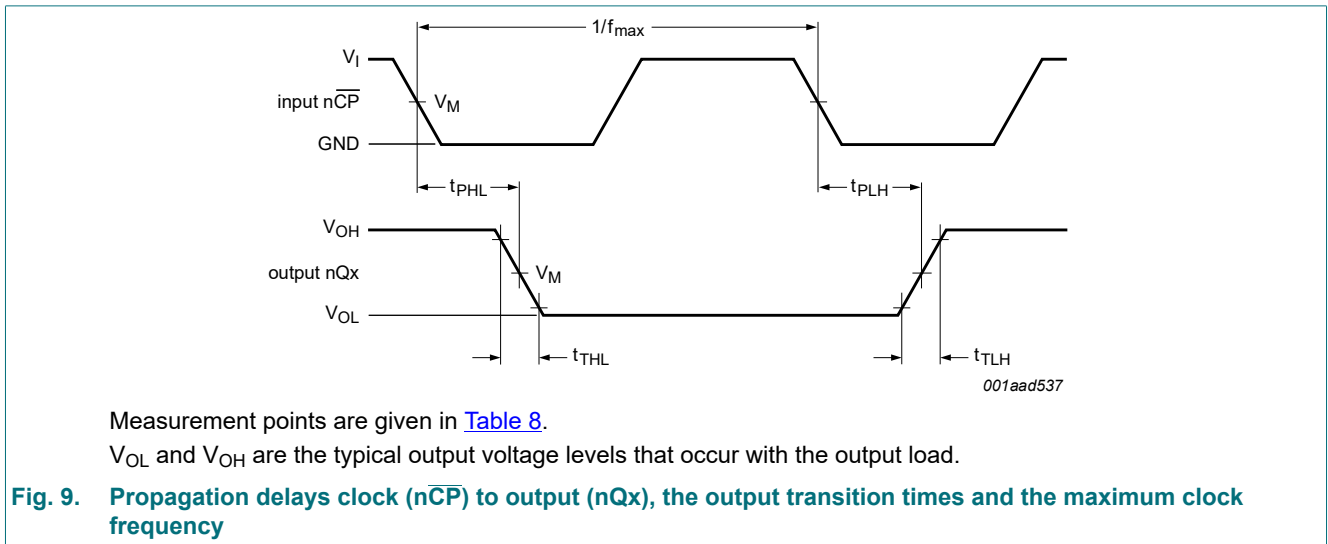
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC393										
t _{pd}	propagation delay	nCP to nQ0; see Fig. 9 [1]								
		V _{CC} = 2.0 V	-	41	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	21	-	26	-	32	ns
		nQx to nQ(x+1); see Fig. 9 [1]								
		V _{CC} = 2.0 V	-	14	45	-	55	-	70	ns
		V _{CC} = 4.5 V	-	5	9	-	11	-	14	ns
		V _{CC} = 5 V; C _L = 15 pF	-	5	-	-	-	-	ns	
		V _{CC} = 6.0 V	-	4	8	-	9	-	12	ns

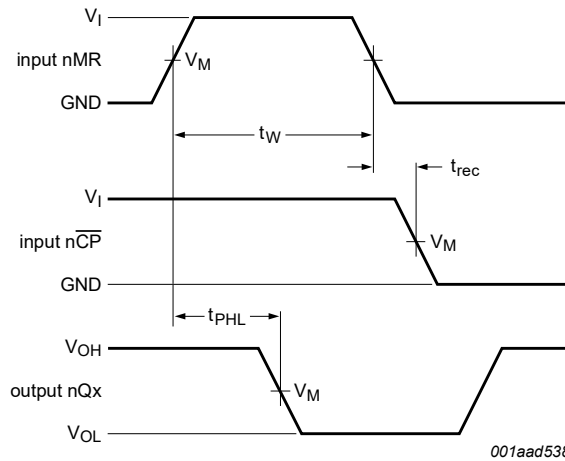
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	nMR to nQx; see Fig. 10								
		V _{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V _{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V _{CC} = 5 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t _t	transition time	Qn; see Fig. 9 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	nCP HIGH or LOW; see Fig. 9								
		V _{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		nMR HIGH; see Fig. 10								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{rec}	recovery time	nMR to nCP; see Fig. 10								
		V _{CC} = 2.0 V	5	3	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	1	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	1	-	5	-	5	-	ns
f _{clk(max)}	maximum clock frequency	see Fig. 9								
		V _{CC} = 2.0 V	6	30	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	90	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	99	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	23	-	-	-	-	-	pF
74HCT393										
t _{pd}	propagation delay	nCP to nQ0; see Fig. 9 [1]								
		V _{CC} = 4.5 V	-	15	25	-	31	-	38	ns
		V _{CC} = 5 V; C _L = 15 pF	-	20	-	-	-	-	-	ns
		nQx to nQ(x+1); see Fig. 9 [1]								
		V _{CC} = 4.5 V	-	6	10	-	13	-	15	ns
t _{PHL}	HIGH to LOW propagation delay	V _{CC} = 4.5 V	-	18	32	-	40	-	48	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _t	transition time	Qn; see Fig. 9 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _W	pulse width	nCP HIGH or LOW; see Fig. 9								
		V _{CC} = 4.5 V	19	11	-	24	-	29	-	ns
t _{rec}	recovery time	nMR HIGH; see Fig. 10								
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
f _{clk(max)}	maximum clock frequency	see Fig. 9								
		V _{CC} = 4.5 V	27	48	-	22	-	18	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	53	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [3]	-	25	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.

10.1. Waveforms





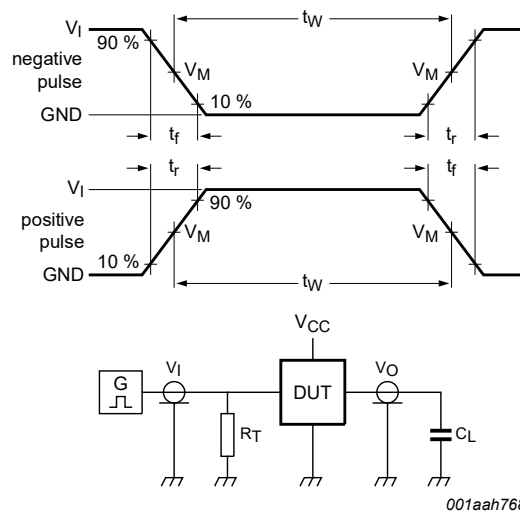
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 10. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)

Table 8. Measurement points

Type	Input		Output
	V_M	V_M	V_M
74HC393	$0.5V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT393	1.3 V	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_i	t_r, t_f	C_L	
74HC393	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT393	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

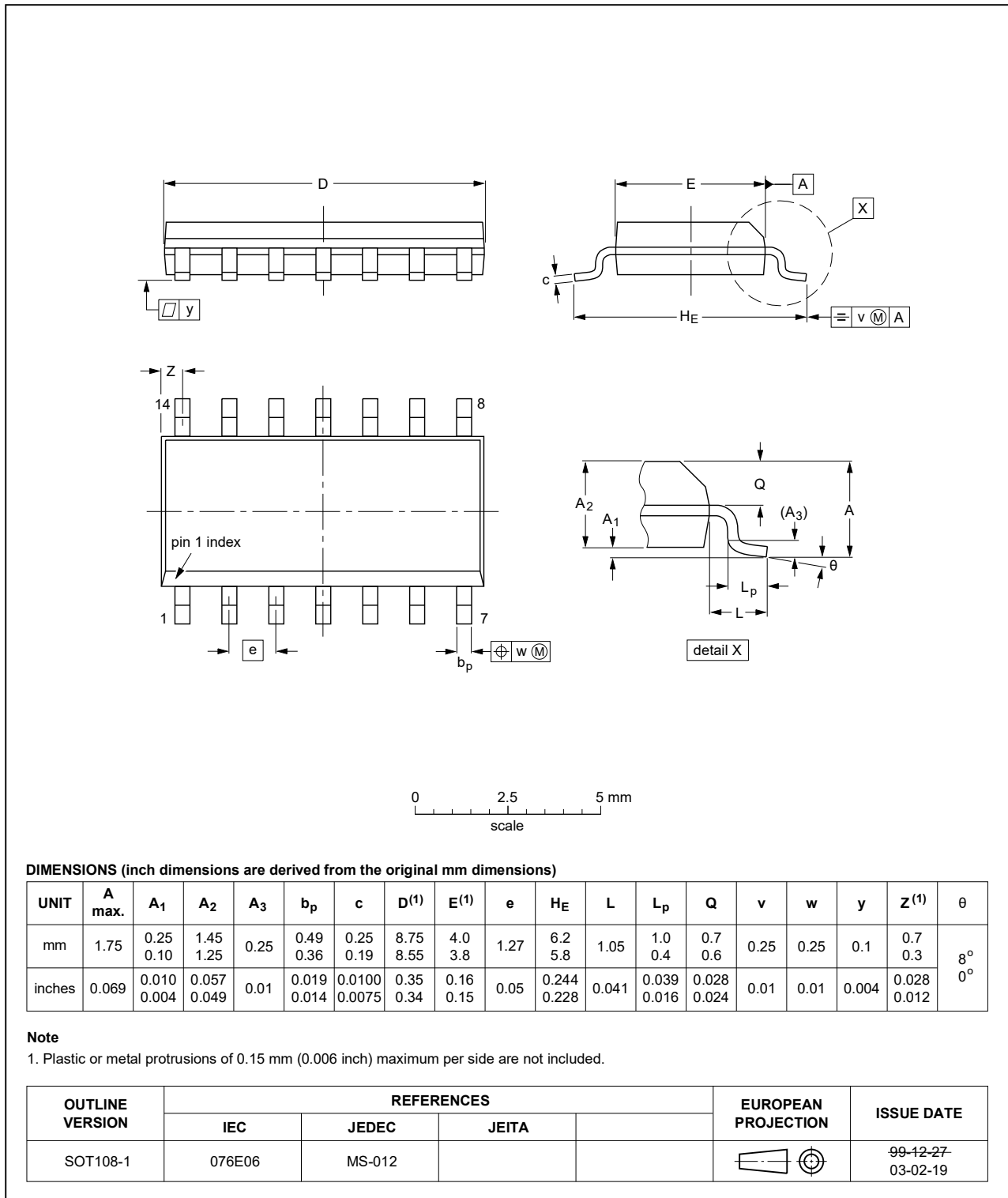


Fig. 12. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

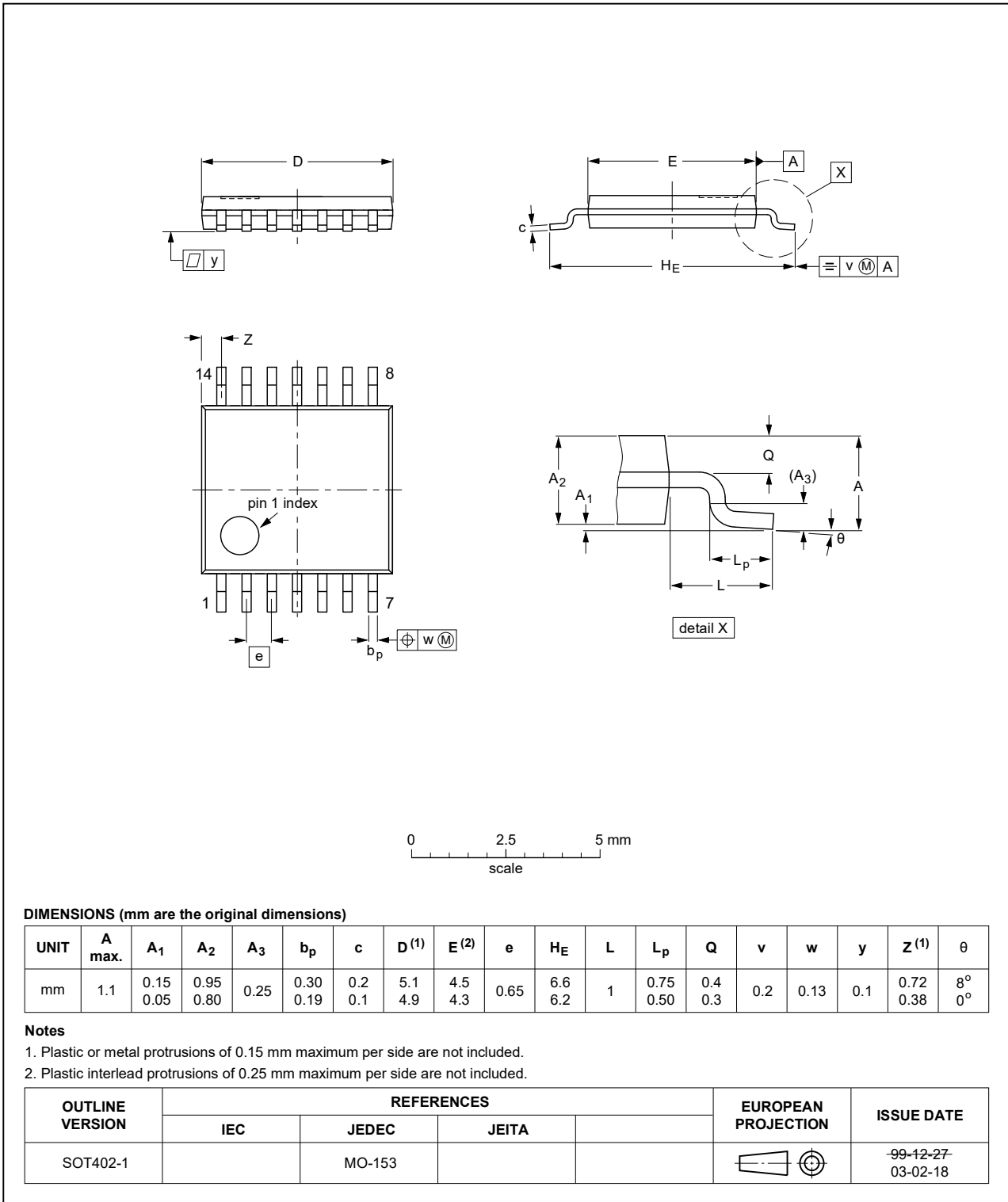


Fig. 13. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

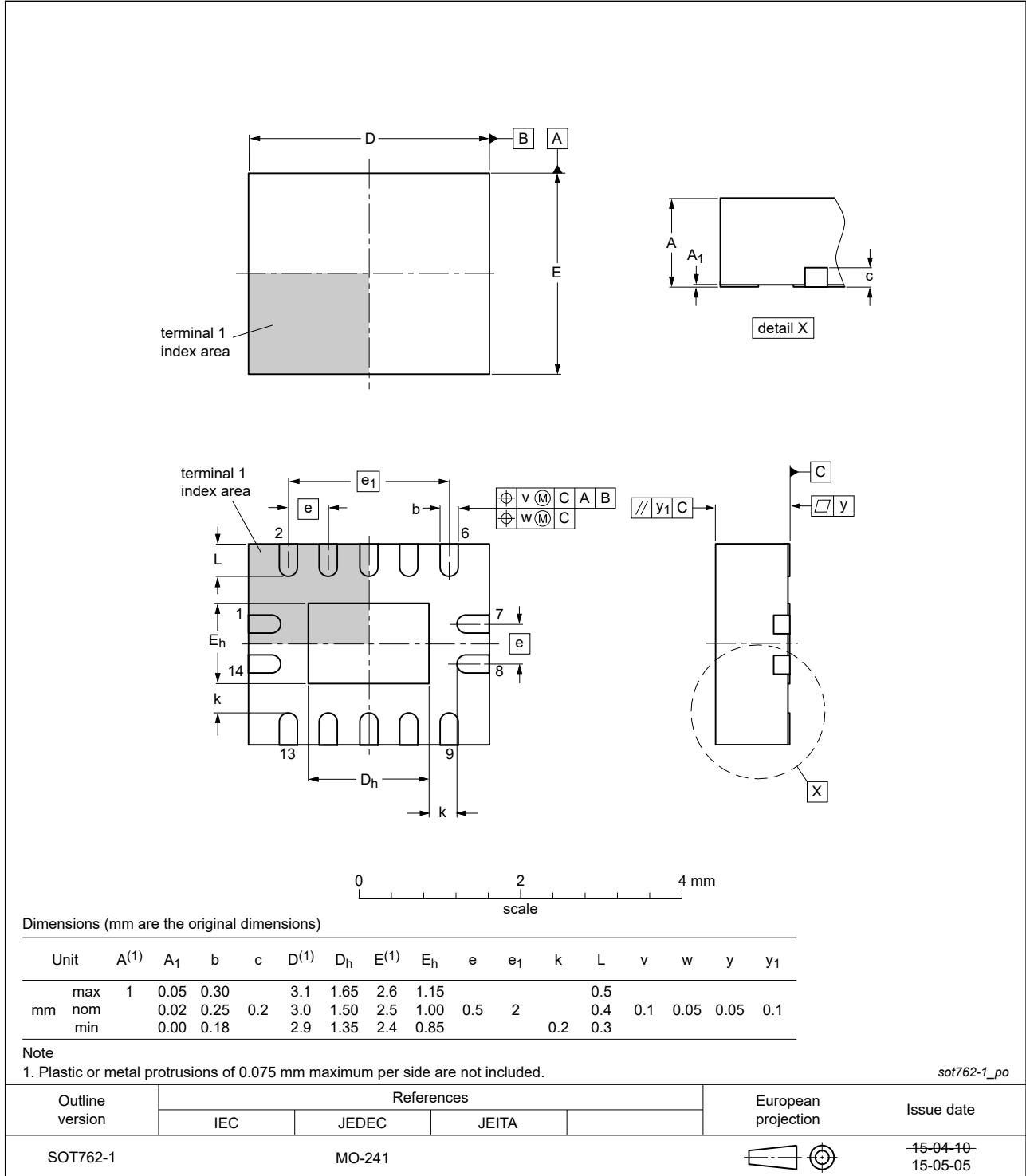


Fig. 14. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT393 v.8	20211022	Product data sheet	-	74HC_HCT393 v.7.1
Modifications:	<ul style="list-style-type: none"> Table 6: V_{OH} and V_{OL} conditions for 74HCT393 corrected. (Errata) 			
74HC_HCT393 v.7.1	20201021	Product data sheet	-	74HC_HCT393 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74HC393DB and 74HCT393DB (SOT337-1/SSOP14) removed. Section 1 (Errata) and Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. v.7.1: Table 6: Values input leakage current for 74HC393 aligned with 74HCT393. (Errata) 			
74HC_HCT393 v.6	20151203	Product data sheet	-	74HC_HCT393 v.5
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC393N and 74HCT393N (SOT27-1) removed. 			
74HC_HCT393 v.5	20140401	Product data sheet	-	74HC_HCT393 v.4
Modifications:	<ul style="list-style-type: none"> Table 7: The conditions for C_{PD} have been corrected (errata). 			
74HC_HCT393 v.4	20130516	Product data sheet	-	74HC_HCT393 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT393 v.3	20050906	Product data sheet	-	74HC_HCT393_CNV v.2
74HC_HCT393_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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