

74HC597-Q100; 74HCT597-Q100

8-bit shift register with input flip-flops

Rev. 1 — 26 May 2014

Product data sheet

1. General description

The 74HC597-Q100; 74HCT597-Q100 is an 8-bit shift register with input flip-flops. It consists of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to $+85\text{ °C}$ and from -40 °C to $+125\text{ °C}$
- Complies with JEDEC standard JESD7A
- Input levels:
 - ◆ For 74HC597-Q100: CMOS level
 - ◆ For 74HCT597-Q100: TTL level
- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\ \Omega$)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC597D-Q100	-40 °C to $+125\text{ °C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT597D-Q100				
74HC597PW-Q100	-40 °C to $+125\text{ °C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

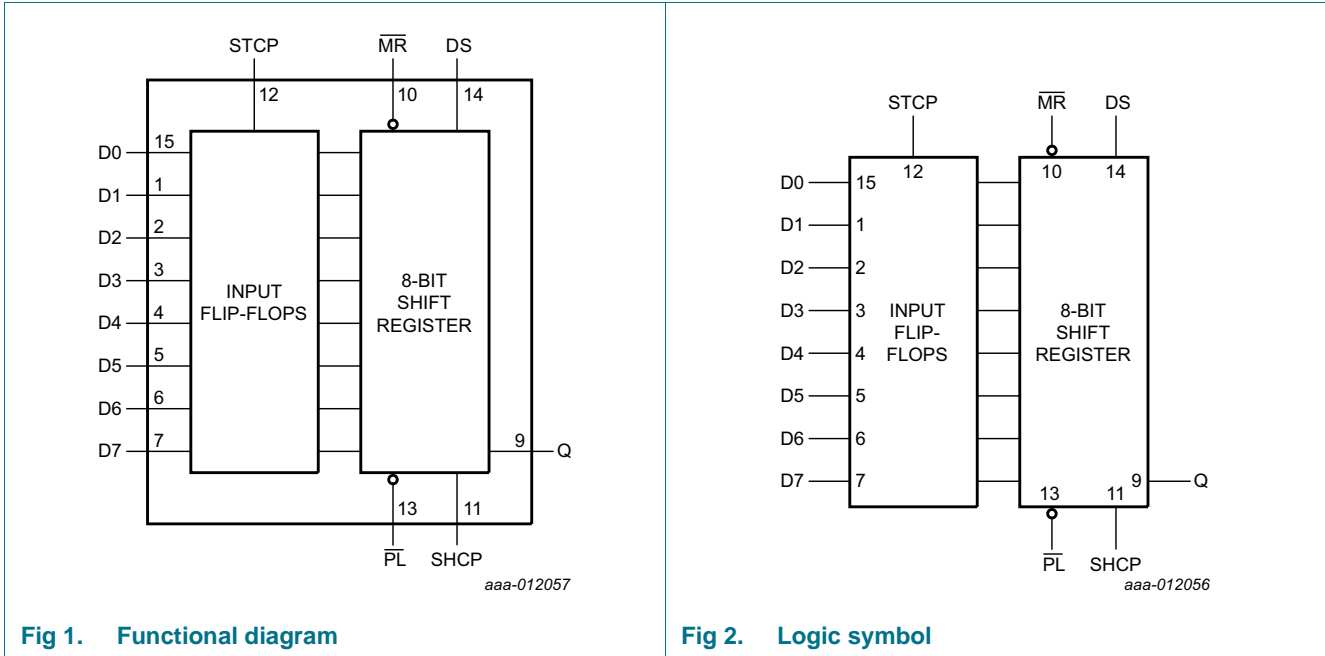


Fig 1. Functional diagram

Fig 2. Logic symbol

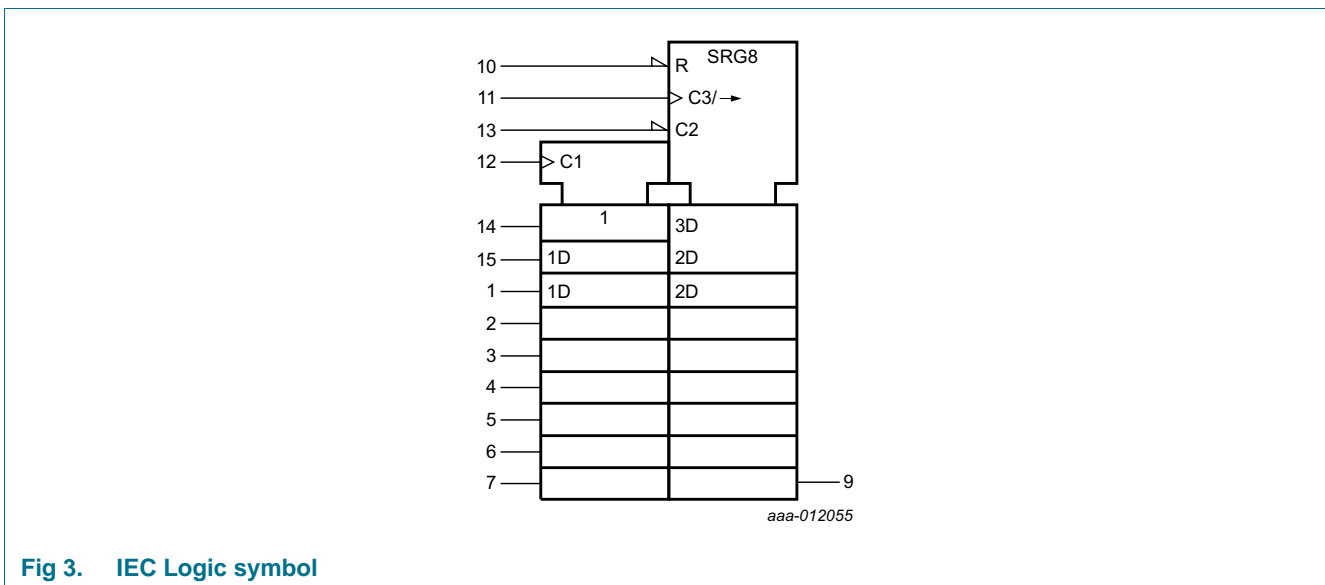


Fig 3. IEC Logic symbol

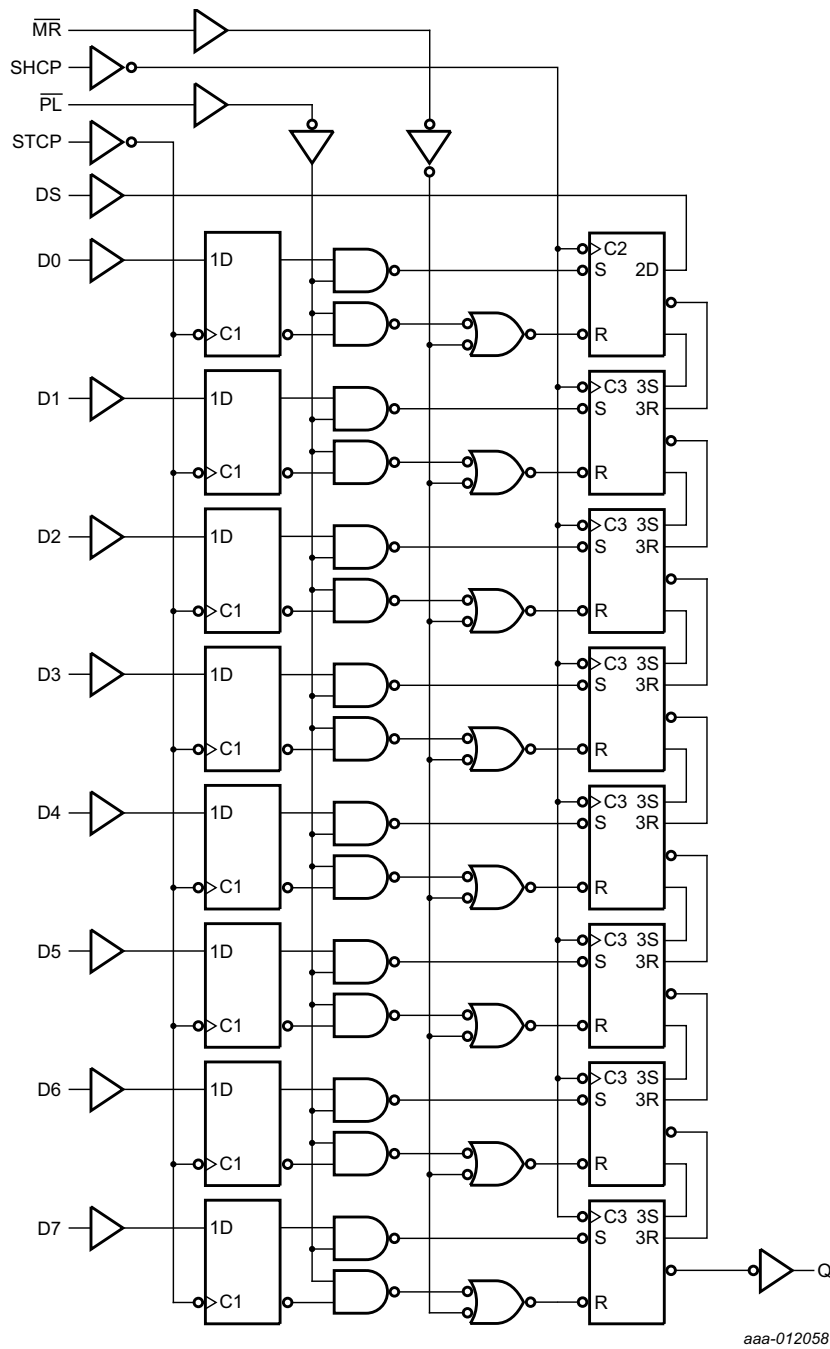
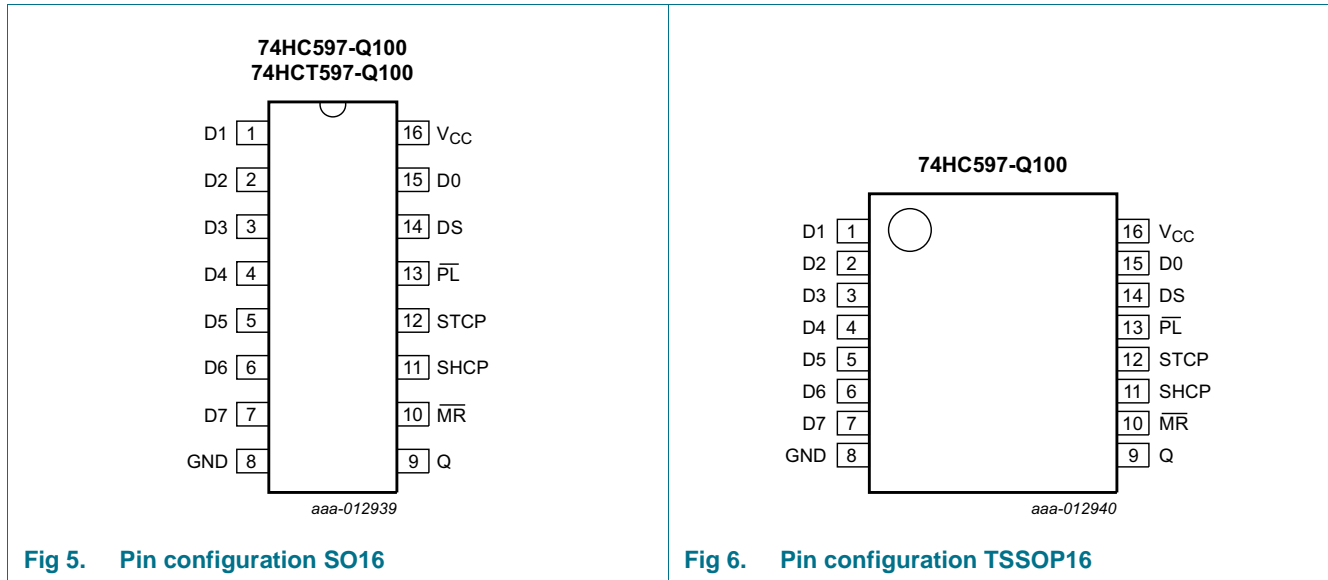


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	8	ground (0 V)
Q	9	serial data output
$\overline{\text{MR}}$	10	asynchronous master reset input (active LOW)
SHCP	11	shift register clock input (LOW-to-HIGH, edge-triggered)
STCP	12	storage register clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{PL}}$	13	parallel load input (active LOW)
DS	14	serial data input
D0, D1, D2, D3, D4, D5, D6, D7	15, 1, 2, 3, 4, 5, 6, 7	parallel data inputs
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Inputs				Function
STCP	SHCP	\overline{PL}	\overline{MR}	
↑	X	X	X	data loaded to input latches
↑	X	L	H	data loaded from inputs to shift register
no clock edge	X	L	H	data transferred from input flip-flops to shift register
X	X	L	L	invalid logic, state of shift register is indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$, $Q_0 = DS$

- [1] H = HIGH voltage level.
 L = LOW voltage level.
 X = don't care.
 ↑ = positive-going transition.

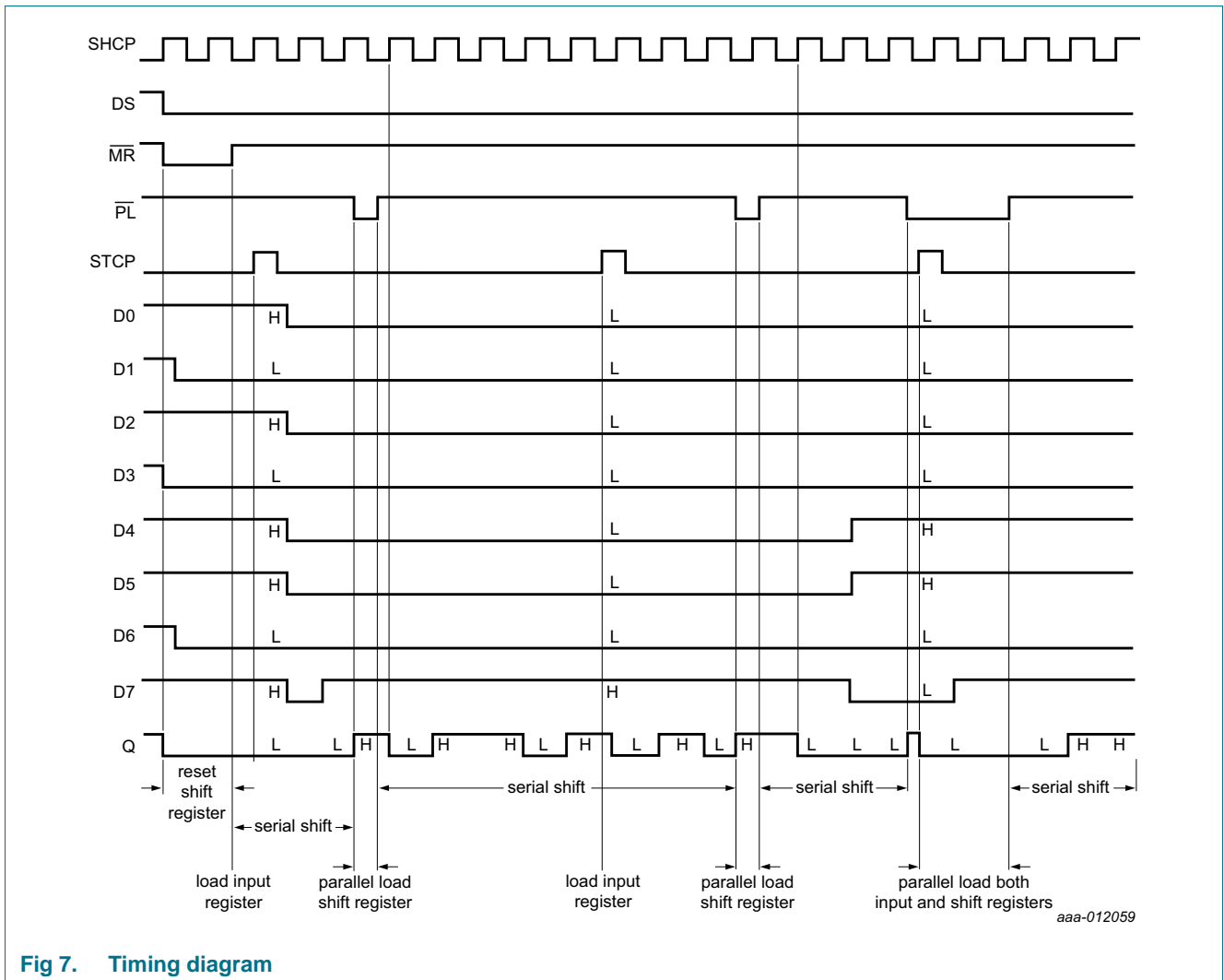


Fig 7. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		[1]	500	mW

[1] For SO16: P_{tot} derates linearly with 8 mW/K above 70 °C.

For TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC597-Q100			74HCT597-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC597-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
		I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80.0	-
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT597-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; DS input	-	25	90	-	112.5	-	122.5	μA
		per input pin; Dn inputs	-	30	108	-	135	-	147	μA
		per input pin; \overline{PL} , \overline{MR} inputs	-	150	540	-	675	-	735	μA
C _I	input capacitance	per input pin; STCP, SHCP inputs	-	150	540	-	675	-	735	μA
		-	-	3.5	-	-	-	-	-	pF
		-	-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-	-

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
74HC597-Q100											
t _{pd}	propagation delay	SHCP to Q; see Figure 8 ^[1]									
		V _{CC} = 2.0 V	-	55	175	-	220	-	265	ns	
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns	
		V _{CC} = 6.0 V	-	16	30	-	37	-	45	ns	
		\overline{MR} to Q; see Figure 9 ^[1]									
		V _{CC} = 2.0 V	-	58	175	-	220	-	265	ns	
		V _{CC} = 4.5 V	-	21	35	-	44	-	53	ns	
		V _{CC} = 6.0 V	-	17	30	-	37	-	45	ns	
		STCP to Q; see Figure 8 ^[1]									
		V _{CC} = 2.0 V	-	80	250	-	315	-	375	ns	
		V _{CC} = 4.5 V	-	29	50	-	63	-	75	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	-	25	-	-	-	-	-	ns	
		V _{CC} = 6.0 V	-	23	43	-	54	-	64	ns	
		\overline{PL} to Q; see Figure 10 ^[1]									
		V _{CC} = 2.0 V	-	69	215	-	270	-	325	ns	
V _{CC} = 4.5 V	-	25	43	-	54	-	65	ns			
V _{CC} = 5.0 V; C _L = 15 pF	-	21	-	-	-	-	-	ns			
V _{CC} = 6.0 V	-	20	37	-	46	-	55	ns			

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit		
			Min	Typ	Max	Min	Max	Min	Max			
t_t	transition time	see Figure 10 ^[2]										
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns		
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns		
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns		
t_w	pulse width	STCP HIGH or LOW; see Figure 8										
		$V_{CC} = 2.0$ V	80	11	-	100	-	120	-	ns		
		$V_{CC} = 4.5$ V	16	4	-	20	-	24	-	ns		
		$V_{CC} = 6.0$ V	14	3	-	17	-	20	-	ns		
		SHCP HIGH or LOW; see Figure 8										
		$V_{CC} = 2.0$ V	80	14	-	100	-	120	-	ns		
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns		
		$V_{CC} = 6.0$ V	14	4	-	17	-	20	-	ns		
		\overline{MR} LOW; see Figure 9										
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns		
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns		
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns		
		\overline{PL} LOW; see Figure 10										
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns		
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns		
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns		
		t_{rec}	recovery time	\overline{MR} to SHCP; see Figure 11								
				$V_{CC} = 2.0$ V	60	-3	-	75	-	90	-	ns
				$V_{CC} = 4.5$ V	12	-1	-	15	-	18	-	ns
$V_{CC} = 6.0$ V	10			-1	-	13	-	15	-	ns		
t_{su}	set-up time	Dn to STCP; see Figure 12										
		$V_{CC} = 2.0$ V	60	8	-	75	-	90	-	ns		
		$V_{CC} = 4.5$ V	12	3	-	15	-	18	-	ns		
		$V_{CC} = 6.0$ V	10	2	-	13	-	15	-	ns		
		DS to SHCP; see Figure 12										
		$V_{CC} = 2.0$ V	60	11	-	75	-	90	-	ns		
		$V_{CC} = 4.5$ V	12	4	-	15	-	18	-	ns		
		$V_{CC} = 6.0$ V	10	3	-	13	-	15	-	ns		
		\overline{PL} to SHCP; see Figure 13										
		$V_{CC} = 2.0$ V	60	11	-	75	-	90	-	ns		
		$V_{CC} = 4.5$ V	12	4	-	15	-	18	-	ns		
		$V_{CC} = 6.0$ V	10	3	-	13	-	15	-	ns		

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit		
			Min	Typ	Max	Min	Max	Min	Max			
t_h	hold time	Dn to STCP; see Figure 12										
		$V_{CC} = 2.0$ V	5	-3	-	5	-	5	-	ns		
		$V_{CC} = 4.5$ V	5	-1	-	5	-	5	-	ns		
		$V_{CC} = 6.0$ V	5	-1	-	5	-	5	-	ns		
		\overline{PL} , DS to SHCP; see Figure 12										
		$V_{CC} = 2.0$ V	5	-6	-	5	-	5	-	ns		
		$V_{CC} = 4.5$ V	5	-2	-	5	-	5	-	ns		
f_{max}	maximum frequency	SHCP; see Figure 8										
		$V_{CC} = 2.0$ V	6.0	29	-	4.8	-	4.0	-	MHz		
		$V_{CC} = 4.5$ V	30	87	-	24	-	20	-	MHz		
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	96	-	-	-	-	-	MHz		
C_{PD}	power dissipation capacitance	$C_L = 50$ pF; $f = 1$ MHz; $V_I = \text{GND to } V_{CC}$ [3]	-	29	-	-	-	-	-	pF		
		74HCT597-Q100										
		t_{pd}	propagation delay	SHCP to Q; see Figure 8 [1]								
				$V_{CC} = 4.5$ V	-	23	40	-	50	-	60	ns
$V_{CC} = 5.0$ V; $C_L = 15$ pF	-			20	-	-	-	-	-	ns		
\overline{MR} to Q; see Figure 9 [1]												
$V_{CC} = 4.5$ V	-			28	49	-	61	-	74	ns		
STCP to Q; see Figure 8 [1]												
$V_{CC} = 4.5$ V	-			33	57	-	71	-	86	ns		
$V_{CC} = 5.0$ V; $C_L = 15$ pF	-			29	-	-	-	-	-	ns		
\overline{PL} to Q; see Figure 10 [1]												
$V_{CC} = 4.5$ V	-			30	52	-	65	-	78	ns		
t_t	transition time	see Figure 8 [2]										
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns		
t_w	pulse width	STCP HIGH or LOW; see Figure 8										
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns		
		SHCP HIGH or LOW; see Figure 8										
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns		
		\overline{MR} LOW; see Figure 9										
		$V_{CC} = 4.5$ V	25	14	-	31	-	38	-	ns		
t_{rec}	recovery time	\overline{PL} LOW; see Figure 10										
		$V_{CC} = 4.5$ V	20	10	-	25	-	30	-	ns		
t_{rec}	recovery time	\overline{MR} to SHCP; see Figure 11										
		$V_{CC} = 4.5$ V	12	-2	-	15	-	18	-	ns		

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to STCP; see Figure 12								
		$V_{CC} = 4.5$ V	12	5	-	15	-	18	-	ns
		DS to SHCP; see Figure 12								
		$V_{CC} = 4.5$ V	12	2	-	15	-	18	-	ns
t_h	hold time	\overline{PL} to SHCP; see Figure 13								
		$V_{CC} = 4.5$ V	12	4	-	15	-	18	-	ns
		Dn to STCP; see Figure 12								
		$V_{CC} = 4.5$ V	5	-1	-	5	-	5	-	ns
f_{max}	maximum frequency	\overline{PL} , DS to SHCP; see Figure 12								
		$V_{CC} = 4.5$ V	5	-2	-	5	-	5	-	ns
		SHCP; see Figure 8								
		$V_{CC} = 4.5$ V	30	75	-	24	-	20	-	MHz
C_{PD}	power dissipation capacitance	$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	83	-	-	-	-	-	MHz
		$C_L = 50$ pF; $f = 1$ MHz; $V_1 = GND$ to $V_{CC} - 1.5$ V ^[3]	-	32	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

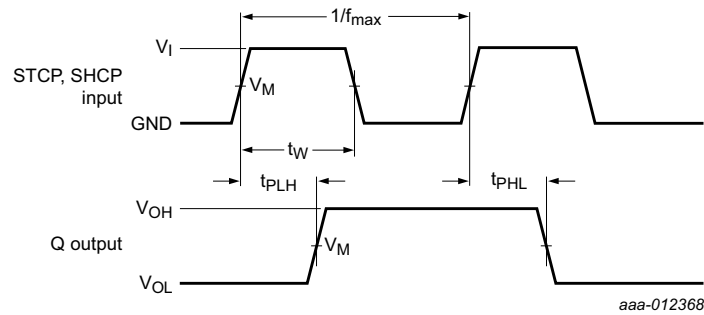
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

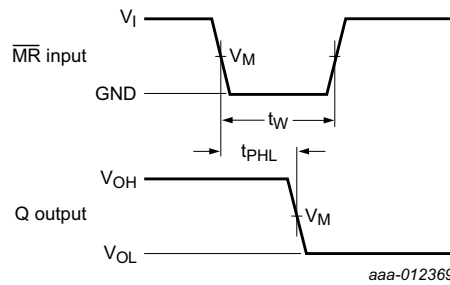
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

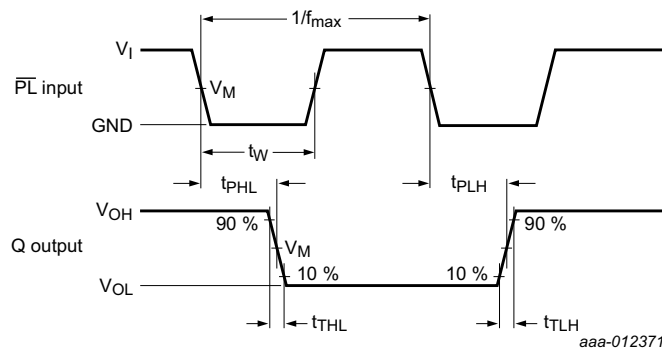
Fig 8. Shift clock and storage clock inputs to output, propagation delays, pulse widths and maximum clock frequency



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

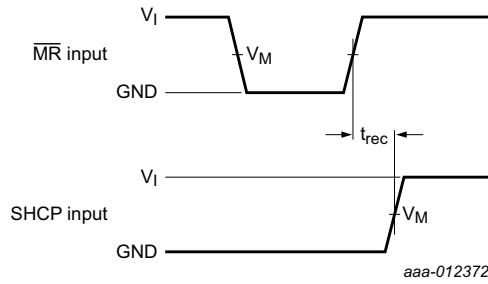
Fig 9. input (\overline{MR}) to (Q), output propagation delays and (\overline{MR}) pulse width



Measurement points are given in [Table 8](#).

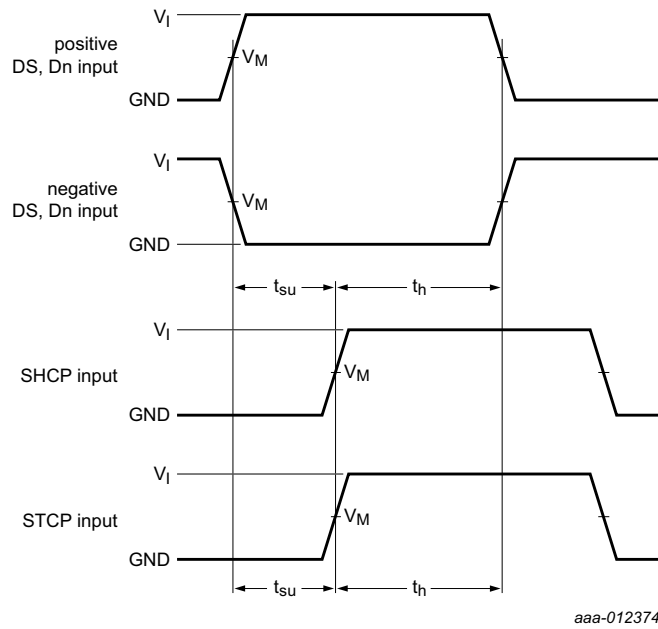
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Input (\overline{PL}) to (Q), output propagation delays, \overline{PL} pulse width and output transition times



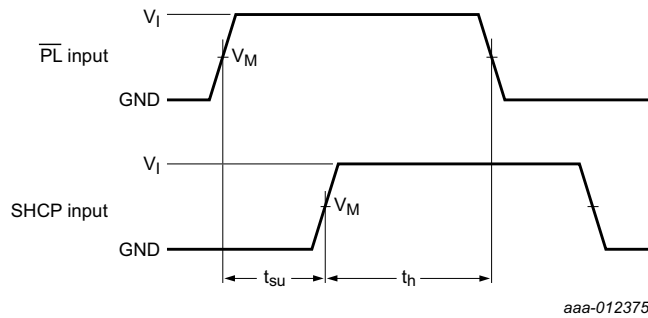
Measurement points are given in [Table 8](#).

Fig 11. Input ($\overline{\text{MR}}$) to shift clock (SHCP) and storage clock (STCP) recovery times



Measurement points are given in [Table 8](#).

Fig 12. Hold and set-up times for (DS), (Dn) inputs to (SHCP), (STCP) inputs



Measurement points are given in [Table 8](#).

Fig 13. Set-up times for ($\overline{\text{PL}}$) input to (SHCP) input

Table 8. Measurement points

Type	Input	V_I	Output
	V_M		V_M
74HC597-Q100	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT597-Q100	1.3 V	GND to 3 V	1.3 V

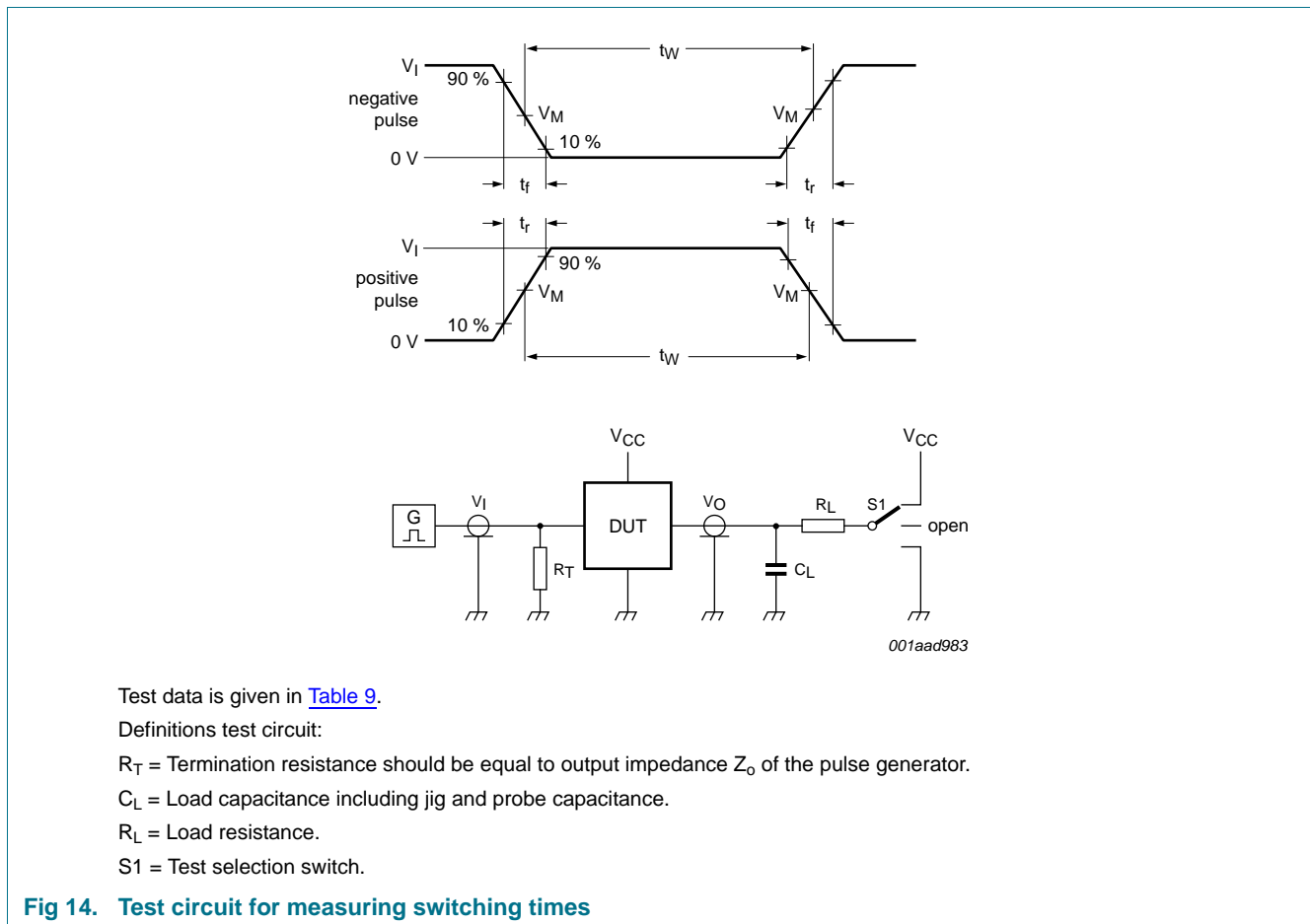


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC597-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT597-Q100	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

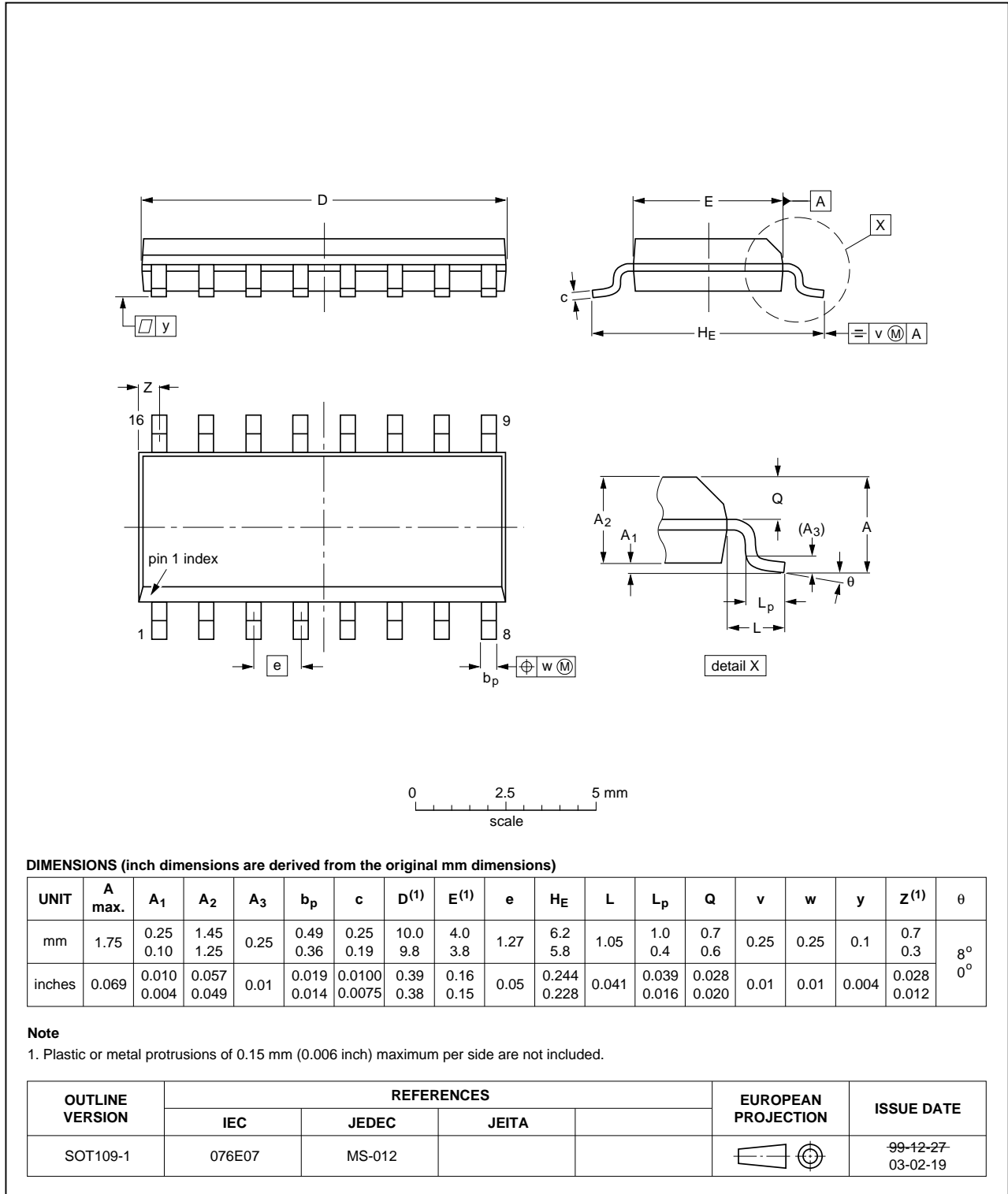


Fig 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

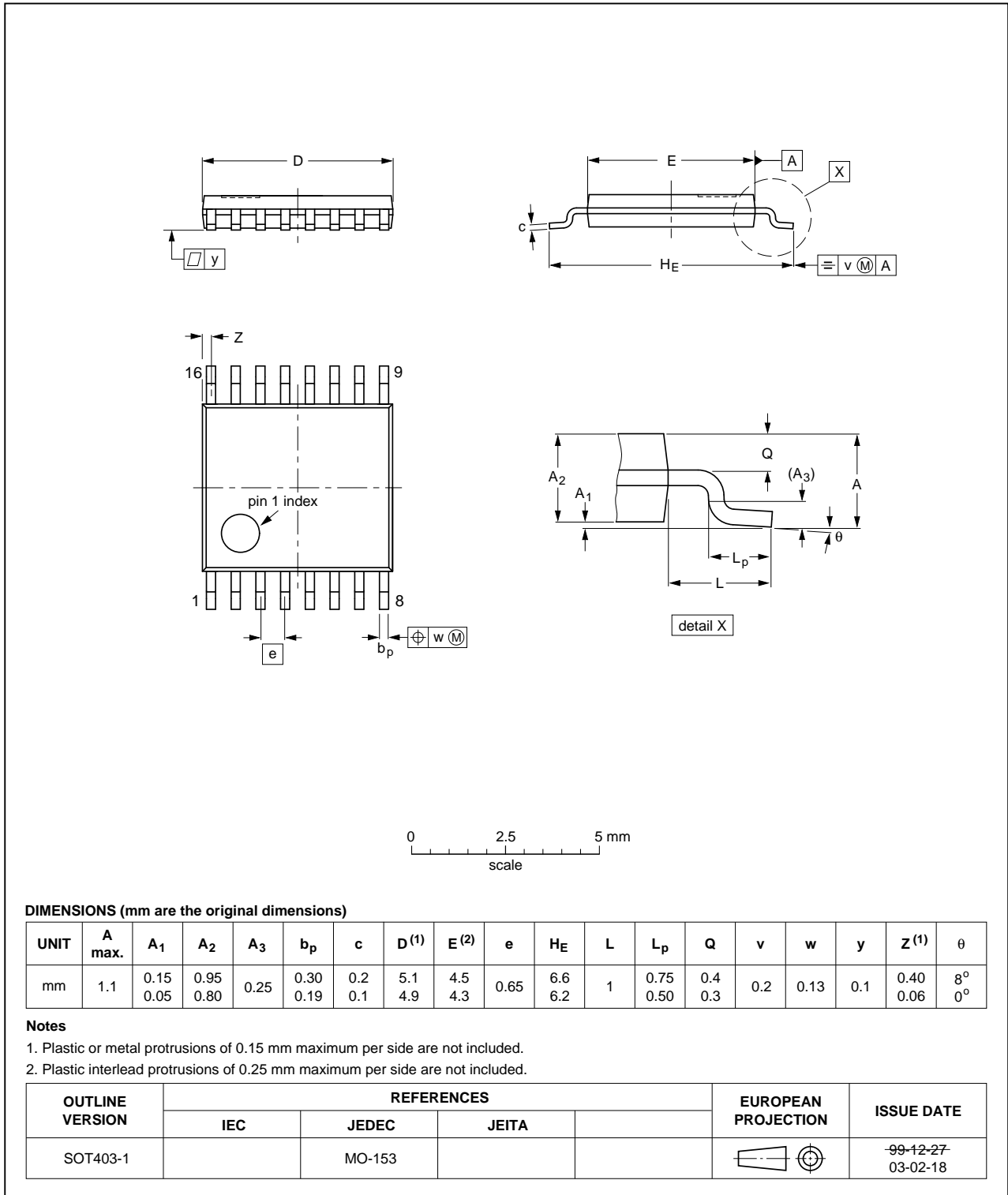


Fig 16. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT597_Q100 v.1	20140526	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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