

74HC74; 74HCT74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 7 — 13 September 2021

Product data sheet

1. General description

The 74HC74 and 74HCT74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set (nSD) and reset (nRD) inputs, and complementary nQ and nQ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

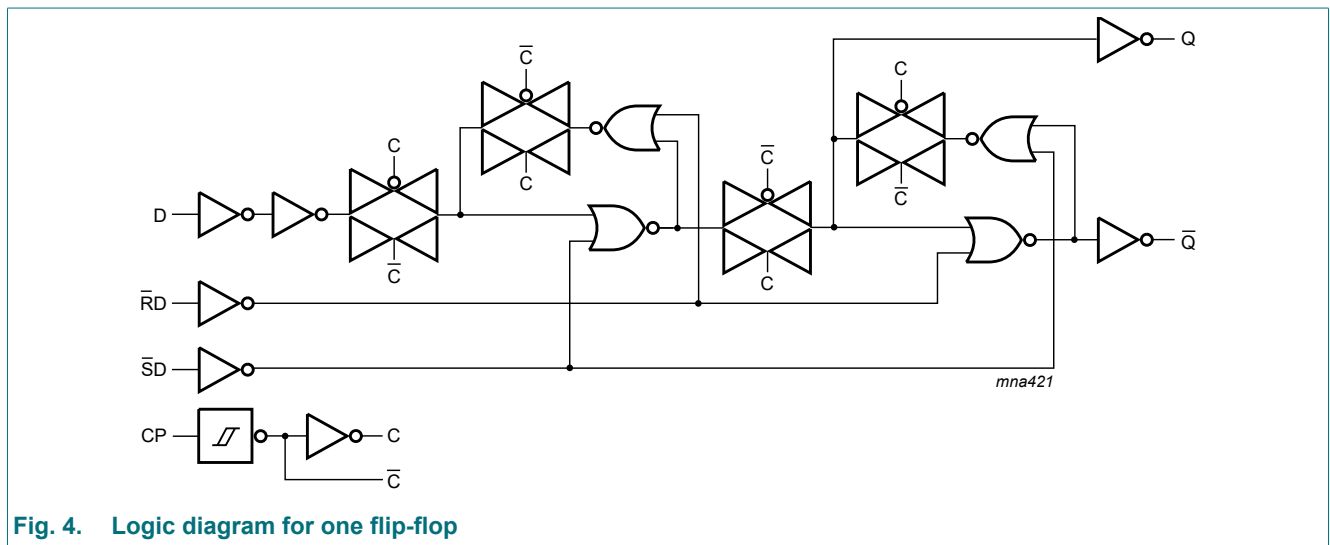
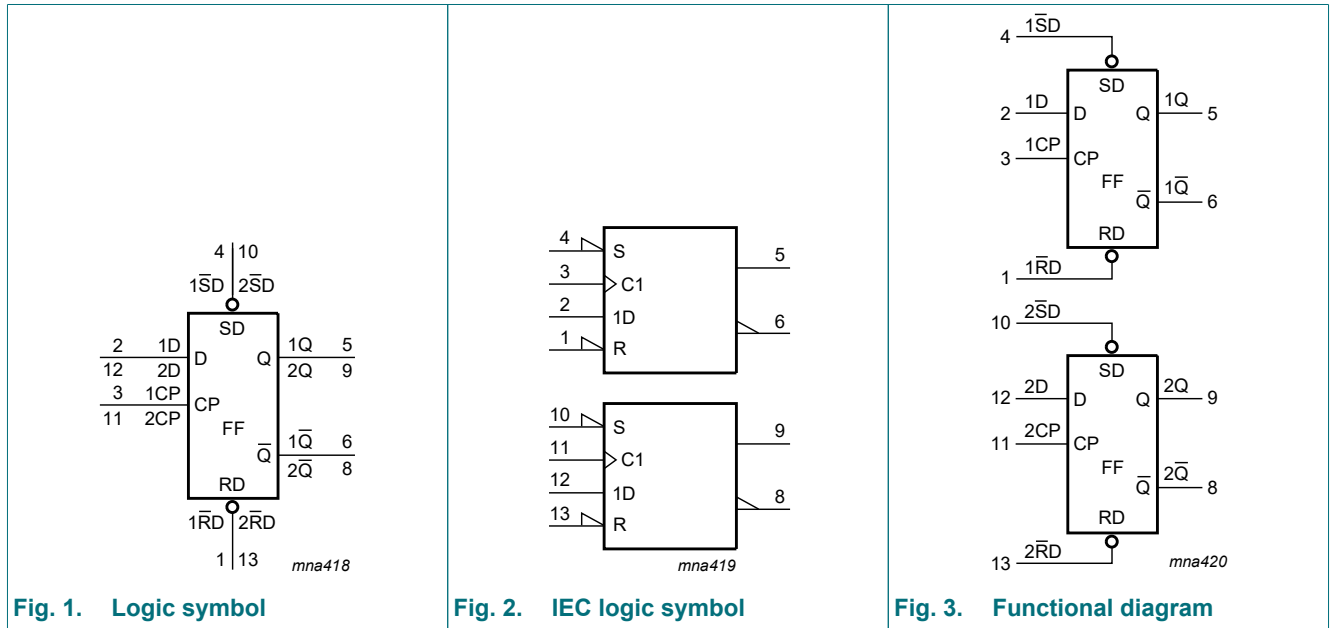
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC74: CMOS level
 - For 74HCT74: TTL level
- Symmetrical output impedance
- High noise immunity
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

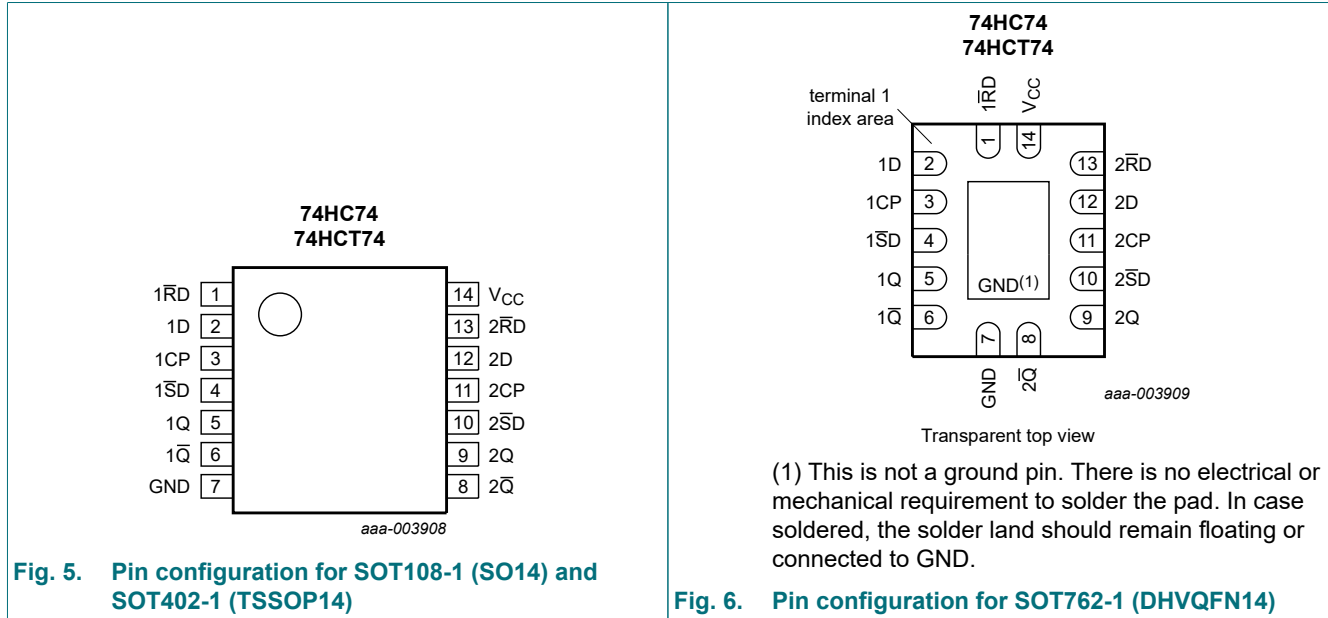
| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC74D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HCT74D | | | | |
| 74HC74PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74HCT74PW | | | | |
| 74HC74BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74HCT74BQ | | | | |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--|
| 1RD | 1 | asynchronous reset-direct input (active LOW) |
| 1D | 2 | data input |
| 1CP | 3 | clock input (LOW-to-HIGH, edge-triggered) |
| 1SD | 4 | asynchronous set-direct input (active LOW) |
| 1Q | 5 | output |
| 1Q | 6 | complement output |
| GND | 7 | ground (0 V) |
| 2Q | 8 | complement output |
| 2Q | 9 | output |
| 2SD | 10 | asynchronous set-direct input (active LOW) |
| 2CP | 11 | clock input (LOW-to-HIGH, edge-triggered) |
| 2D | 12 | data input |
| 2RD | 13 | asynchronous reset-direct input (active LOW) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | | | Output | |
|-------|-----|-----|----|--------|-----|
| nSD | nRD | nCP | nD | nQ | nQ̄ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition.

| Input | | | | Output | |
|-------|-----|-----|----|-------------------|--------------------|
| nSD | nRD | nCP | nD | nQ _{n+1} | nQ̄ _{n+1} |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V | - | ±20 | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V | - | ±20 | mA |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | - | ±25 | mA |
| I _{CC} | supply current | | - | +100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | | [1] | 500 | mW |

- [1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
 For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
 For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC74 | | | 74HCT74 | | | Unit |
|------------------|-------------------------------------|-------------------------|--------|------|-----------------|---------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------------------------------------|---------|------|--------------------------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| 74HC74 | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.84 | 4.32 | - | 3.7 | - | V |
| | | I _O = -5.2 mA; V _{CC} = 6.0 V | 5.34 | 5.81 | - | 5.2 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.33 | - | 0.4 | V |
| | | I _O = 5.2 mA; V _{CC} = 6.0 V | - | 0.16 | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 40 | - | 80 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | pF |
| 74HCT74 | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | V |

Dual D-type flip-flop with set and reset; positive edge-trigger

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------------------------------------|---------|------|--------------------------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V I _O = -4 mA | 3.84 | 4.32 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V I _O = 4.0 mA | - | 0.15 | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±1.0 | - | ±1.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 40 | - | 80 | µA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | | | |
| | | per input pin; nD, nRD inputs | - | 70 | 315 | - | 343 | µA |
| | | per input pin; nSD, nCP input | - | 80 | 360 | - | 392 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 9.

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|---|-------------------|---|-------------------------------------|---------|-----|--------------------------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| 74HC74 | | | | | | | | |
| t _{pd} | propagation delay | nCP to nQ, nQ̄; see Fig. 7 [2] | | | | | | |
| | | V _{CC} = 2.0 V | - | 47 | 220 | - | 265 | ns |
| | | V _{CC} = 4.5 V | - | 17 | 44 | - | 53 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 14 | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 14 | 37 | - | 45 | ns |
| | | nSD to nQ, nQ̄; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 2.0 V | - | 50 | 250 | - | 300 | ns |
| | | V _{CC} = 4.5 V | - | 18 | 50 | - | 60 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 15 | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 14 | 43 | - | 51 | ns |
| | | nRD to nQ, nQ̄; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 2.0 V | - | 52 | 250 | - | 300 | ns |
| V _{CC} = 4.5 V | - | 19 | 50 | - | 60 | ns | | |
| V _{CC} = 5 V; C _L = 15 pF | - | 16 | - | - | - | ns | | |
| V _{CC} = 6.0 V | - | 15 | 43 | - | 51 | ns | | |
| t _t | transition time | nQ, nQ̄; see Fig. 7 [3] | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 16 | - | 19 | ns |

Dual D-type flip-flop with set and reset; positive edge-trigger

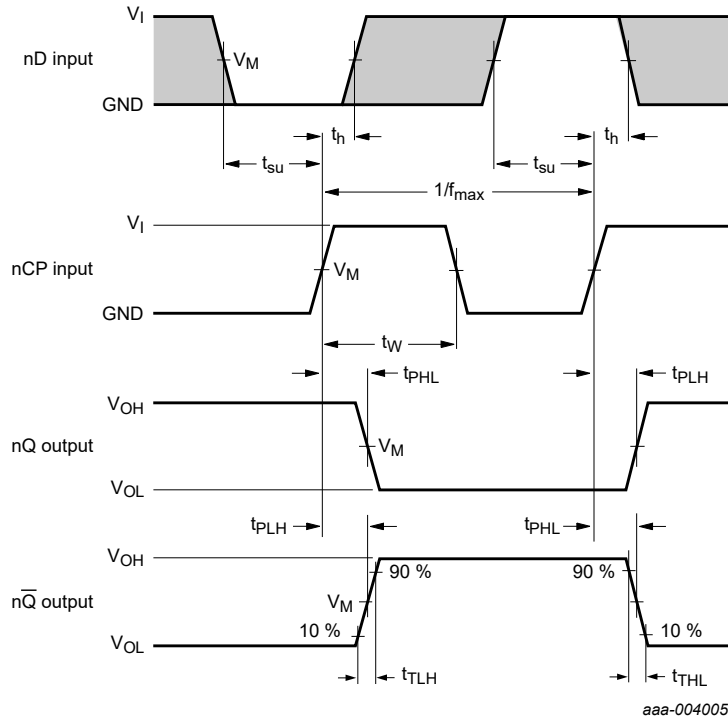
| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|---|-------------------------------|--|-------------------------------------|---------|-----|--------------------------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _w | pulse width | nCP HIGH or LOW; see Fig. 7 | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 19 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 7 | - | 24 | - | ns |
| | | V _{CC} = 6.0 V | 17 | 6 | - | 20 | - | ns |
| | | nSD, nRD LOW; see Fig. 8 | | | | | | |
| | | V _{CC} = 2.0 V | 100 | 19 | - | 120 | - | ns |
| | | V _{CC} = 4.5 V | 20 | 7 | - | 24 | - | ns |
| V _{CC} = 6.0 V | 17 | 6 | - | 20 | - | ns | | |
| t _{rec} | recovery time | nSD, nRD; see Fig. 8 | | | | | | |
| | | V _{CC} = 2.0 V | 40 | 3 | - | 45 | - | ns |
| | | V _{CC} = 4.5 V | 8 | 1 | - | 9 | - | ns |
| | | V _{CC} = 6.0 V | 7 | 1 | - | 8 | - | ns |
| t _{su} | set-up time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 2.0 V | 75 | 6 | - | 90 | - | ns |
| | | V _{CC} = 4.5 V | 15 | 2 | - | 18 | - | ns |
| | | V _{CC} = 6.0 V | 13 | 2 | - | 15 | - | ns |
| t _h | hold time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 2.0 V | 3 | -6 | - | 3 | - | ns |
| | | V _{CC} = 4.5 V | 3 | -2 | - | 3 | - | ns |
| | | V _{CC} = 6.0 V | 3 | -2 | - | 3 | - | ns |
| f _{max} | maximum frequency | nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 2.0 V | 4.8 | 23 | - | 4.0 | - | MHz |
| | | V _{CC} = 4.5 V | 24 | 69 | - | 20 | - | MHz |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 76 | - | - | - | MHz |
| | | V _{CC} = 6.0 V | 28 | 82 | - | 24 | - | MHz |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [4] | - | 24 | - | - | - | pF |
| 74HCT74 | | | | | | | | |
| t _{pd} | propagation delay | nCP to nQ, nQ̄; see Fig. 7 [2] | | | | | | |
| | | V _{CC} = 4.5 V | - | 18 | 44 | - | 53 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 15 | - | - | - | ns |
| | | nSD to nQ, nQ̄; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 4.5 V | - | 23 | 50 | - | 60 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 18 | - | - | - | ns |
| | | nRD to nQ, nQ̄; see Fig. 8 [2] | | | | | | |
| | | V _{CC} = 4.5 V | - | 24 | 50 | - | 60 | ns |
| V _{CC} = 5 V; C _L = 15 pF | - | 18 | - | - | - | ns | | |

Dual D-type flip-flop with set and reset; positive edge-trigger

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|--|-------------------------------------|---------|-----|--------------------------------------|-----|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _t | transition time | nQ, n \bar{Q} ; see Fig. 7 [3] | | | | | | |
| | | V _{CC} = 4.5 V | - | 7 | 19 | - | 22 | ns |
| t _W | pulse width | nCP HIGH or LOW; see Fig. 7 | | | | | | |
| | | V _{CC} = 4.5 V | 23 | 9 | - | 27 | - | ns |
| | | n \bar{S} D, n \bar{R} D LOW; see Fig. 8 | | | | | | |
| | | V _{CC} = 4.5 V | 20 | 9 | - | 24 | - | ns |
| t _{rec} | recovery time | n \bar{S} D, n \bar{R} D; see Fig. 8 | | | | | | |
| | | V _{CC} = 4.5 V | 8 | 1 | - | 9 | - | ns |
| t _{su} | set-up time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 4.5 V | 15 | 5 | - | 18 | - | ns |
| t _h | hold time | nD to nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 4.5 V | 3 | -3 | - | 3 | - | ns |
| f _{max} | maximum frequency | nCP; see Fig. 7 | | | | | | |
| | | V _{CC} = 4.5 V | 22 | 54 | - | 18 | - | MHz |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 59 | - | - | - | MHz |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [4] | - | 29 | - | - | - | pF |

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] t_t is the same as t_{THL} and t_{TLH}.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

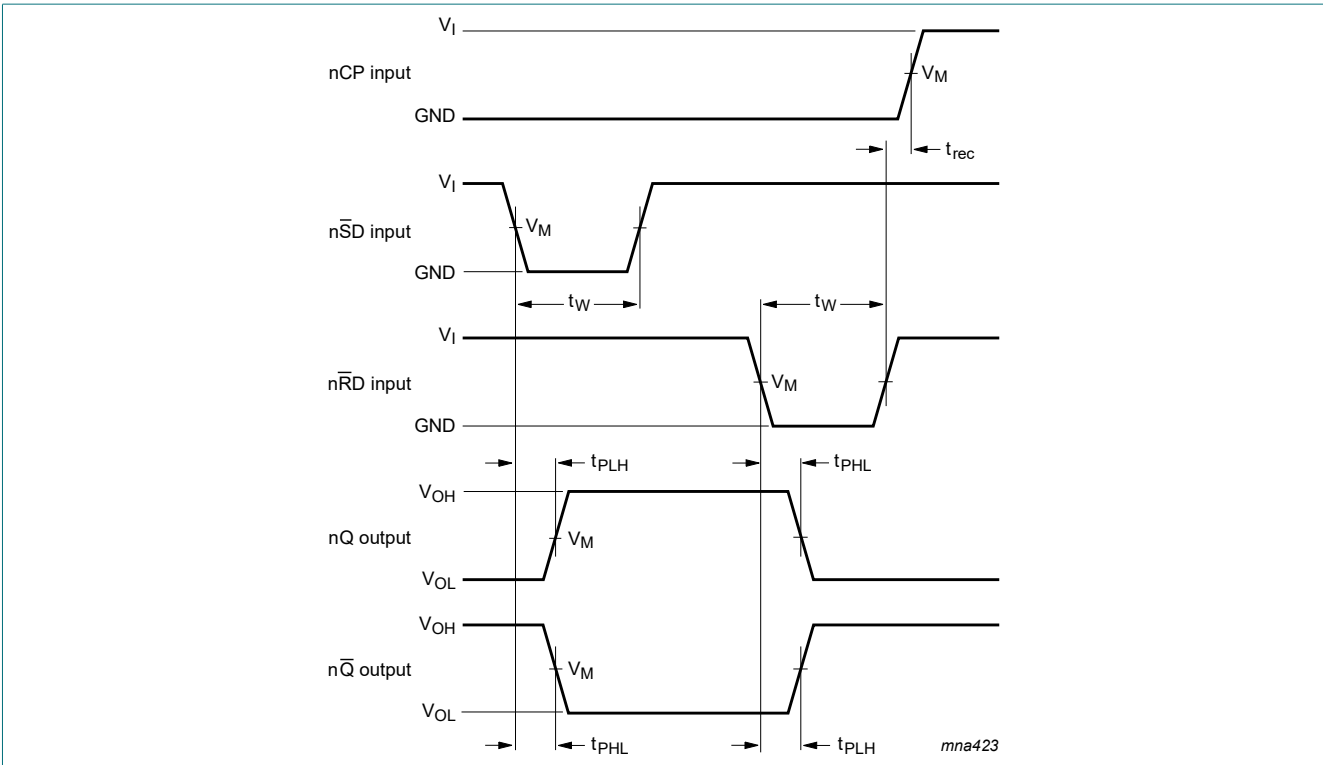


Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)

Dual D-type flip-flop with set and reset; positive edge-trigger



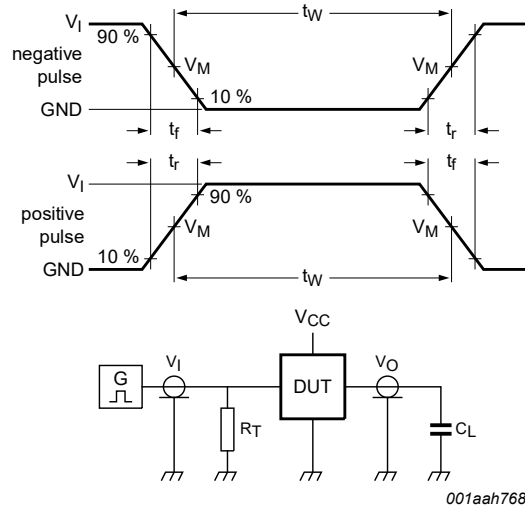
Measurement points are given in [Table 9](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. The set ($n\bar{SD}$) and reset ($n\bar{RD}$) input to output ($nQ, n\bar{Q}$) propagation delays, set and reset pulse widths and the $n\bar{SD}, n\bar{RD}$ to nCP recovery time

Table 9. Measurement points

| Type | Input | Output |
|---------|-------------|-------------|
| | V_M | V_M |
| 74HC74 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT74 | 1.3 V | 1.3 V |

Dual D-type flip-flop with set and reset; positive edge-trigger



001aah768

Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

| Type | Input | | Load | | Test |
|---------|----------|------------|--------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | |
| 74HC74 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | t_{PLH}, t_{PHL} |
| 74HCT74 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

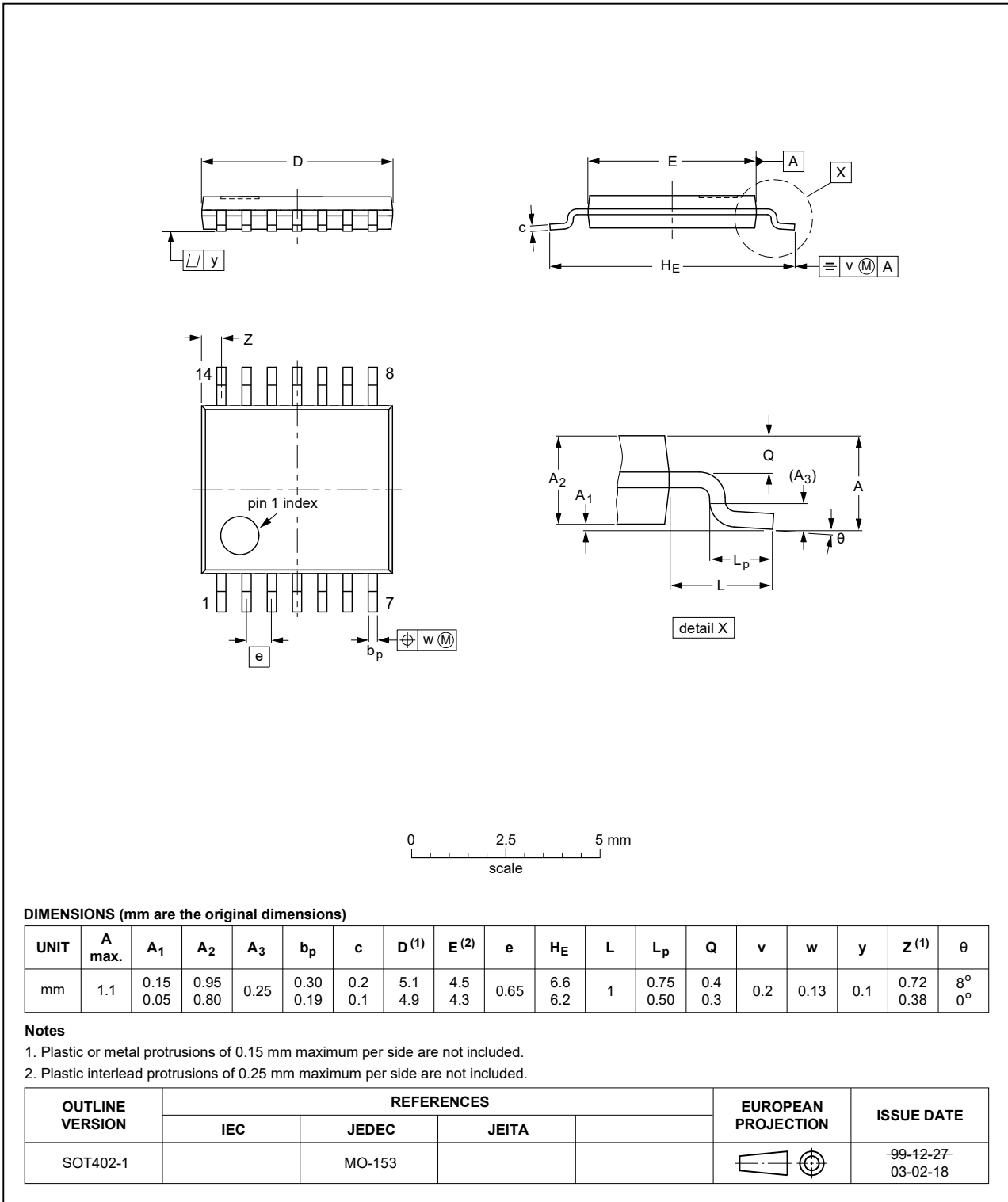


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 12. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--|-----------------------|---------------|--------------------|
| 74HC_HCT74 v.7 | 20210913 | Product data sheet | - | 74HC_HCT74 v.6 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC74DB and 74HCTDB (SOT337-1/SSOP14) removed. Section 2 updated. | | | |
| 74HC_HCT74 v.6 | 20200421 | Product data sheet | - | 74HC_HCT74 v.5 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 6: Pin configuration for SOT762-1 (DHVQFN14) corrected (errata). Table 5: Derating values for P_{tot} total power dissipation updated. | | | |
| 74HC_HCT74 v.5 | 20151203 | Product data sheet | - | 74HC_HCT74 v.4 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC74N and 74HCT74N (SOT27-1) removed. | | | |
| 74HC_HCT74 v.4 | 20120827 | Product data sheet | - | 74HC_HCT74 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT74 v.3 | 20030710 | Product data sheet | - | 74HC_HCT74_CNV v.2 |
| 74HC_HCT74_CNV v.2 | 19980223 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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