74LVC1G240

Single inverting buffer/line driver; 3-state

Rev. 1 — 9 March 2022 Product data sheet

1. General description

The 74LVC1G240 is a 1-bit inverting buffer/line driver with 3-state output. The device features an output enable $\overline{OE}$. A HIGH on $\overline{OE}$ causes the output to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 1000 V
- CMOS low power consumption
- Inputs accept voltages up to 5 V
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
74LVC1G240GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G240GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G240GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3

4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC1G240GM	V2
74LVC1G240GS	V2
74LVC1G240GX	V2

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

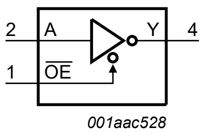


Fig. 1. Logic symbol

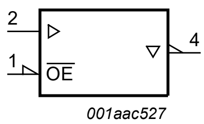


Fig. 2. IEC logic symbol

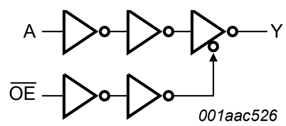


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

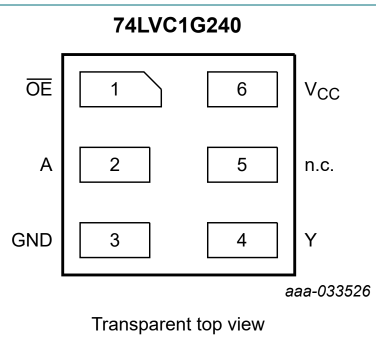


Fig. 4. Pin configuration SOT886 and SOT1202 (XSON6)

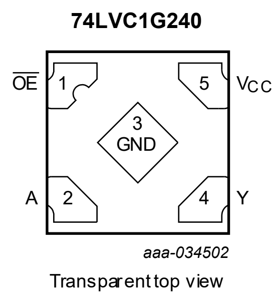


Fig. 5. Pin configuration SOT1226-3 (X2SON5)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT886 and SOT1202	SOT1226-3	
$\overline{\text{OE}}$	1	1	output enable input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	5	-	not connected
V_{CC}	6	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state.

Input		Output
$\overline{OE}$	A	Y
L	L	H
L	H	L
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW
T_{stg}	storage temperature			-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 μA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.45	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.3	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.4	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.55	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = -100 μA	V_{CC} - 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = -4 mA	1.2	-	-	V
		V_{CC} = 2.3 V; I_O = -8 mA	1.9	-	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	2.2	-	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	2.3	-	-	V
		V_{CC} = 4.5 V; I_O = -32 mA	3.8	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	±0.1	±1	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	±0.1	±2	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	5	500	μA
C_I	input capacitance		-	5	-	pF

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = 100 μA	-	-	0.1	V
		V_{CC} = 1.65 V; I_O = 4 mA	-	-	0.70	V
		V_{CC} = 2.3 V; I_O = 8 mA	-	-	0.45	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	-	0.60	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	-	0.80	V
		V_{CC} = 4.5 V; I_O = 32 mA	-	-	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 1.65 V to 5.5 V; I_O = -100 μA	V_{CC} - 0.1	-	-	V
		V_{CC} = 1.65 V; I_O = -4 mA	0.95	-	-	V
		V_{CC} = 2.3 V; I_O = -8 mA	1.7	-	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	1.9	-	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	2.0	-	-	V
		V_{CC} = 4.5 V; I_O = -32 mA	3.4	-	-	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	-	±1	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	-	±2	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	-	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	4	μA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	-	500	μA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A to Y; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V; C_L = 15 pF; R_L = 1 MΩ	1.0	3.8	6.9	1.0	8.7	ns
		V_{CC} = 2.3 V to 2.7 V; C_L = 15 pF; R_L = 1 MΩ	0.5	2.4	4.6	0.5	5.8	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF; R_L = 1 MΩ	0.5	1.9	3.7	0.5	4.6	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF; R_L = 1 MΩ	0.5	1.6	3.4	0.5	4.2	ns
		A to Y; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V; C_L = 30 pF; R_L = 1 kΩ	1.0	3.3	8.0	1.0	10.5	ns
		V_{CC} = 2.3 V to 2.7 V; C_L = 30 pF; R_L = 500 Ω	0.5	2.2	5.5	0.5	7	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	0.5	2.5	5.5	0.5	7	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF; R_L = 500 Ω	0.5	2.1	4.5	0.5	6	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF; R_L = 500 Ω	0.5	1.7	4.0	0.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to Y; see Fig. 7 [3]						
		V_{CC} = 1.65 V to 1.95 V; C_L = 30 pF; R_L = 1 kΩ	1.0	4.1	9.4	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V; C_L = 30 pF; R_L = 500 Ω	0.5	2.8	6.6	0.5	8.5	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	0.5	3.3	6.6	0.5	8.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF; R_L = 500 Ω	0.5	2.4	5.3	0.5	7	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF; R_L = 500 Ω	0.5	2.1	5.0	0.5	6.5	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Fig. 7 [4]						
		V_{CC} = 1.65 V to 1.95 V; C_L = 30 pF; R_L = 1 kΩ	1.0	4.3	9.2	1.0	12	ns
		V_{CC} = 2.3 V to 2.7 V; C_L = 30 pF; R_L = 500 Ω	0.5	2.7	5.0	0.5	6.5	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	0.5	3.0	5.0	0.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF; R_L = 500 Ω	0.5	3.1	5.0	0.5	6.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF; R_L = 500 Ω	0.5	2.2	4.2	0.5	5.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; f_i = 10 MHz [5]						
		output enabled	-	25	-	-	-	pF
		output disabled	-	6	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}
[3] t_{en} is the same as t_{PZH} and t_{PZL}
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

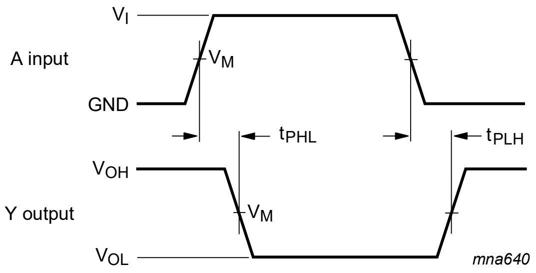
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

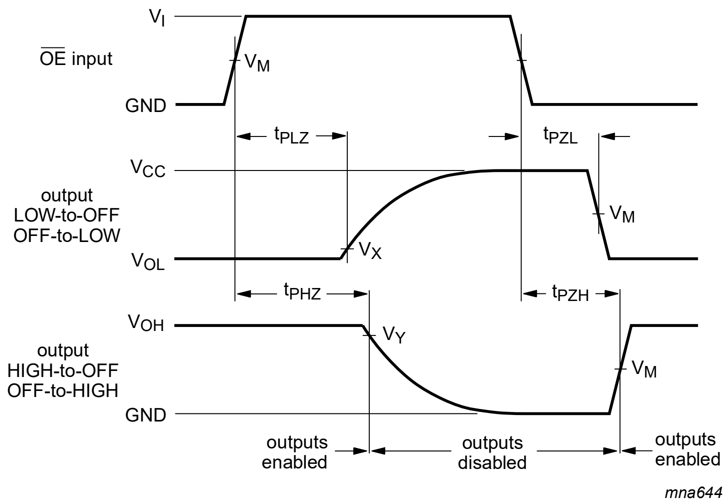
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The data input (A) to output (Y) propagation delays



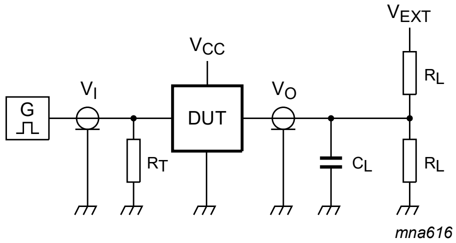
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

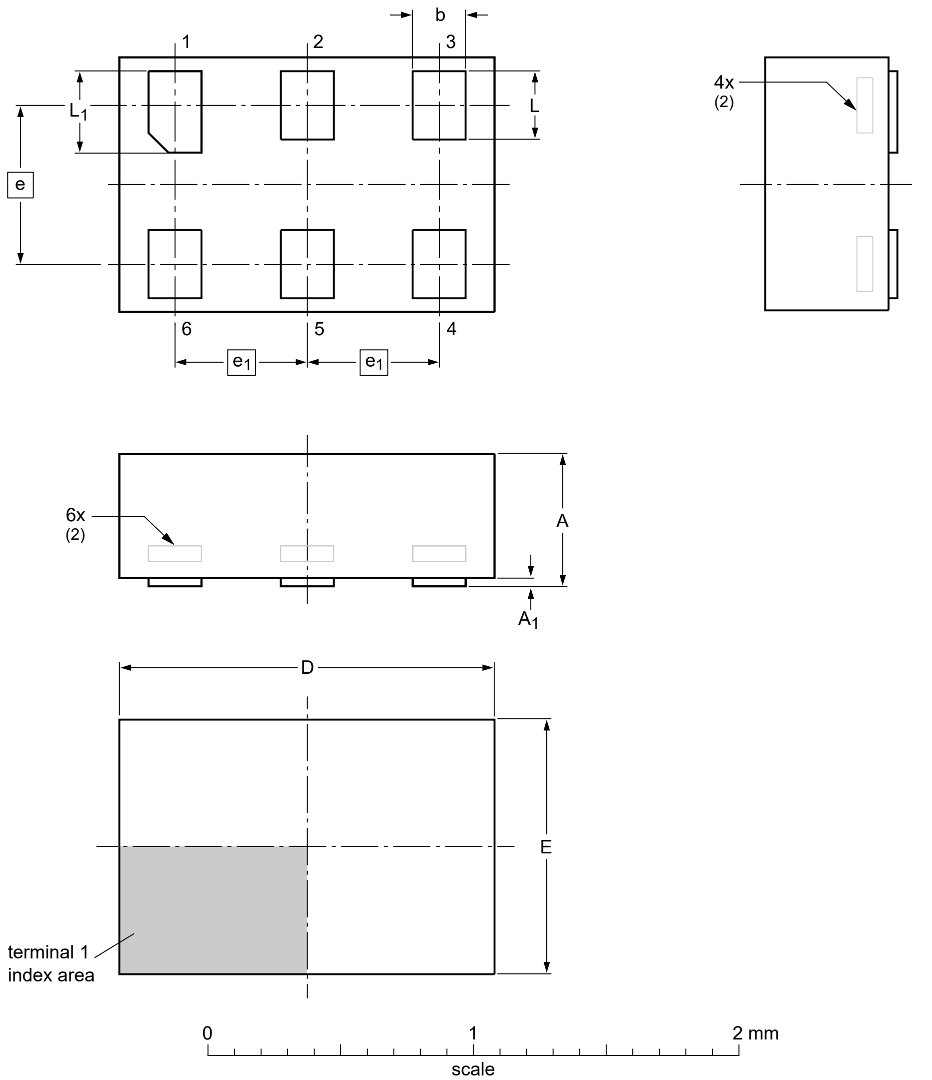
Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		V_{EXT}		
V_{CC}	V_I	t_r, t_f	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	open	GND	$2V_{CC}$

12. Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm | SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
mm	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

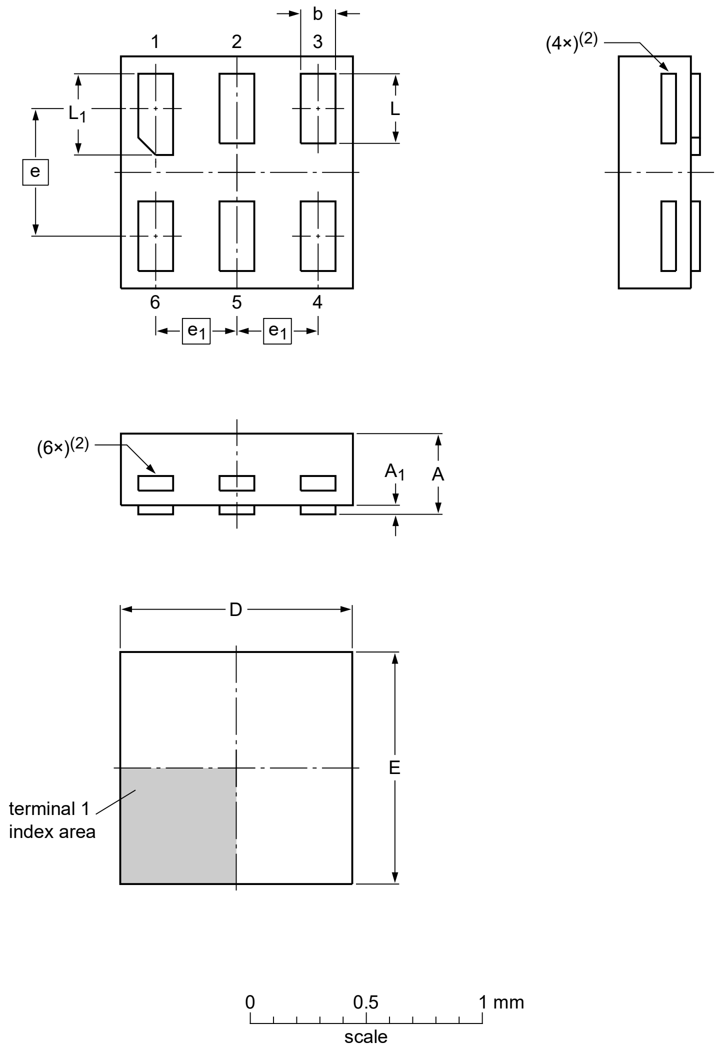
Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 9. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

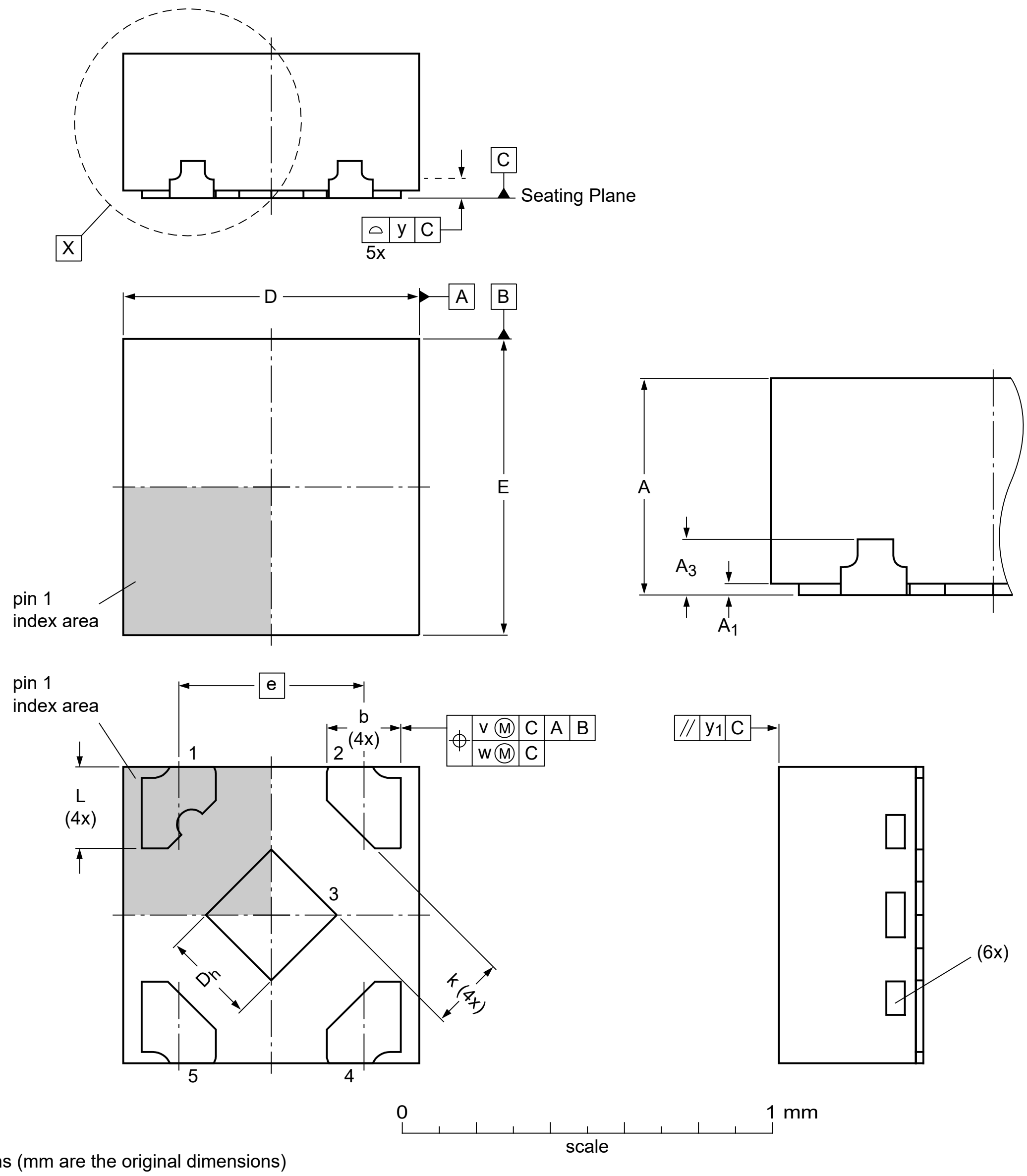
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig. 10. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm **SOT1226-3**



Dimensions (mm are the original dimensions)

Unit		A	A1	A3	D	Dh	E	b	e	K	L	v	w	y	y1
mm	max	0.35	0.04	0.10 (Typ.)	0.85	0.30	0.85	0.25			0.27				
	nom	0.32	0.02		0.80	0.25	0.80	0.20	0.50		0.22	0.1	0.05	0.05	0.05
	min	0.30	0.00		0.75	0.20	0.75	0.15		0.20	0.17				

sot1226-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT1226-3		- - -				~~19-11-06~~ 19-11-07

Fig. 11. Package outline SOT1226-3 (X2SON5)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G240 v.1	20220309	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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