74LVC3G17-Q100

Triple non-inverting Schmitt trigger with 5 V tolerant input

Rev. 3 — 27 November 2018

Product data sheet

1. General description

The 74LVC3G17-Q100 provides three non-inverting buffers with Schmitt trigger input. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC3G17-Q100 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- · Direct interface with TTL levels

3. Applications

· Wave and pulse shapers for highly noisy environments

4. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74LVC3G17DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2					
74LVC3G17DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1					



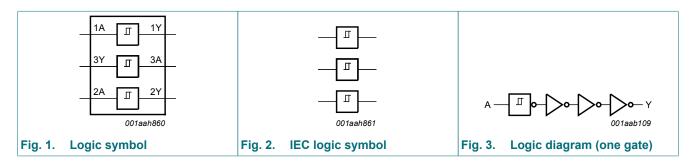
5. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC3G17DP-Q100	V17
74LVC3G17DC-Q100	V17

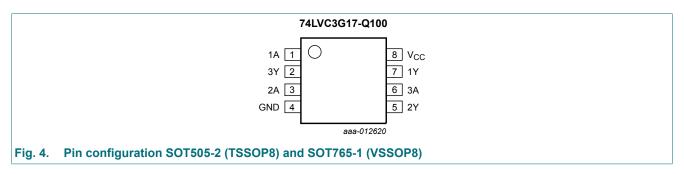
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram



7. Pinning information

7.1. Pinning



7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

8. Functional description

Table 4. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input	Output
nA	nY
L	L
Н	Н

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
Vo	output voltage	Active mode	[1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V	[1][2]	-0.5	+6.5	V
I _O	output current	$V_O = 0 \text{ V to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	250	mW

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] When $V_{CC} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.
- [3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_{I}	input voltage		0	5.5	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T _{amb} =	-40 °C to	+85 °C	T _{am} -40 °C to		Unit
				Min	Typ [1]	Max	Min	Max	1
V _{OL}	LOW-level output	$V_I = V_{T+} \text{ or } V_{T-}$							
	voltage	I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V		-	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V		-	-	0.45	-	0.70	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$		-	-	0.3	-	0.45	V
		I_{O} = 12 mA; V_{CC} = 2.7 V		-	-	0.4	-	0.60	V
		I_{O} = 24 mA; V_{CC} = 3.0 V		-	-	0.55	-	0.80	V
		I_{O} = 32 mA; V_{CC} = 4.5 V		-	-	0.55	-	0.80	V
V _{OH}	HIGH-level	$V_I = V_{T+}$ or V_{T-}							
	output voltage	I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V		V _{CC} - 0.1	-	-	V _{CC} - 0.1	-	V
		I_{O} = -4 mA; V_{CC} = 1.65 V		1.2	-	-	0.95	-	V
		I_{O} = -8 mA; V_{CC} = 2.3 V		1.9	-	-	1.7	-	V
		I _O = -12 mA; V _{CC} = 2.7 V		2.2	-	-	1.9	-	V
		I _O = -24 mA; V _{CC} = 3.0 V		2.3	-	-	2.0	-	V
		I _O = -32 mA; V _{CC} = 4.5 V		3.8	-	-	3.4	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	[2]	-	±0.1	±1	-	±1	μA
l _{OFF}	power-off leakage current	V_{I} or $V_{O} = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$		-	±0.1	±2	-	±2	μΑ
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	[2]	-	0.1	4	-	4	μΑ
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	[2]	-	5	500	-	500	μΑ
Cı	input capacitance			-	3.5	-	-	-	pF

^[1] All typical values are measured at T_{amb} = 25 °C.

11.1. Transfer characteristics

Table 8. Transfer characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

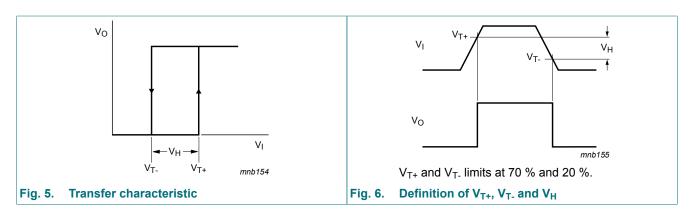
Symbol	Parameter	Conditions	-40 °C to		0 °C to +85 °C		-40 °C to +125 °C	
			Min	Typ [1]	Max	Min	Max	
V_{T+}	positive-going	see Fig. 5 and Fig. 6						
	threshold voltage	V _{CC} = 1.8 V	0.70	1.10	1.50	0.70	1.70	V
		V _{CC} = 2.3 V	1.00	1.40	1.80	1.00	2.00	V
		V _{CC} = 3.0 V	1.30	1.76	2.20	1.30	2.40	V
		V _{CC} = 4.5 V	1.90	2.47	3.10	1.90	3.30	V
		V _{CC} = 5.5 V	2.20	2.91	3.60	2.20	3.80	V

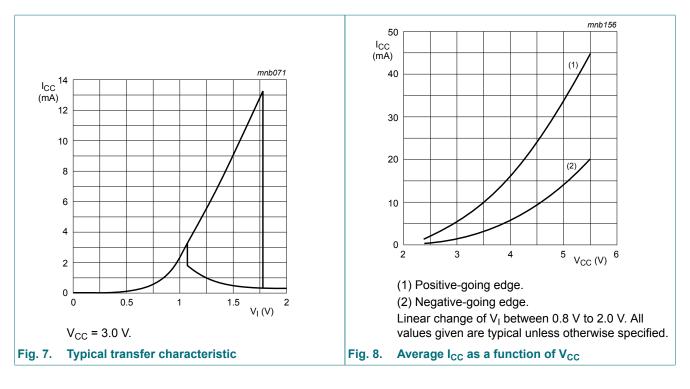
^[2] These typical values are measured at V_{CC} = 3.3 V.

Symbol	Parameter	Conditions	-40	0 °C to +85	°C	-40 °C to	Unit	
			Min	Typ [1]	Max	Min	Max	
V _{T-}	negative-going	see Fig. 5 and Fig. 6						
	threshold voltage	V _{CC} = 1.8 V	0.25	0.61	0.90	0.25	1.10	V
		V _{CC} = 2.3 V	0.40	0.80	1.15	0.40	1.35	V
		V _{CC} = 3.0 V	0.60	1.04	1.50	0.60	1.70	V
		V _{CC} = 4.5 V	1.00	1.55	2.00	1.00	2.20	V
		V _{CC} = 5.5 V	1.20	1.86	2.30	1.20	2.50	V
V _H	hysteresis voltage	$(V_{T+} - V_{T-})$; see <u>Fig. 5</u> , <u>Fig. 6</u> and <u>Fig. 7</u>						
		V _{CC} = 1.8 V	0.15	0.49	1.00	0.15	1.20	V
		V _{CC} = 2.3 V	0.25	0.60	1.10	0.25	1.30	V
		V _{CC} = 3.0 V	0.40	0.73	1.20	0.40	1.40	V
		V _{CC} = 4.5 V	0.60	0.92	1.50	0.60	1.70	V
		V _{CC} = 5.5 V	0.70	1.02	1.70	0.70	1.90	V

[1] All typical values are measured at T_{amb} = 25 °C.

11.2. Waveforms transfer characteristics





12. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40	°C to +85	°C	-40 °C to	+125 °C	Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation	nA to nY; see Fig. 9 [2]						
	delay	V _{CC} = 1.65 V to 1.95 V	1.5	5.6	10.5	1.5	13.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.7	6.5	1.0	8.5	ns
		V _{CC} = 2.7 V	1.0	3.8	6.5	1.0	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.6	5.7	1.0	7.1	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	2.7	4.3	1.0	5.4	ns
C _{PD}	power dissipation capacitance	per buffer; $V_{CC} = 3.3 \text{ V}$; [3] $V_I = \text{GND to } V_{CC}$	-	16.3	-	-	-	pF

- Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_0 = output frequency in MHz;

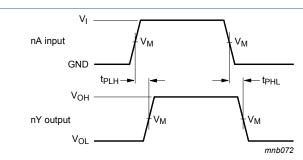
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$ = sum of outputs.

12.1. Waveforms and test circuit



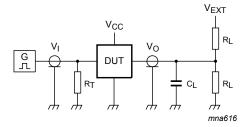
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 9. The input (nA) to output (nY) propagation delays and the output transition times

Table 10. Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_{T} = Termination resistance should be equal to output impedance Z_{o} of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	voltage Input		Load	Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	CL	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	2 × V _{CC}	
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	2 × V _{CC}	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	2 × V _{CC}	

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

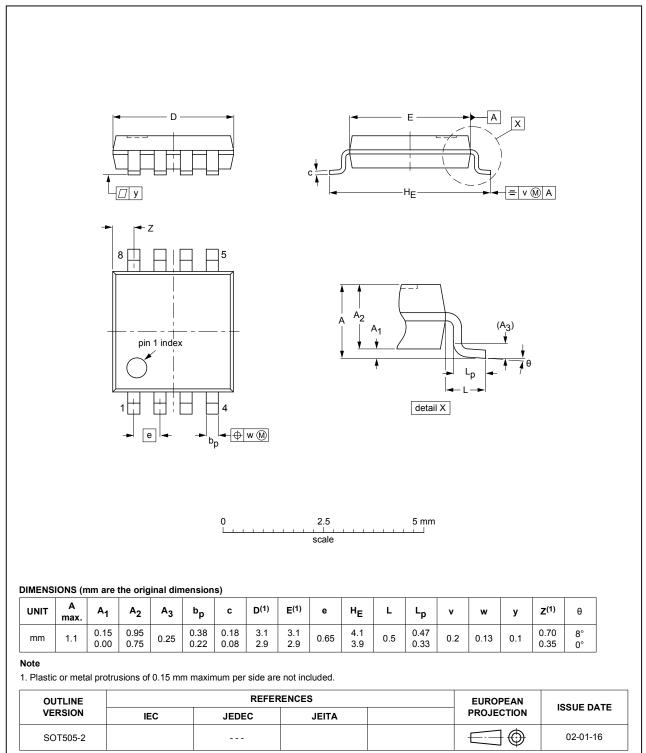


Fig. 11. Package outline SOT505-2 (TSSOP8)

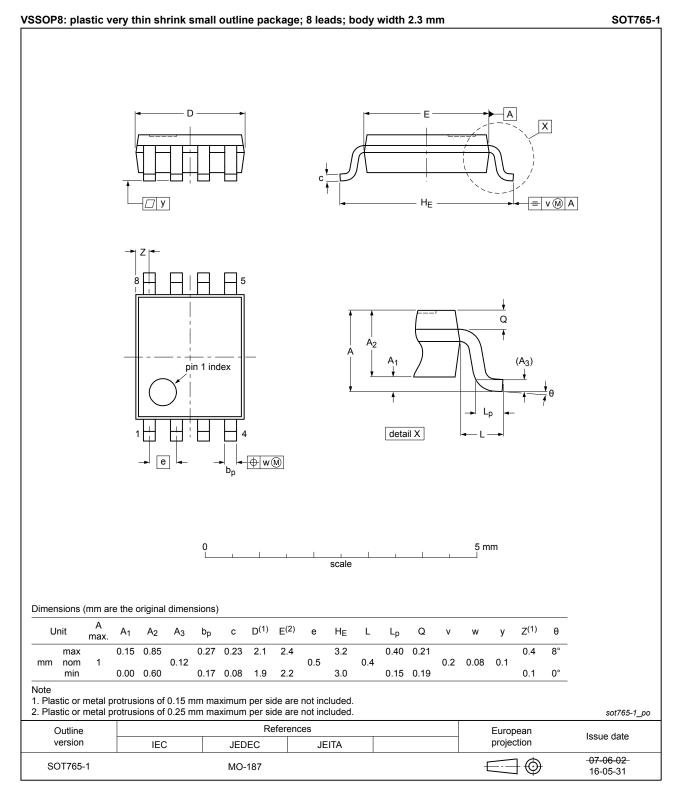


Fig. 12. Package outline SOT765-1 (VSSOP8)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVC3G17_Q100 v.3	20181127	Product data sheet	-	74LVC3G17_Q100 v.2		
Modifications:	of Nexperia	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 				
74LVC3G17_Q100 v.2	20161214	Product data sheet	-	74LVC3G17_Q100 v.1		
Modifications:	• <u>Table 7</u> : The	<u>Table 7</u> : The maximum limits for leakage current and supply current have changed.				
74LVC3G17_Q100 v.1	20140522	Product data sheet	-	-		

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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