74VHC32-Q100; 74VHCT32-Q100 Quad 2-input OR gate

Rev. 1 — 20 December 2013

Product data sheet

1. General description

The 74VHC32-Q100; 74VHCT32-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7-A.

The 74VHC32-Q100; 74VHCT32-Q100 provide the 2-input OR function.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

Features and benefits 2.

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ The 74VHC32-Q100 operates with CMOS input level
 - The 74VHCT32-Q100 operates with TTL input level
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - ♦ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- Multiple package options

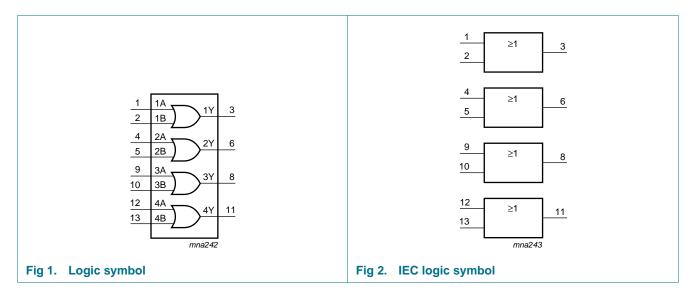


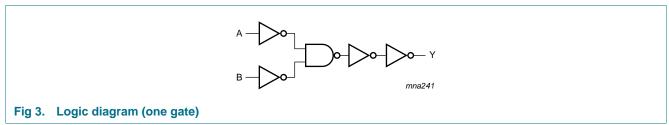
3. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range Name		Description	Version					
74VHC32D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1					
74VHCT32D-Q100			body width 3.9 mm						
74VHC32PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package;	SOT402-1					
74VHCT32PW-Q100			14 leads; body width 4.4 mm						
74VHC32BQ-Q100	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced	SOT762-1					
74VHCT32BQ-Q100			very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm						

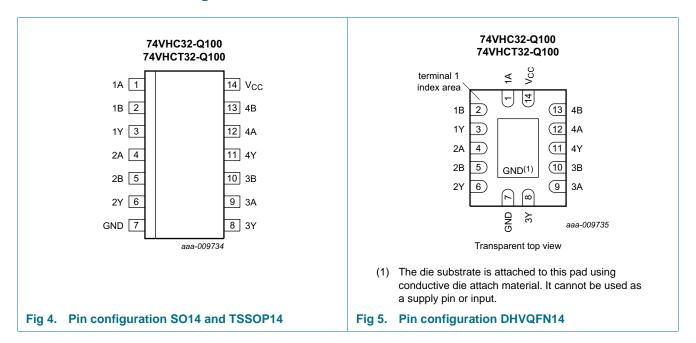
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

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Symbol	Pin	Description
1A	1	data input
1B	2	data input
1Y	3	data output
2A	4	data input
2B	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3B	10	data input
4Y	11	data output
4A	12	data input
4B	13	data input
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input	Output	
nA	nB	nY
L	L	L
X	Н	Н
Н	X	Н

^[1] H = HIGH voltage level;

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

		, ,			,
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_{I}	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 \text{ V}$	<u>[1]</u> –20	-	mA
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{CC} + 0.5 V	<u>[1]</u> –20	+20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		−75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] -	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74VHC3	2-Q100					
V _{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

74VHC_VHCT32_Q100

L = LOW voltage level;

X = don't care.

^[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K. For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K. For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

 Table 5.
 Operating conditions ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74VHCT	32-Q100					
V_{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74VHC3	2-Q100				ı					
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
	V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V	
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
OH	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -50 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -50 \mu A; V_{CC} = 3.0 V$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_{O} = -50 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
cc	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74VHCT	32-Q100					1	1		1	
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
output voltage	$I_{O} = -50 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V	
		$I_0 = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		Ι _Ο = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Δl _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

 Table 7.
 Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see <u>Figure 7</u>.

•		10 //		,							
Symbol	Parameter	Conditions		25 °C -		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
				Min	Typ[1]	Max	Min	Max	Min	Max	
74VHC3	2-Q100										
t _{pd}	propagation	nA, nB to nY; see Figure 6	[2]								
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		C _L = 15 pF		-	3.9	7.9	1.0	9.5	1.0	10.0	ns
		C _L = 50 pF		-	5.6	11.4	1.0	13	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	2.8	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF		-	4.1	7.5	1.0	8.5	1.0	9.5	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[3]	-	10	-	-	-	-	-	pF

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 7.

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			I	Min	Typ[1]	Max	Min	Max	Min	Max	
74VHCT32-Q100; V _{CC} = 4.5 V to 5.5 V											
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[2]								
		C _L = 15 pF		-	3.1	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF		-	4.3	7.9	1.0	9.0	1.0	10.0	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	[3]	-	12	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

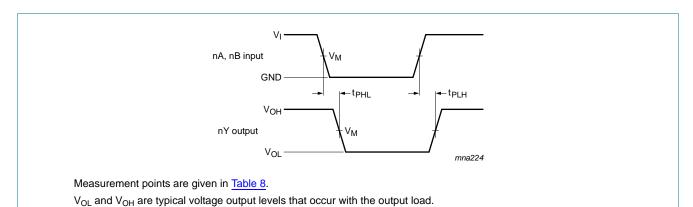
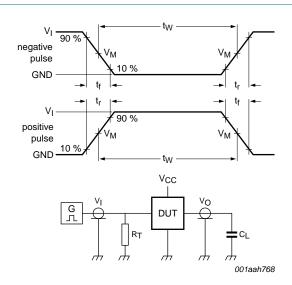


Fig 6. Input to output propagation delays

Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74VHC32-Q100	0.5V _{CC}	0.5V _{CC}
74VHCT32-Q100	1.5 V	0.5V _{CC}

74VHC_VHCT32_Q100



Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

 C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

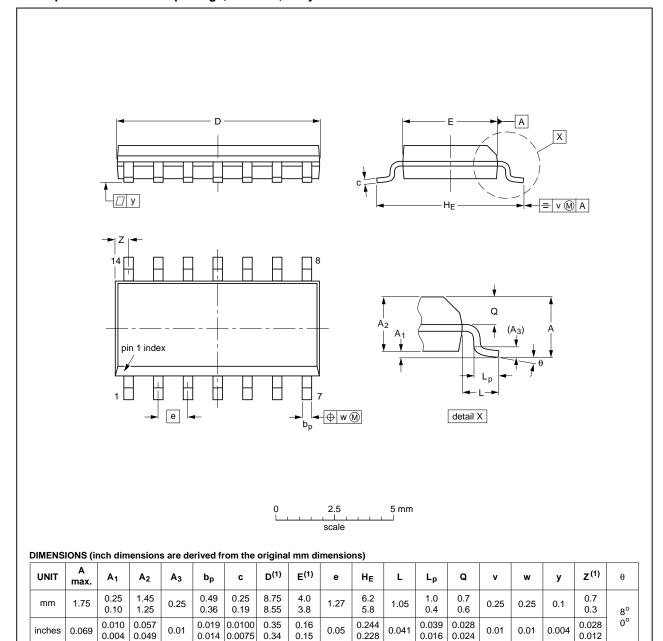
Table 9. Test data

Туре	Input		Load	Test
	V _I	t _r , t _f	CL	
74VHC32-Q100	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74VHCT32-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE REFERENCES					EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

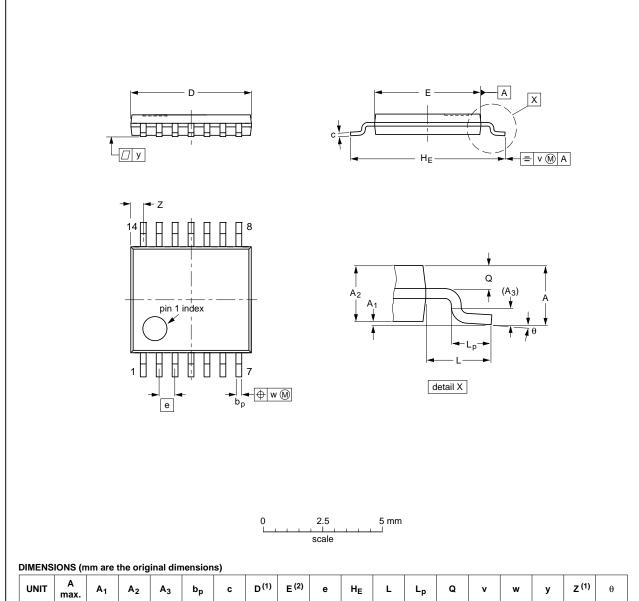
Package outline SOT108-1 (SO14)

74VHC VHCT32 Q100

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E (2)	e	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION		ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Package outline SOT402-1 (TSSOP14)

74VHC_VHCT32_Q100

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

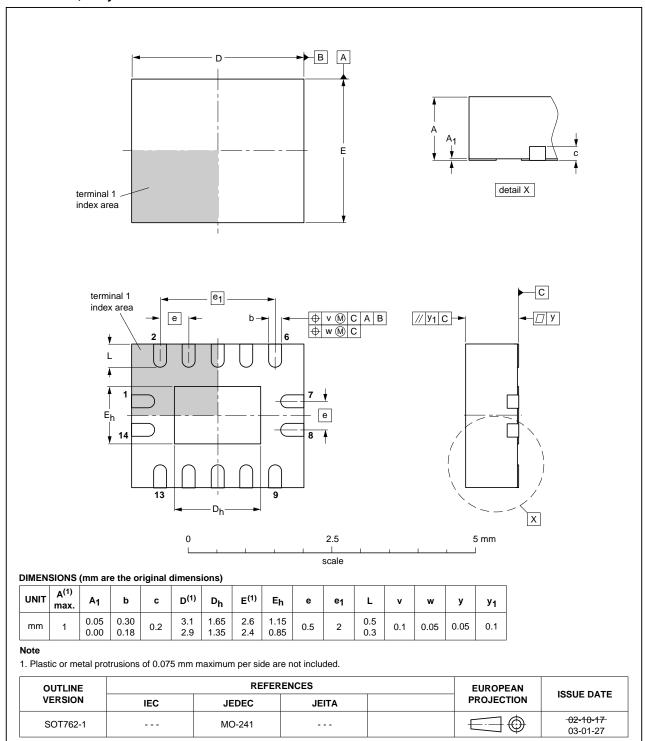


Fig 10. Package outline SOT762-1 (DHVQFN14)

74VHC_VHCT32_Q100

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MIL	Military
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT32_Q100 v.1	20131220	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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74VHC_VHCT32_Q100

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