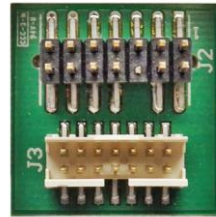


FEATURES

- MityDSP-L138 Family Debug Adapter
- DSP/ARM and FPGA debug interfaces
- Compatible Critical Link System on Modules
 - MityDSP-L138
 - MityDSP-L138F
 - MityARM-1808
 - MityARM-1808F
 - MityARM-1810
 - MityARM-1810F
 - MityDSP-6748F



Top



Bottom

DESCRIPTION

The L138/1808/1810/6748 Debug Adapter board for the MityDSP-L138 Family of System on Modules from Critical Link allows for access to the DSP, ARM and FPGA (module dependent) debug interfaces. Each compatible System on Module includes a 31-pin Hirose connector which this adapter board connects to.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Storage Temperature Range -40°C to 80°C

OPERATING CONDITIONS

Ambient Temperature 0°C to 70°C
 Range Commercial

Humidity 0 to 95%
 Non-condensing

DEBUG INTERFACE

A Hirose 31 pin connector (DF9-31P-1V(32)) is provided on each compatible module to allow for the connection of this adapter board for both FPGA and OMAP-L138 processor debug. Below is the pin-out for the Hirose connector and the debug connectors on the adapter board. This adapter is available through your Critical Link representative; please see the ordering information, Table 4, below.

Debug Interface Connector Description (J1)

Table 1 OMAP-L138 Hirose Connector

| Pin | I/O | Signal | Pin | I/O | Signal |
|-----|-----|--------|-----|-----|-------------------------|
| 1 | - | GND | 2 | O | OMAP EMU1 |
| 3 | - | GND | 4 | O | OMAP EMU0 |
| 5 | - | GND | 6 | I | OMAP TCK |
| 7 | - | GND | 8 | O | OMAP RTCK |
| 9 | - | GND | 10 | O | OMAP TDO |
| 11 | - | GND | 12 | - | OMAP VCC / 3.3V |
| 13 | - | GND | 14 | I | OMAP TDI |
| 15 | - | GND | 16 | I | OMAP TRST |
| 17 | - | GND | 18 | I | OMAP TMS |
| 19 | - | GND | 20 | - | GND |
| 21 | - | GND | 22 | O | NC / FPGA VREF / VCCAUX |
| 23 | - | GND | 24 | I | NC / FPGA TMS |
| 25 | - | GND | 26 | I | NC / FPGA TCK |
| 27 | - | GND | 28 | O | NC / FPGA TDO |
| 29 | - | GND | 30 | I | NC / FPGA TDI |
| 31 | - | GND | | | |

Processor JTAG Interface Description (J2)

Connection for the processor, L138/1808/1810/6748, JTAG and emulator interfaces of a compatible System on Module from Critical Link.

Table 2 OMAP-L138 JTAG Connector Pad

| Pin | I/O | Signal | Pin | I/O | Signal |
|-----|-----|-----------------|-----|-----|-----------|
| 1 | I | OMAP TMS | 2 | I | OMAP TRST |
| 3 | I | OMAP TDI | 4 | - | GND |
| 5 | - | OMAP VCC / 3.3V | 6 | - | KEY |
| 7 | O | OMAP TDO | 8 | - | GND |
| 9 | O | OMAP RTCK | 10 | - | GND |
| 11 | I | OMAP TCK | 12 | - | GND |
| 13 | O | OMAP EMU0 | 14 | O | OMAP EMU1 |

FPGA JTAG Interface Description (J3)

Connection for Xilinx FPGA JTAG interface of a compatible System on Module from Critical Link.

Table 3 FPGA JTAG Connector Pad

| Pin | I/O | Signal | Pin | I/O | Signal |
|-----|-----|--------|-----|-----|--------------------|
| 1 | - | GND | 2 | O | FPGA VREF / VCCAUX |
| 3 | - | GND | 4 | I | FPGA TMS |
| 5 | - | GND | 6 | I | FPGA TCK |
| 7 | - | GND | 8 | O | FPGA TDO |
| 9 | - | GND | 10 | I | FPGA TDI |
| 11 | - | GND | 12 | - | No Connect |
| 13 | - | GND | 14 | - | No Connect |

ORDERING INFORMATION

The following table lists the standard debug adapter ordering information. For shipping status, availability, and lead time please contact your Critical Link representative.

Table 4: Standard Debug Adapter Part Number

| Part Number | Description |
|-------------|--|
| 80-000286 | L138/1808/1810/6748 JTAG Debug Adapter |