Description

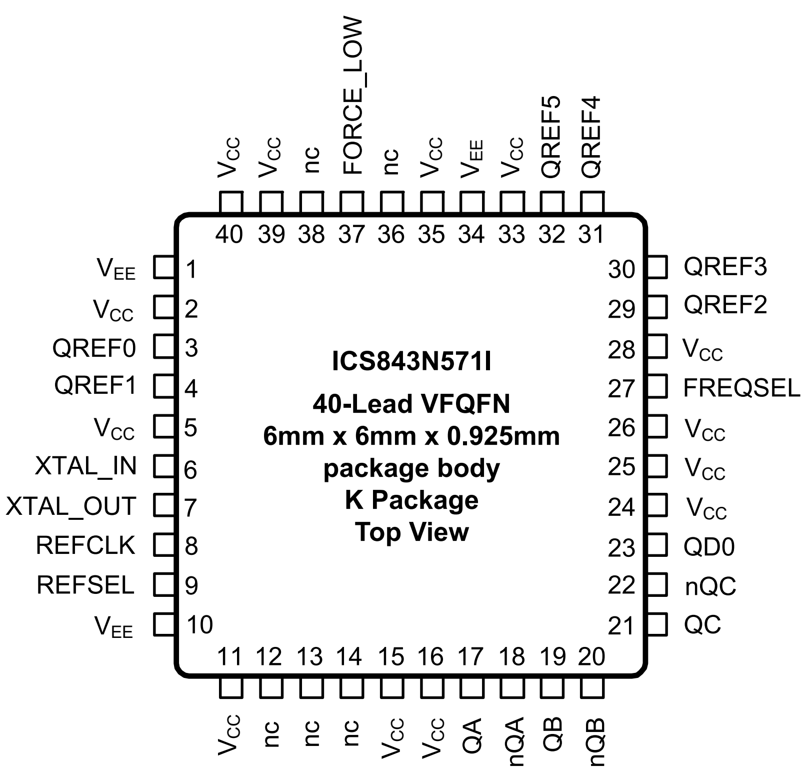
The 843N571I is a PLL based clock synthesizer for use in Ethernet applications. The device uses IDT's fourth generation FemtoClock® NG technology for optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. Using IDT's latest FemtoClock NG PLL technology, the 843N571I achieves <0.3ps RMS phase jitter performance.

843N571I can synthesize 100MHz, 125MHz, 156.25MHz and a low frequency 33.33MHz CPU clock from a single device. Six LVCMOS outputs also serve as additional buffering of the 25MHz crystal reference.

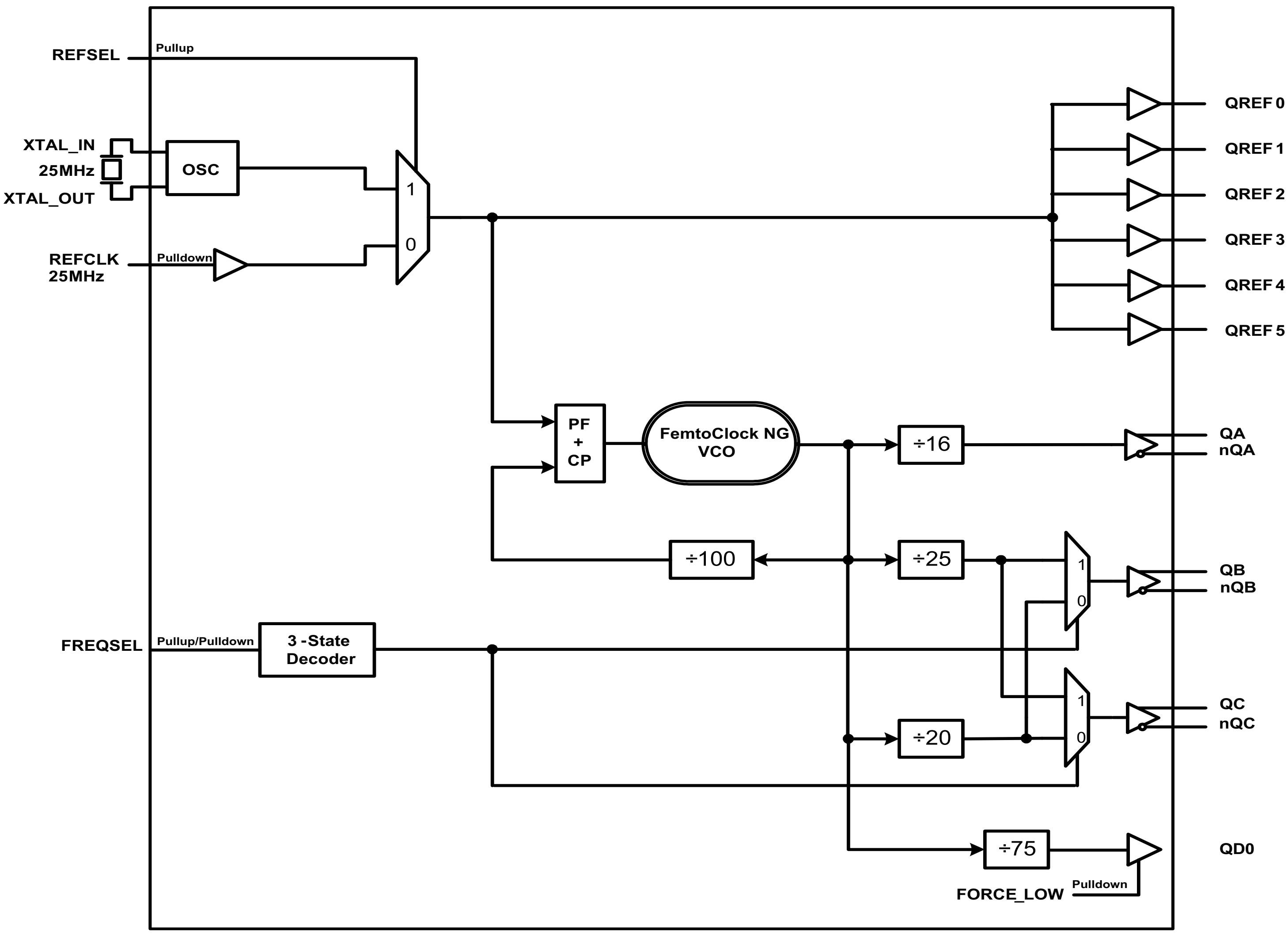
Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- Seven single-ended LVCMOS outputs, 30Ω output impedance
- Three LVPECL output pairs
  One differential LVPECL (QA, nQA) output pair: 156.25MHz
  Two selectable differential LVPECL output pairs (QB, nQB and QC, nQC): 100MHz and 125MHz
- One single-ended LVCMOS (QD0) 33.33MHz CPU clock
- Selectable external crystal or single-ended input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- FemtoClock NG frequency multiplier provides low jitter, high frequency output
- FemtoClock NG VCO frequency: 2.5GHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.283ps (typical)
- Power supply noise rejection PSNR: -80dB
- 3.3V supply voltage
- -40C to 85C ambient operating temperature
- Lead-free (RoHS 6) packaging

Pin Assignment



Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 10, 34	V_{EE}	Power		Negative supply pins.
2, 5, 11, 15, 16, 24, 25, 26, 28, 33, 35, 39, 40	V_{CC}	Power		Power supply pins. Pins 2, 28, 33 – power supply connection for the 25MHz LVCMOS outputs Pin 5 – power supply connection for the crystal oscillator Pins 11, 15, 26, 35 – power supply connection for the dividers and other core circuitry Pin 16 (vposO) – power supply connection for the differential LVPECL outputs Pin 24, 25 – power supply connection for the 33MHz LVCMOS output Pin 39 – power supply connection for the digital logic Pin 40 – power supply connection for the PLL
3, 4, 29, 30, 31, 32	QREF0, QREF1, QREF2, QREF3, QREF4, QREF5	Output		Single-ended outputs. 3.3V LVCMOS/LVTTL reference levels.
6, 7	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
8	REFCLK	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
9	REFSEL	Input	Pullup	Reference select pin. When HIGH, selects crystal. When LOW, selects REFCLK. See Table 3A. LVCMOS/LVTTL interface levels.
12, 13, 14, 36, 38	nc			No connect.
17, 18	QA, nQA	Output		Differential output pair. LVPECL interface levels.
19, 20	QB, nQB	Output		Differential output pair. LVPECL interface levels.
21, 22	QC, nQC	Output		Differential output pair. LVPECL interface levels.
23	QD0	Output		Single-ended output. 3.3V LVCMOS/LVTTL reference levels.
27	FREQSEL	Input	Pullup/ Pulldown	Frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.
37	FORCE_LOW	Input	Pulldown	Forces the QD0 output into a low state. See Table 3C. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		Crystal Not Included		2		pF
C_{PD}	Power Dissipation Capacitance (per output)	QD0, QREF[0:5]	V_{CC} = 3.6V		6		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QD0, QREF[0:5]			30		Ω

Function Tables

Table 3A. REFSEL Function Table

Inputs	Input Source
REFSEL	
0	REFCLK
1 (default)	XTAL_IN, XTAL_OUT

Table 3C. FORCE_LOW Function Table

Inputs	Output Frequency (MHz)
FORCE_LOW	QD0
0 (default)	33.33
1	Disabled

Table 3B. FREQSEL Function Table

Inputs	Output Frequency (MHz)	
FREQSEL	QB, nQB	QC, nQC
0	125	125
1	100	100
Float (default)	125	100

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{CC} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	37.7°C/W (0 mps)
Maximum Junction Temperature, $T_{J,MAX}$	150°C
Storage Temperature, T_{STG}	-65°C to 150°C

Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C

NOTE 1: It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.
NOTE 2: All conditions in the table must be met to guarantee device functionality.
NOTE 3: The device is verified to the maximum operating junction temperature through simulation.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current	No Load			250	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	REFSEL, FORCE_LOW		2		V_{CC} + 0.3	V
		FREQSEL		V_{CC} - 0.4			V
V_{IL}	Input Low Voltage	REFSEL, FORCE_LOW		-0.3		0.8	V
		FREQSEL				0.4	V
V_{IM}	Input Medium Voltage	FREQSEL		$V_{CC}/2$ - 0.1		$V_{CC}/2$ + 0.1	V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REFCLK, FREQSEL, FORCE_LOW	$V_{CC} = V_{IN} = 3.6V$			150	µA
		REFSEL	$V_{CC} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	REFCLK, FORCE_LOW	$V_{CC} = 3.6V, V_{IN} = 0V$	-5			µA
		REFSEL, FREQSEL	$V_{CC} = 3.6V, V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} = 3.3V \pm 0.3V$	2.3			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} = 3.3V \pm 0.3V$			0.8	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 4C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} – 1.4$		$V_{CC} – 0.8$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} – 2.0$		$V_{CC} – 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC} – 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. LVPECL AC Characteristics, $V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency			25		MHz
f_{OUT}	Output Frequency		100		156.25	MHz

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
tjit(θ)	RMS Phase Jitter (Random) NOTE 1		156.25MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 20MHz		0.233		ps
			125MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 20MHz		0.283		ps
			100MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 20MHz		0.299		ps
*t*sk(o)	Output Skew; NOTE 2, 3		Measured on the Rising Edge			40	ps
PSNR	Power Supply Noise Reduction	Pin 40 (V_{CC})	From DC to 8MHz, FORCE_LOW = HIGH		-75		dB
		Pin 40 (V_{CC})	From DC to 3MHz, FORCE_LOW = LOW		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		550	ps
odc	Output Duty Cycle			48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

Table 6B. AC Characteristics for Single Side Band Power Levels (LVPECL Outputs),
V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V, T_A = 25°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	156.25MHz, 33.33MHz Output disabled		-120		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier			-132		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier			-135		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier			-140		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier			-156		dBc/Hz
Φ_N(20M)	Single-side band phase noise, 20MHz from Carrier			-157		dBc/Hz

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	125MHz, 33.33MHz Output disabled		-121		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier			-133		dBc/Hz
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier			-137		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier			-143		dBc/Hz
$\Phi_N(10M)$	Single-side band phase noise, 10MHz from Carrier			-153		dBc/Hz
$\Phi_N(20M)$	Single-side band phase noise, 20MHz from Carrier			-153		dBc/Hz
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	100MHz, 33.33MHz Output disabled		-123		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier			-135		dBc/Hz
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier			-139		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier			-145		dBc/Hz
$\Phi_N(10M)$	Single-side band phase noise, 10MHz from Carrier			-154		dBc/Hz
$\Phi_N(20M)$	Single-side band phase noise, 20MHz from Carrier			-154		dBc/Hz

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 6C. LVCMOS AC Characteristics, V_{CC} = 3.3V ± 0.3V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency				25		MHz
f_{OUT}	Output Frequency			25		33.33	MHz
$tjit(\theta)$	RMS Phase Jitter (Random) NOTE 1		33.33MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 5MHz		0.266		ps
			25MHz f_{OUT}, 25MHz crystal Integration Range: 12kHz – 5MHz		0.212		ps
*t*sk(o)	Output Skew; NOTE 2, 3	QREF[0:5]	Measured on the Rising Edge			50	ps
PSNR	Power Supply Noise Reduction	Pin 40, (V_{CC})	From DC to 6.25MHz		-80		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		600	ps
odc	Output Duty Cycle			48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions
NOTE 1: Refer to the Phase Noise Plot.

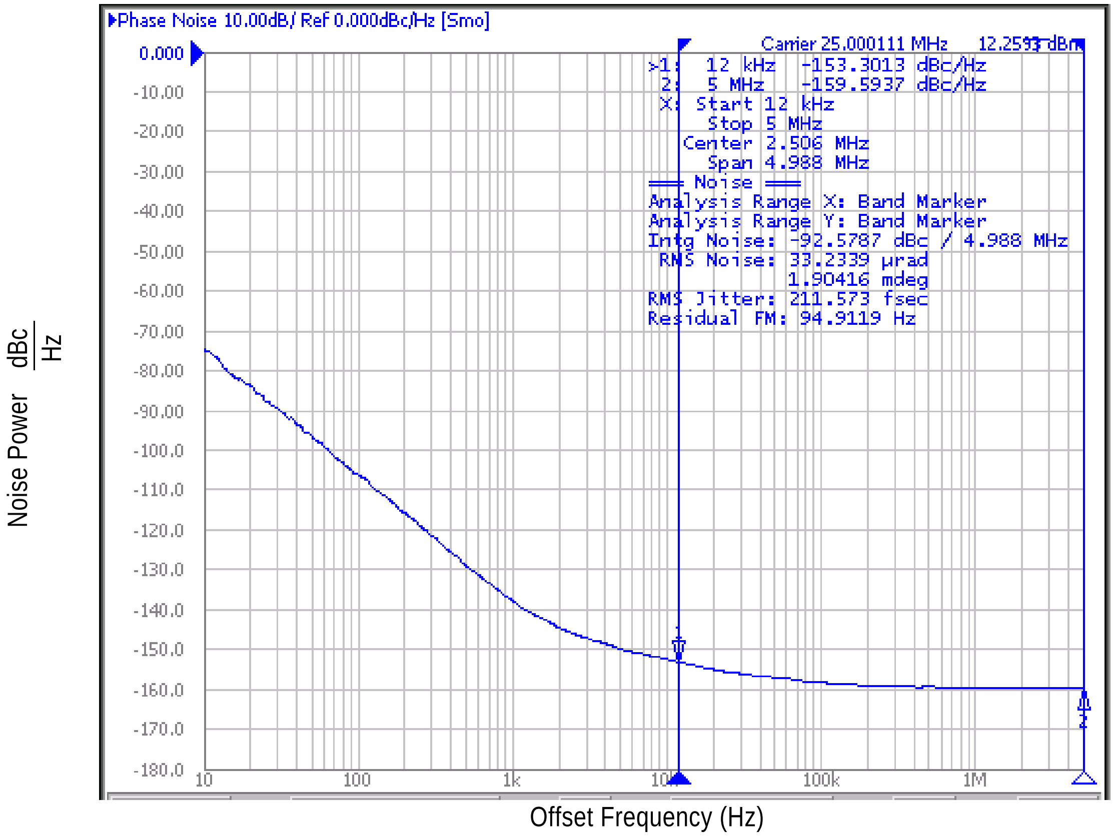
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{CC}/2$.

Table 6D. AC Characteristics for Single Side Band Power Levels (LVCMOS Outputs),
$V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$, $T_A = 25°C$

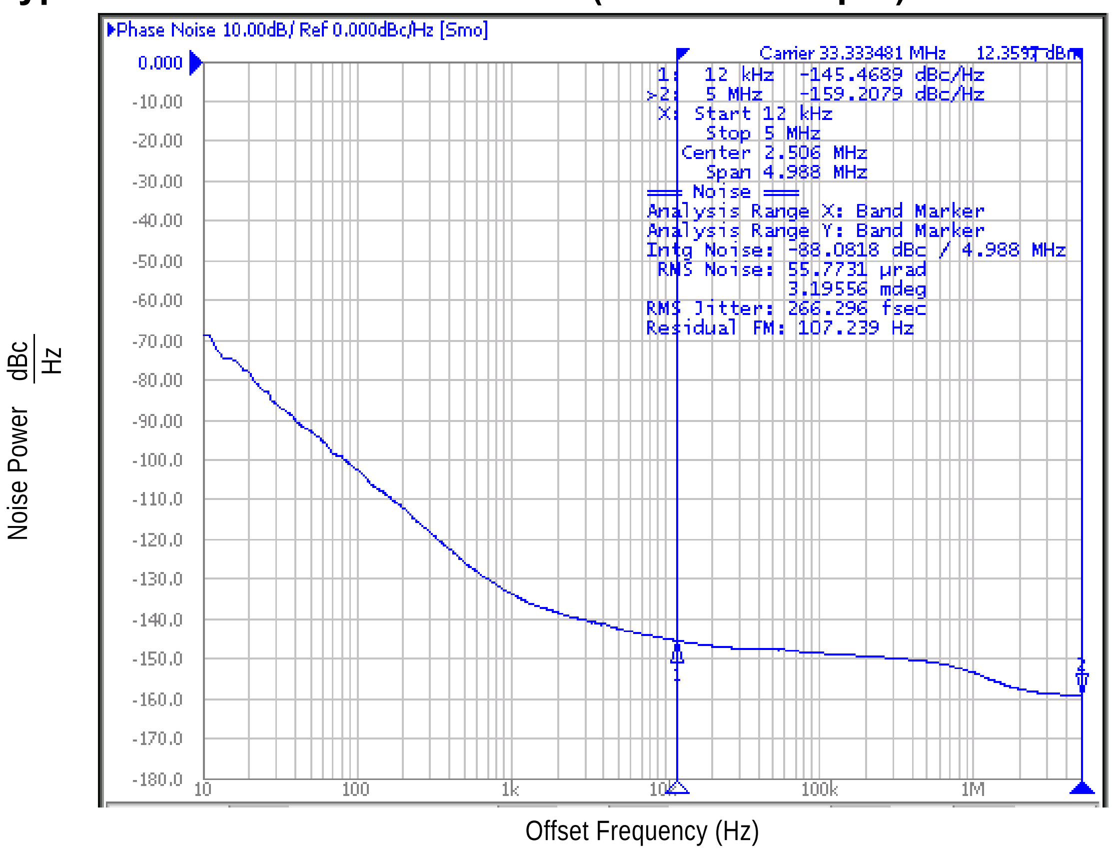
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	33.33MHz		-134		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier			-144		dBc/Hz
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier			-149		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier			-153		dBc/Hz
$\Phi_N(5M)$	Single-side band phase noise, 5MHz from Carrier			-159		dBc/Hz
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	25MHz		-137		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier			-152		dBc/Hz
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier			-158		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier			-160		dBc/Hz
$\Phi_N(5M)$	Single-side band phase noise, 5MHz from Carrier			-160		dBc/Hz

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

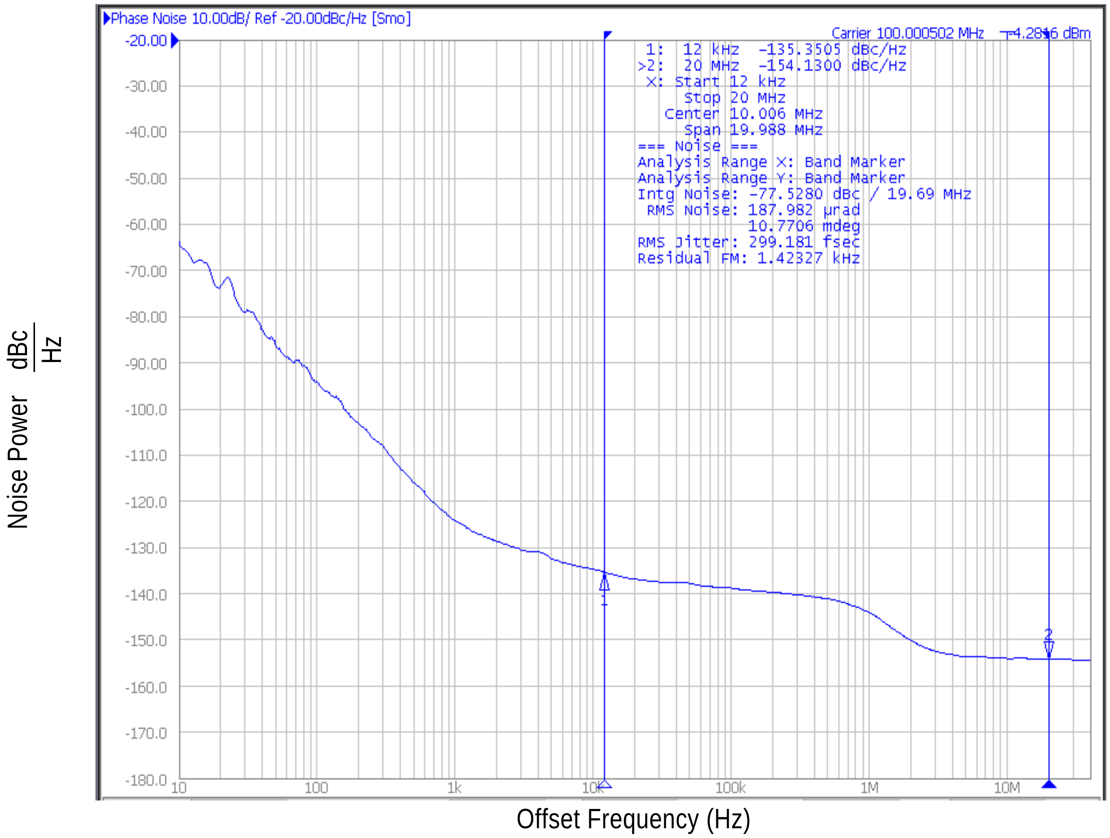
Typical Phase Noise at 25MHz (LVCMOS Output)



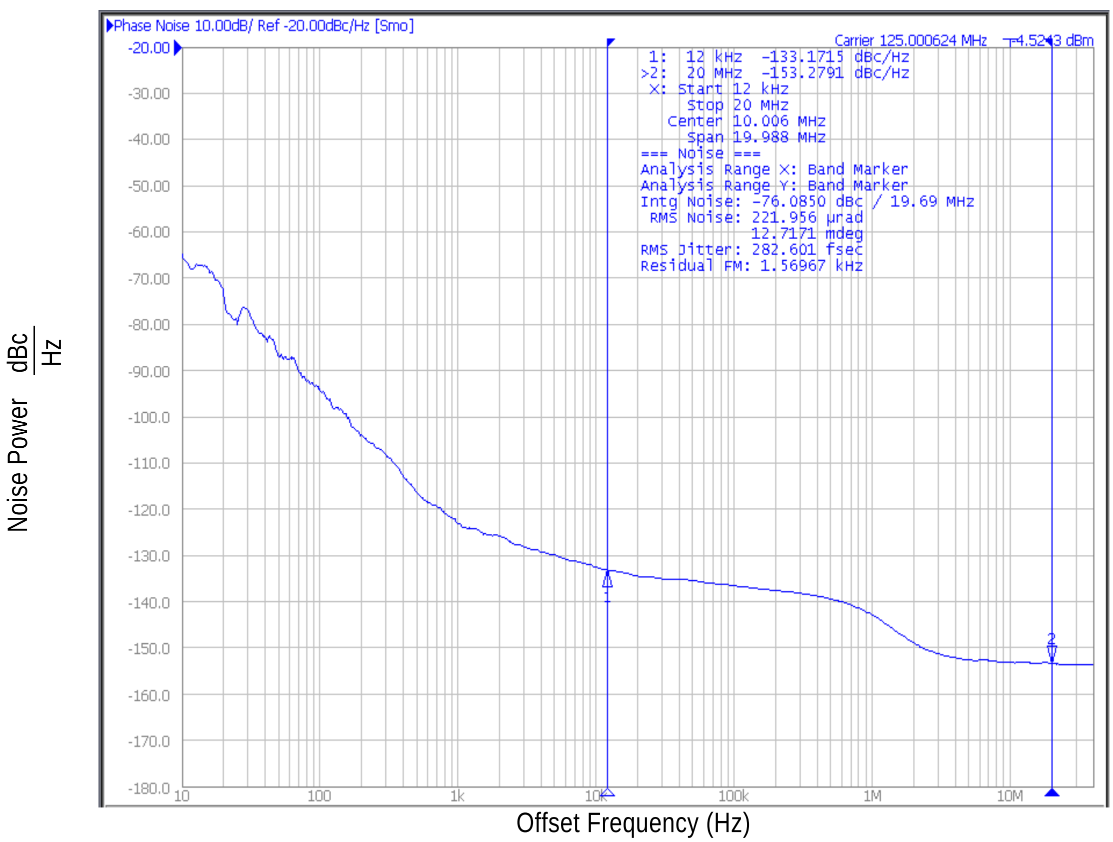
Typical Phase Noise at 33.33MHz (LVCMOS Output)



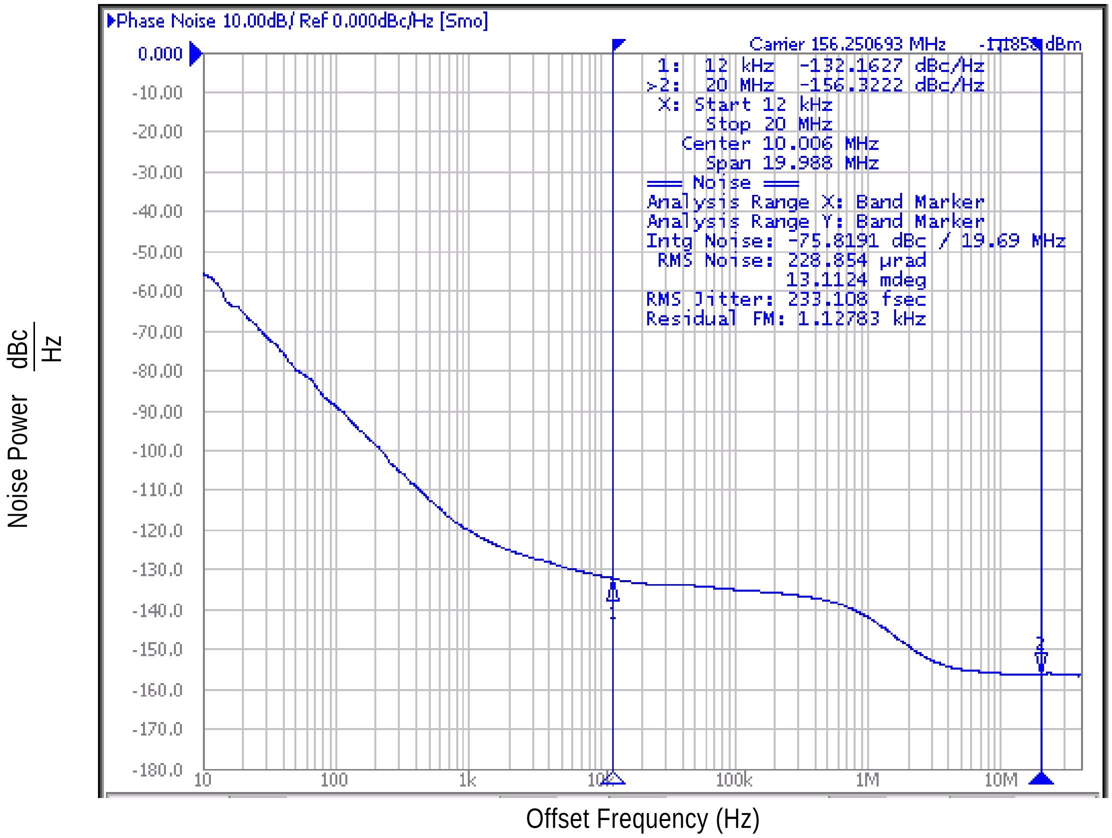
Typical Phase Noise at 100MHz (LVPECL Output)



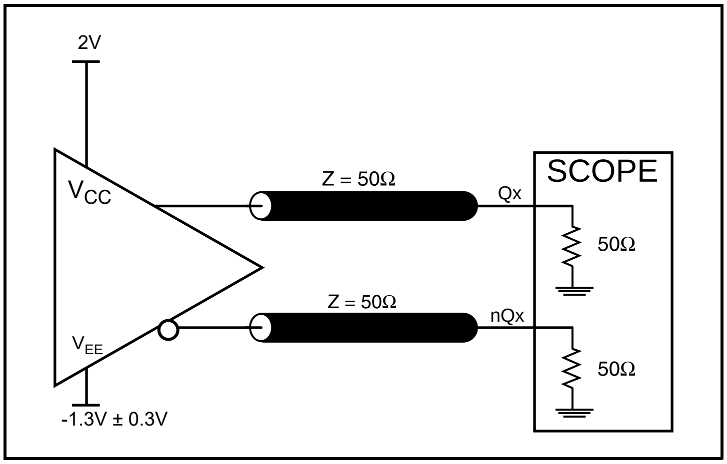
Typical Phase Noise at 125MHz (LVPECL Output)



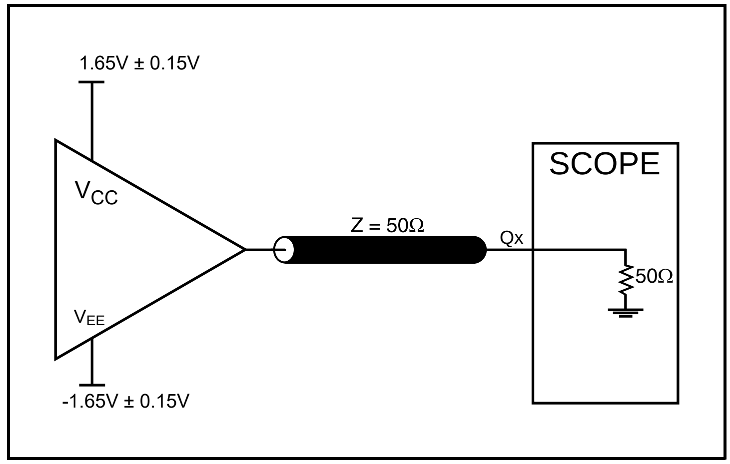
Typical Phase Noise at 156.25MHz (LVPECL Output)



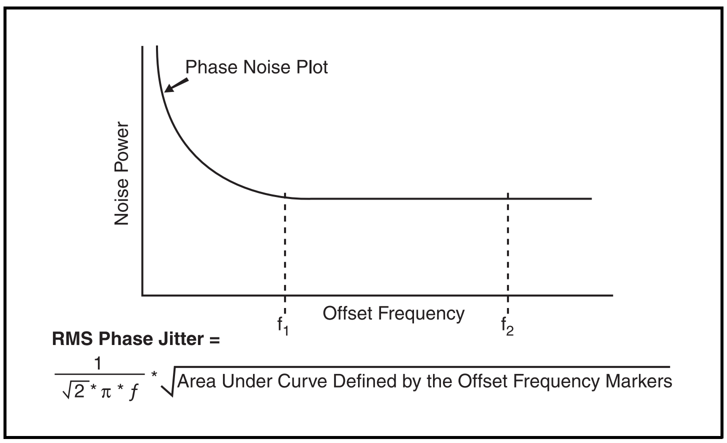
Parameter Measurement Information



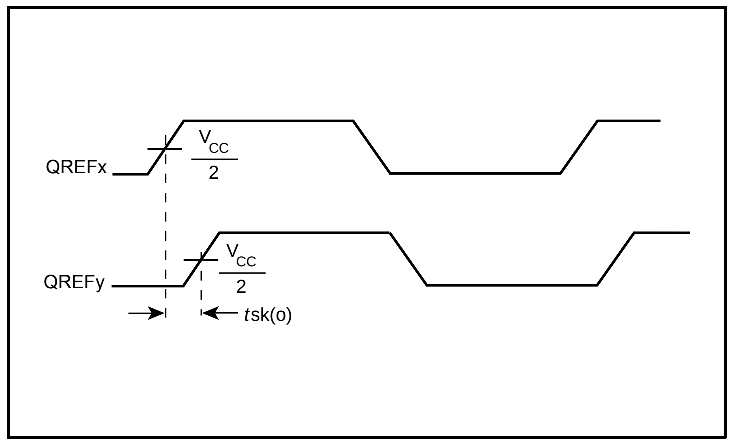
LVPECL Output Load Test Circuit



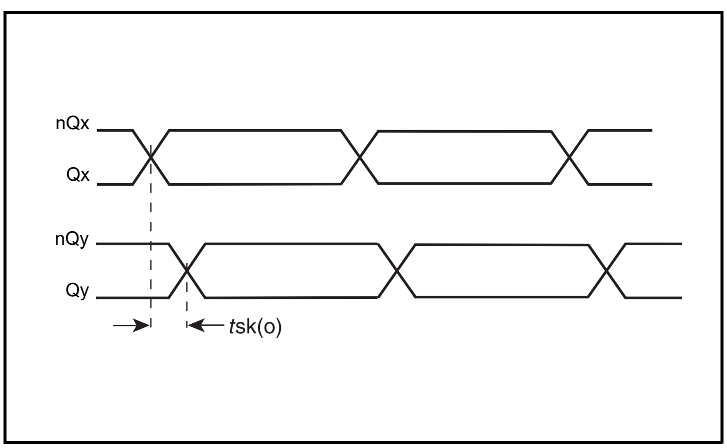
LVCMOS Output Load Test Circuit



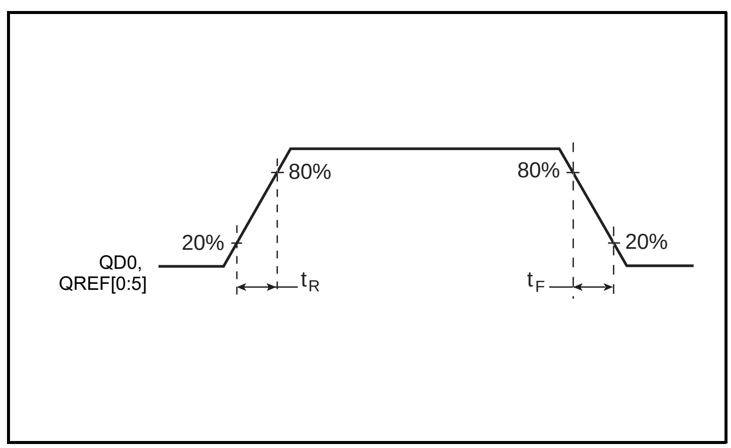
Phase Jitter



LVCMOS Output Skew

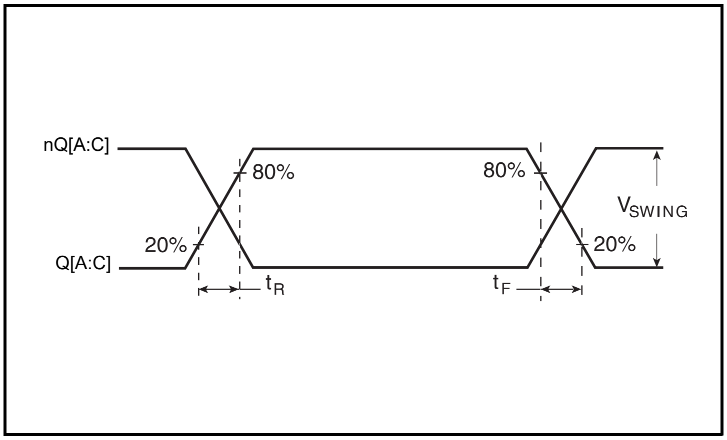


LVPECL Output Skew

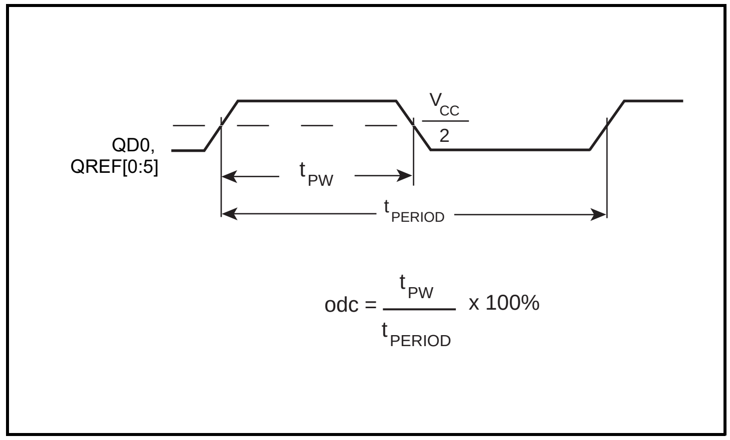


LVCMOS Output Rise/Fall Time

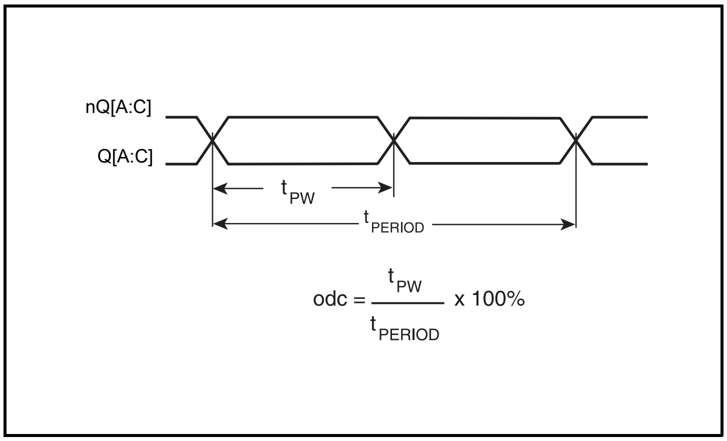
Parameter Measurement Information, continued



LVPECL Output Rise/Fall Time



LVCMOS Output Duty Cycle/Pulse Width/Period



LVPECL Output Duty Cycle/Pulse Width/Period

Applications Information

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

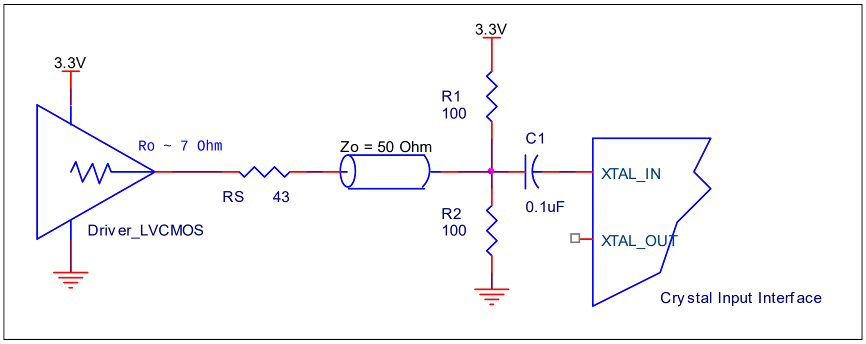


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

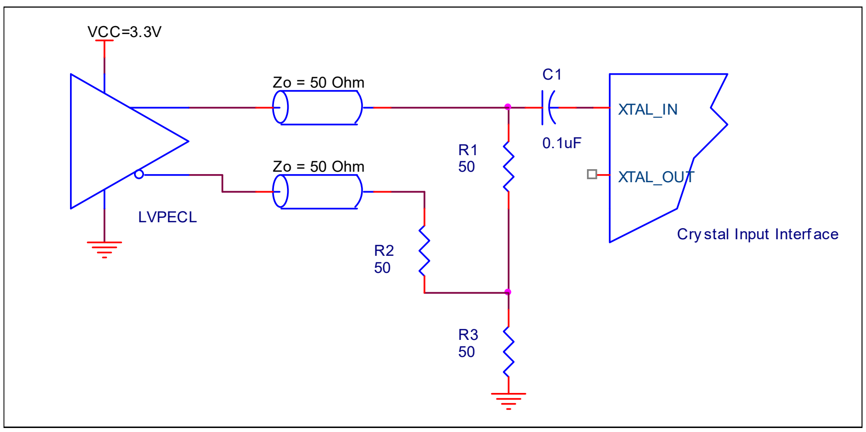


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

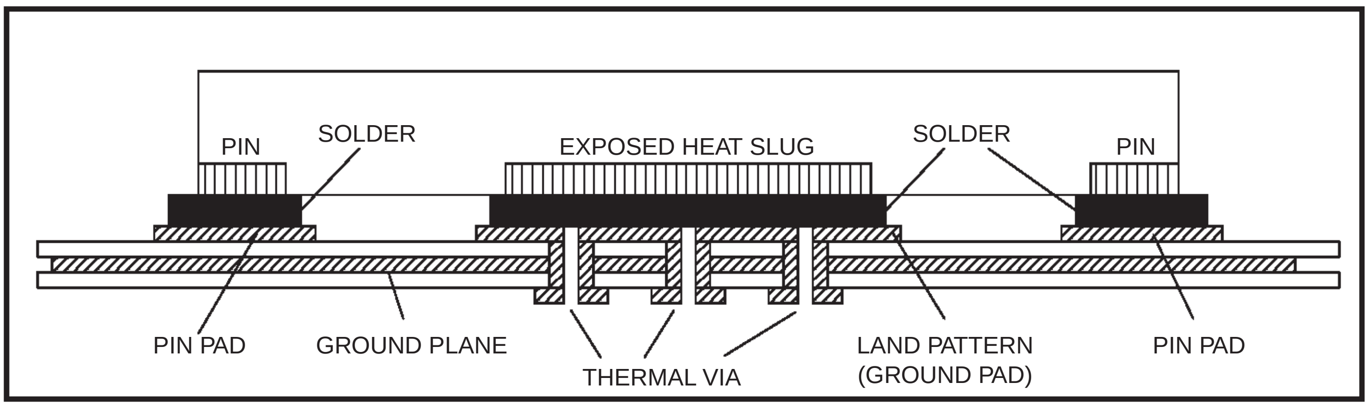


Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

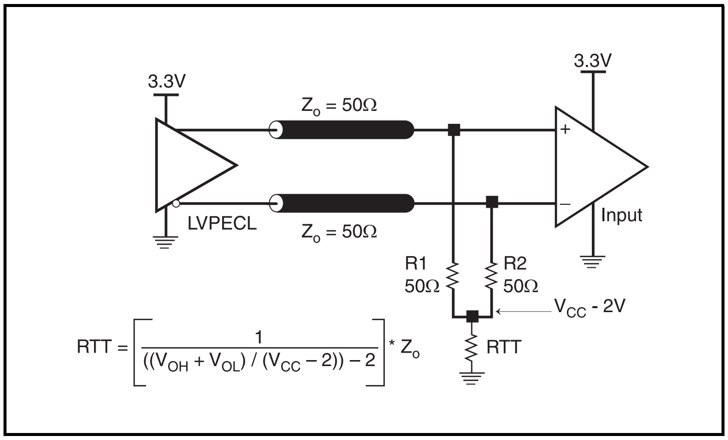


Figure 3A. 3.3V LVPECL Output Termination

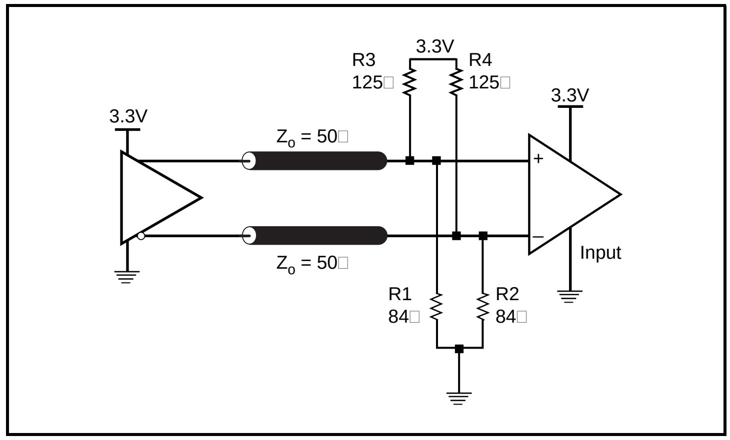


Figure 3B. 3.3V LVPECL Output Termination

Recommendations for Unused Input and Output Pins

Inputs:

REFCLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REFCLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

LVPECL Outputs:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Application Schematic Example

Figure 4 shows an example of 843N571I application schematic. In this example, the device is operated at V_{CC} = 3.3V. An 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 15pF and C2 = 15pF are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might required slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

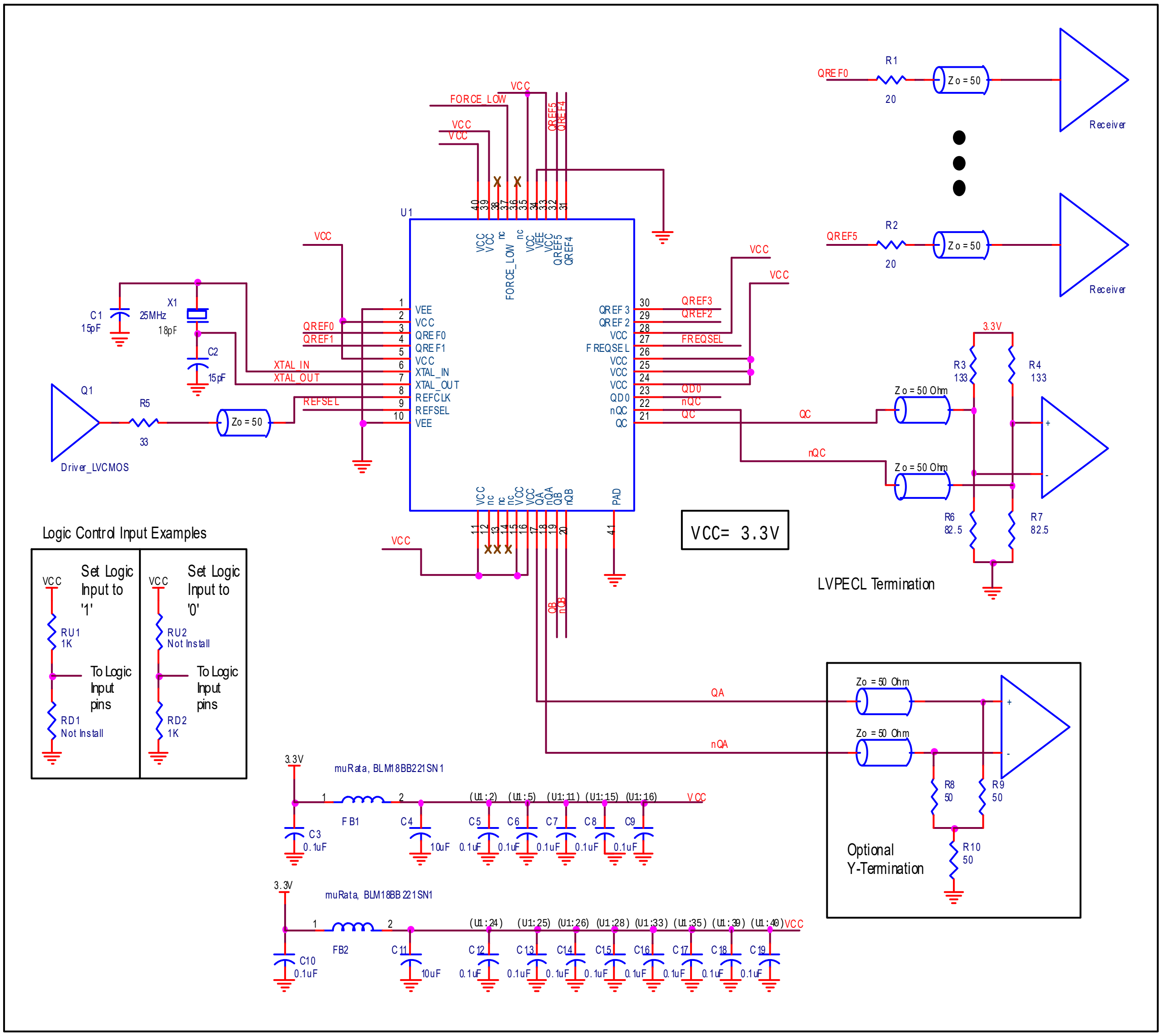


Figure 4. 843N571I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 843N571I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843N571I is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CC} = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

Core and LVPECL Output Power Dissipation

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.6V * 250mA = **900mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 32mW = **96mW**

Dynamic Power Dissipation at 33.3333MHz and 25MHz

Power (33.33MHz) = C_{PD} * Frequency * $(V_{CC})^2$ * # of outputs = 6pF * 33.3333MHz * $(3.6V)^2$ * 1= **2.592mW**
Power (25MHz) = C_{PD} * Frequency * $(V_{CC})^2$ * # of outputs = 6pF * 25MHz * $(3.6V)^2$ * 6 = **11.664mW**

Total Power Dissipation

- **Total Power**

  = Power (Core) + Power (Output) + Dynamic Power (33.3333MHz) + Dynamic Power (25MHz)

  = 900mW + 96mW + 2.592mW + 11.66mW

  = 1010.252mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.010W * 37.7°C/W = 123.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 40 Lead VFQFN Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	31.6°C/W	28.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 5.*

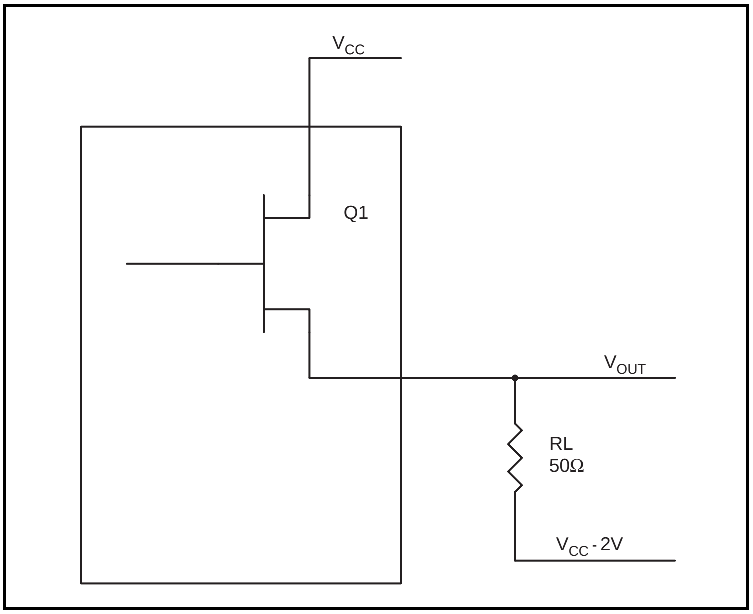


Figure 5. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.8V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) =$ **0.8V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.6V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) =$ **1.6V**
-

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.8V)/50\Omega] * 0.8V =$ **19.2mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.6V)/50\Omega] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 40 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	31.6°C/W	28.8°C/W

Transistor Count

The transistor count for 843N571I is: 22,466

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nlnlg-40-package-outline-60-x-60-mm-body-epad-290-x-290-mm-qfn

Ordering Information

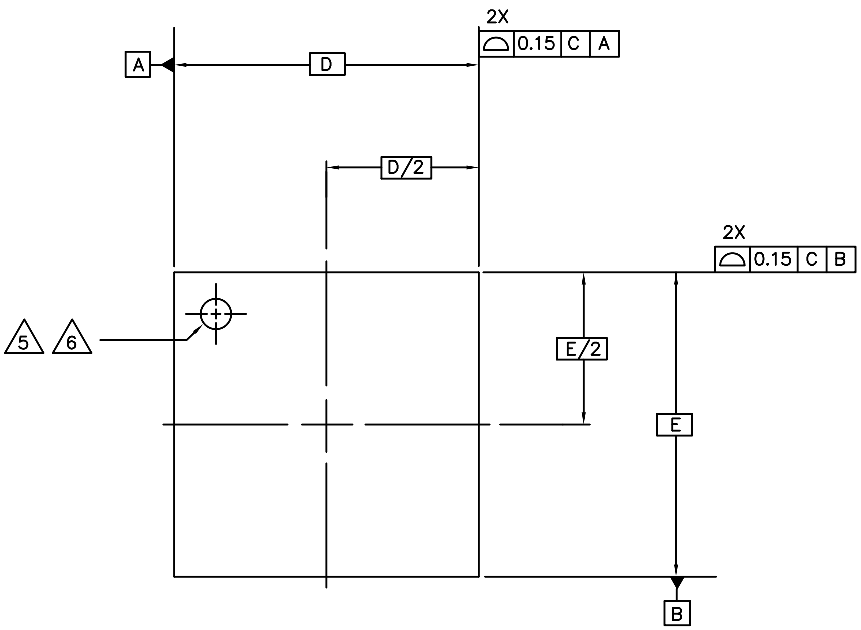
Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843N571BKILF	ICS43N571BIL	"Lead-Free" 40 Lead VFQFN	Tray	-40°C to 85°C
843N571BKILFT	ICS43N571BIL	"Lead-Free" 40 Lead VFQFN	Tape & Reel	-40°C to 85°C

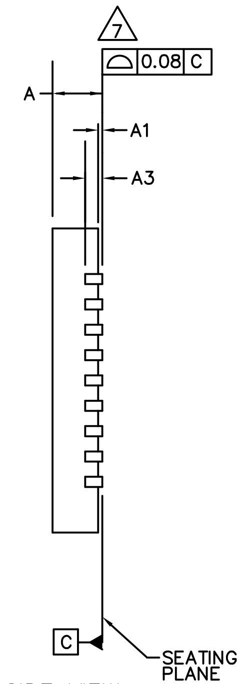
Revision History

Revision Date	Description of Change
November 29, 2018	Updated description of Absolute Maximum Ratings; also added $T_{J,MAX}$ to the table Added Recommended Operating Conditions Updated Package Outline Drawings; however, no technical changes
April 20, 2016	Removed ICS from the part number where needed. Updated data sheet header and footer.
October 4, 2013	PCN #N1302-03_RTB expired.
PCN Expiration Date August 16, 2013	PCN Expiration Period extended to 8/16/2013. Front Page, updated PCN Notification Period. Corrected block diagram. Pin Description Table - showed rest of QREFx pin names. Absolute Maximum Ratings - XTAL_IN input rating, changed from V_{CC} to 2V. LVCMOS DC Characteristics Table - add units to V_{IH}. AC Characteristics Table - changed f_{OUT} min. spec from 25MHz to 100MHz. AC Tables - corrected TA temperature from -25°C to 25°C. Power Considerations - added missing Power Output to Total Power Calculation. Revision History Sheet - changed Date column to the extended PCN date.
May 20, 2013	f_{OUT} Minimum = 100MHz
April 3, 2013	PCN N1302-03 Notification Period Expires 5/28/2013 Part/Order Number: 843N571BKILF, 843N571BKILFT Marking: ICS43N571BIL

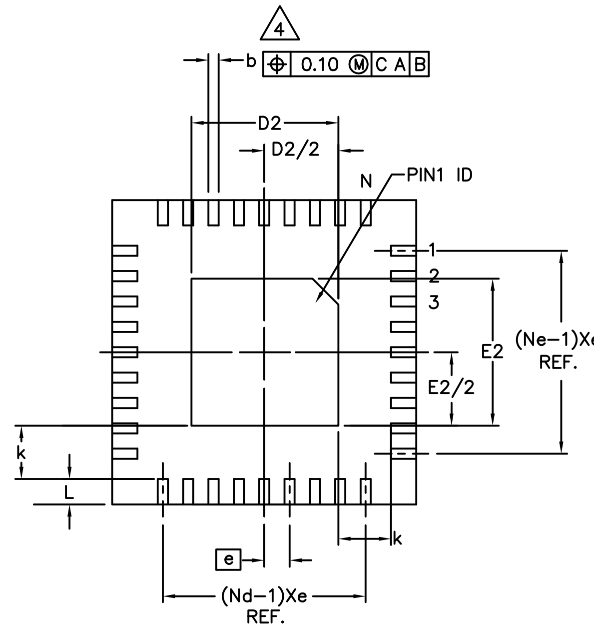
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH



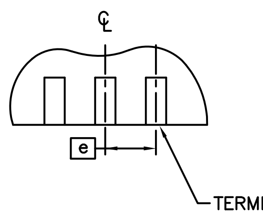
TOP VIEW



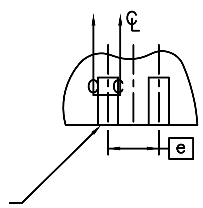
SIDE VIEW



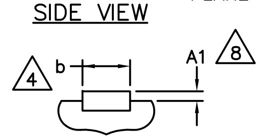
BOTTOM VIEW



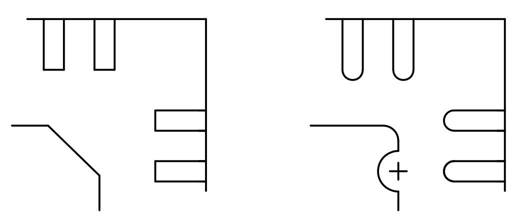
FOR ODD TERMINAL/SIDE



FOR EVEN TERMINAL/SIDE



SECTION "C–C"
SCALE: NONE



PIN #1 ID AND TIE BAR MARK OPTION

TOLERANCES UNLESS SPECIFIED		IDT™ www.IDT.com	6024 SILVERCREEK VALLEY ROAD SAN JOSE CA.95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE	NL/NLG 40 PACKAGE OUTLINE 6.0 X 6.0 mm BODY EPAD 2.90 x 2.90 mm QFN
DRAWN RAC	02/4/16		
CHECKED			
		SIZE C	DRAWING No. PSC−4115−01 — REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 3

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH

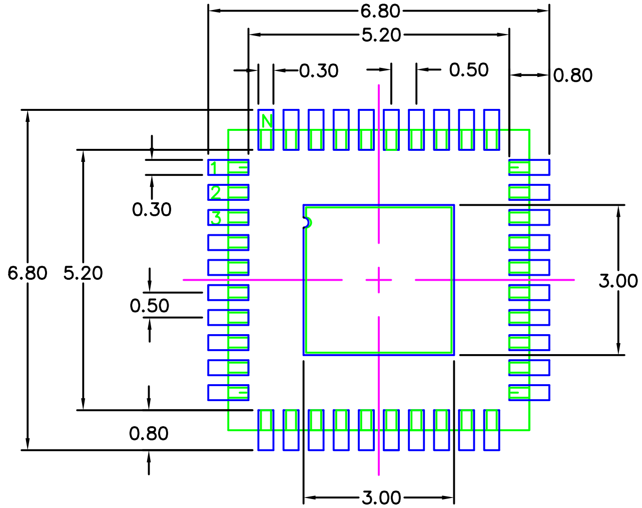
NOTES:

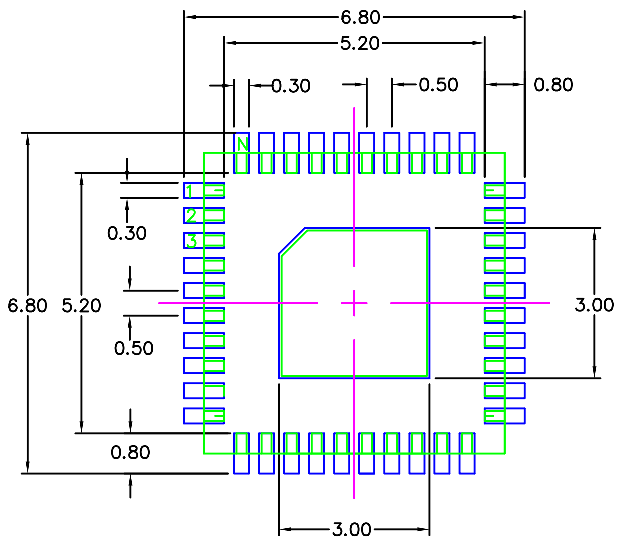
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VJJC–3 & VJJD–5 WITH THE EXCEPTION OF D2 & E2.

SYMBOL	DIMENSION			NOTE
	MIN	NOM	MAX	
b	0.18	0.25	0.30	4
D	6.00 BSC			
E	6.00 BSC			
D2	2.80	2.90	3.00	
E2	2.80	2.90	3.00	
L	0.30	0.40	0.50	
e	0.50 BSC			
k	1.15 REF.			
N	40			2
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A3	0.2 REF			
Nd	10			2
Ne	10			2

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	IDT www.IDT.com	6024 SILVERCREEK VALLEY ROAD SAN JOSE CA.95138 PHONE: (408) 284–8200 FAX: (408) 284–8591	
APPROVALS / DATE DRAWN RAC 02/4/16 CHECKED	TITLE NL/NLG 40 PACKAGE OUTLINE 6.0 X 6.0 mm BODY EPAD 2.90 x 2.90 mm QFN		
	SIZE C	DRAWING No. PSC–4115–01	REV 00
	DO NOT SCALE DRAWING	SHEET 2 OF 3	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH





RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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APPROVALS	DATE
DRAWN RAC	02/4/16
CHECKED	

TITLE NL/NLG 40 PACKAGE OUTLINE
6.0 X 6.0 mm BODY
EPAD 2.90 x 2.90 mm QFN

SIZE	DRAWING No.	REV
C	PSC-4115-01	00

DO NOT SCALE DRAWING