Description

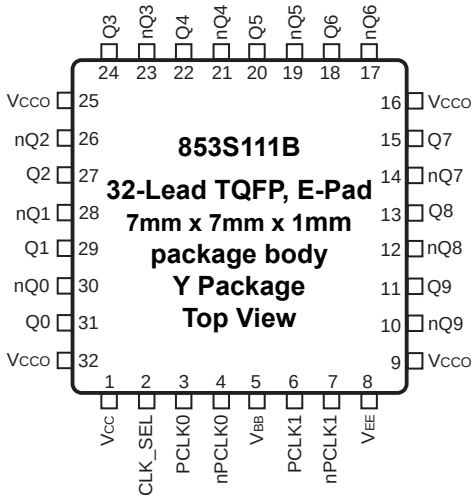
The 853S111B is a low skew, high performance 1-to-10 Differential-to-2.5V/ 3.3V LVPECL/ECL Fanout Buffer. The 853S111B is characterized to operate from either a 2.5V or a 3.3V power supply.

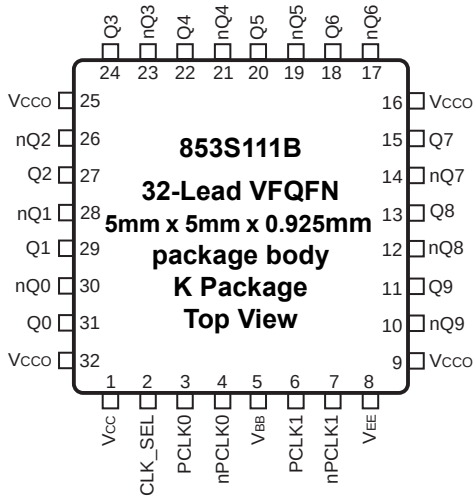
Guaranteed output and part-to-part skew characteristics make the 853S111B ideal for those clock distribution applications demanding well defined performance and repeatability.

Features

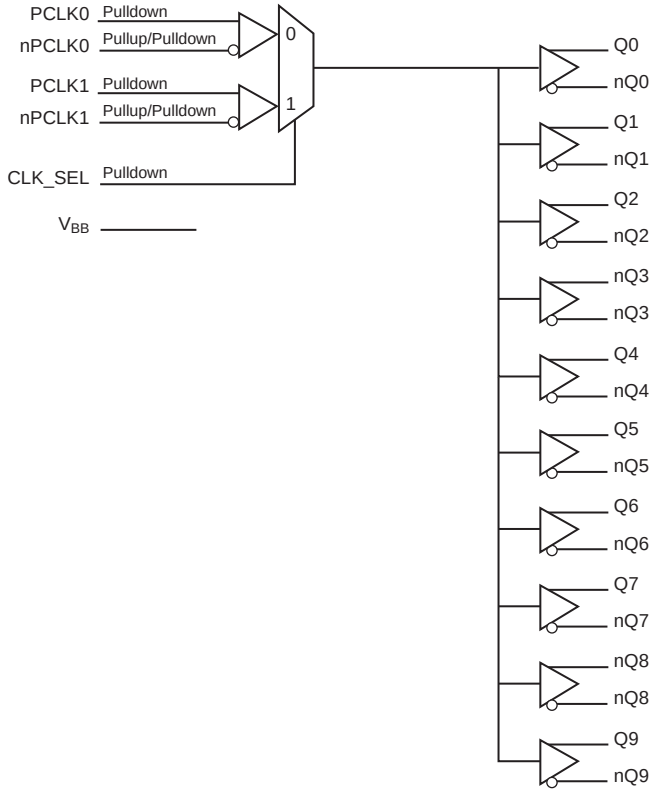
- Ten differential 2.5V, 3.3V LVPECL/ECL outputs
- Two selectable differential input pairs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, SSTL, CML
- Maximum output frequency: 2.5GHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 645ps (maximum)
- Additive Phase Jitter, RMS: 0.03ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) packaging
- Supports ≤ 105°C board temperature operations

Pin Assignments





Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CC}	Power		Positive supply pin.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1/nPCLK1 inputs. When LOW, selects PCLK0/nPCLK0 inputs. LVPECL interface levels. Also accepts standard LVCMOS input levels.
3	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
5	V_{BB}	Output		Bias voltage to be connected for single-ended applications.
6	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
8	V_{EE}	Power		Negative supply pin.
9, 16, 25, 32	V_{CCO}	Power		Output supply pins.
10, 11	nQ9, Q9	Output		Differential output pair. LVPECL/ECL interface levels.
12, 13	nQ8, Q8	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ7, Q7	Output		Differential output pair. LVPECL/ECL interface levels.
17, 18	nQ6, Q6	Output		Differential output pair. LVPECL/ECL interface levels.
19, 20	nQ5, Q5	Output		Differential output pair. LVPECL/ECL interface levels.
21, 22	nQ4, Q4	Output		Differential output pair. LVPECL/ECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL/ECL interface levels.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL/ECL interface levels.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL/ECL interface levels.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	RPullup/Pulldown Resistors			50		kΩ

Function Tables

Table 3A. Clock Input Function Table

Inputs		Outputs			
PCLK0 or PCLK1	**nPCLK0 or nPCLK1**	**Q0:Q9**	**nQ0:nQ9**	**Input to Output Mode**	**Polarity**
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Applications Information, “Wiring the Differential Input to Accept Single Ended Levels”.

Table 3B. Control Input Function Table

Inputs	
CLK_SEL	**Selected Source**
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
V_{BB} Sink//Source, I_{BB}	±0.5mA
Junction Temperature, T_j	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = V_{CCO} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C or T_B = -40°C to 105°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				124	mA

Table 4B. LVPECL DC Characteristics, V_{CC} = V_{CCO} = 3.3V; V_{EE} = 0V, T_A = -40°C to 85°C or T_B = -40°C to 105°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.445	2.225	2.295	2.445	2.215	2.33	2.410	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.70	1.375	1.52	1.645	1.355	1.535	1.63	V
V_{IH}	Input High Voltage (Single-ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 3		150	800	1300	150	800	1200	150	800	1200	mV
V_{CMR1}	Input High Voltage Common Mode Range; NOTE 3, 4		1.3		3.3	1.2		3.3	1.2		3.3	V
V_{CMR2}	Input Voltage Common Mode Range referenced to Cross-point; NOTE 3, 5		1.3 - $V_{PP}/2$		3.3 - $V_{PP}/2$	1.2 - $V_{PP}/2$		3.3 - $V_{PP}/2$	1.2 - $V_{PP}/2$		3.3 - $V_{PP}/2$	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	-10			-10			-10			µA
		nPCLK0, nPCLK1	-200			-200			-200			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: V_{IL} should not be less than V_{EE} – 0.3V, V_{IH} should not be greater than V_{CC}.
NOTE 4: Common mode voltage is defined as V_{IH}.
NOTE 5: Common mode voltage is defined as $V_{CROSS-POINT}$.

Table 4C. LVPECL DC Characteristics, V_{CC} = V_{CCO} = 2.5V; V_{EE} = 0V, T_A = -40°C to 85°C or T_B = -40°C to 105°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.645	1.425	1.495	1.645	1.415	1.53	1.61	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.90	0.575	0.72	0.845	0.555	0.735	0.83	V
V_{IH}	Input High Voltage (Single-ended)		1.275		1.56	1.275		1.56	1.275		1.56	V
V_{IL}	Input Low Voltage (Single-ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{BB}	Output Voltage Reference		0.87		1.34	0.87		1.34	0.87		1.34	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2		150	800	1300	150	800	1200	150	800	1200	mV
V_{CMR1}	Input High Voltage Common Mode Range; NOTE 2, 3		1.3		2.5	1.2		2.5	1.2		2.5	V
V_{CMR2}	Input Voltage Common Mode Range referenced to Cross-point; NOTE 2, 4		1.3 - $V_{PP}/2$		2.5 - $V_{PP}/2$	1.2 - $V_{PP}/2$		2.5 - $V_{PP}/2$	1.2 - $V_{PP}/2$		2.5 - $V_{PP}/2$	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	-10			-10			-10			µA
		nPCLK0, nPCLK1	-200			-200			-200			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: V_{IL} should not be less than V_{EE} – 0.3V, V_{IH} should not be greater than V_{CC}.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: Common mode voltage is defined as $V_{CROSS-POINT}$.

Table 4D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -3.8V to -2.375V, T_A = -40°C to 85°C or T_B = -40°C to 105°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.855	-1.075	-1.005	-0.855	-1.085	-0.97	-0.890	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.60	-1.925	-1.78	-1.655	-1.945	-1.765	-1.67	V
V_{IH}	Input High Voltage (Single-ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage (Single-ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 3		150	800	1300	150	800	1200	150	800	1200	mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.3		0	V_{EE}+1.2		0	V_{EE}+1.2		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			200			200			200	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	-10			-10			-10			µA
		nPCLK0, nPCLK1	-200			-200			-200			µA

NOTE: Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: V_{IL} should not be less than V_{EE} – 0.3V.
NOTE 4: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

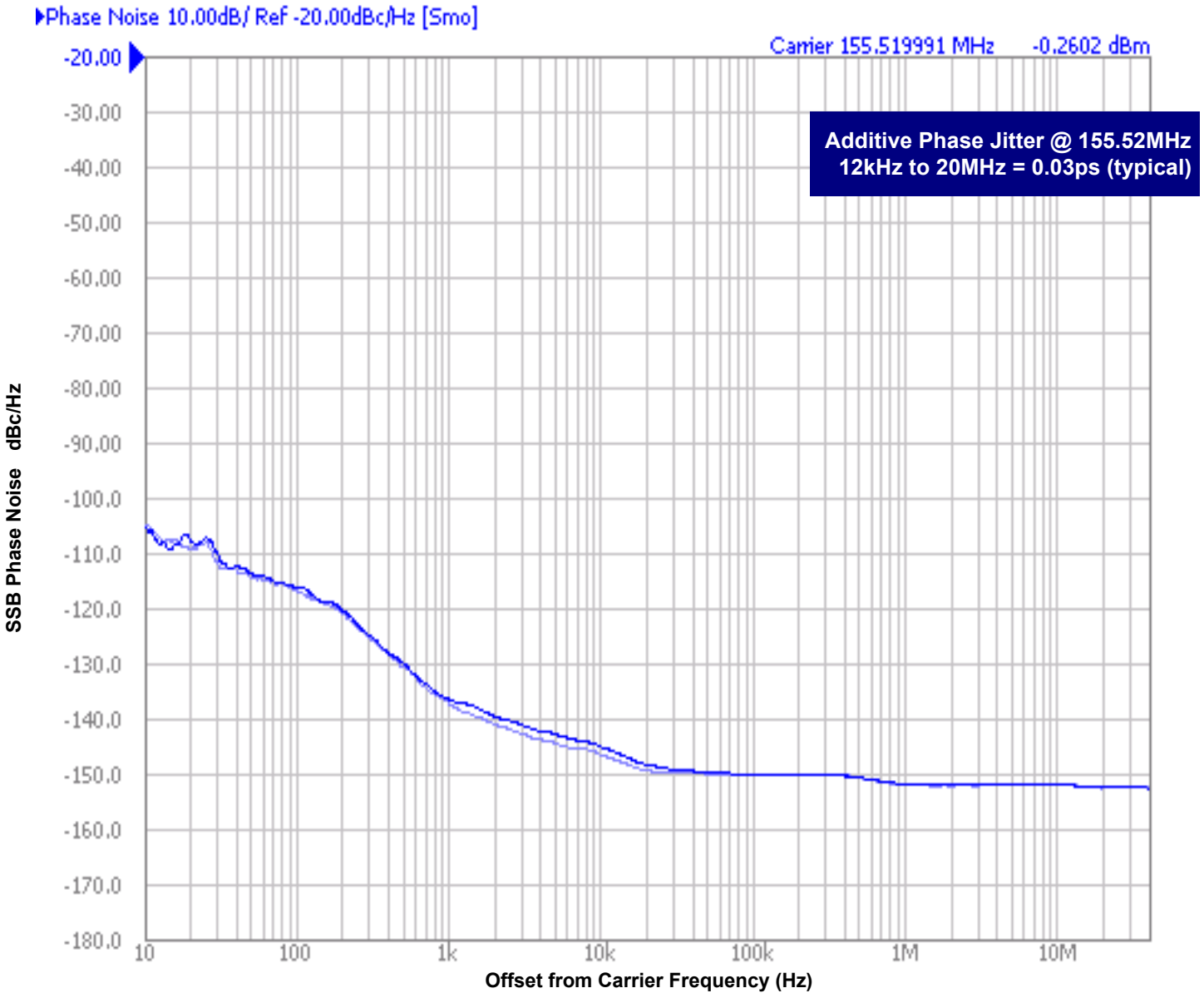
Table 5. AC Characteristics, V_{CC} = V_{CCO} = -3.8V to -2.375V or, V_{CC} = V_{CCO} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C or T_B = -40°C to 105°C

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{OUT}	Output Frequency				2.5			2.5			2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		375	475	580	395	495	610	425	530	645	ps
*t*sk(o)	Output Skew; NOTE 2, 4			30	50		30	50		30	50	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			85	150		85	150		85	150	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section			0.03	0.13		0.03	0.13		0.03	0.13	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	75	150	220	80	150	215	78	150	235	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters are measured at f ≤ 1GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

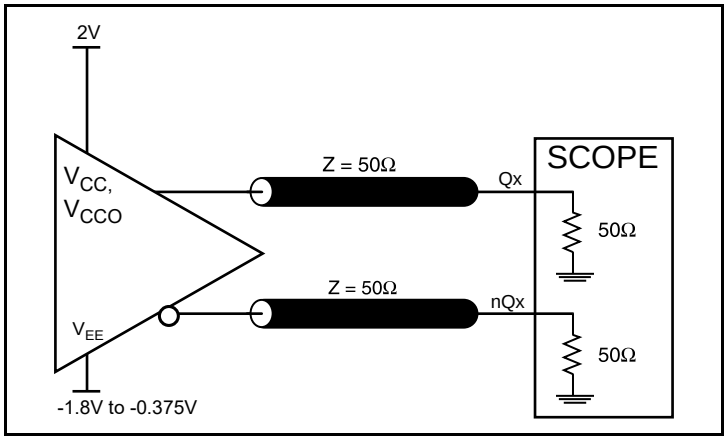
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



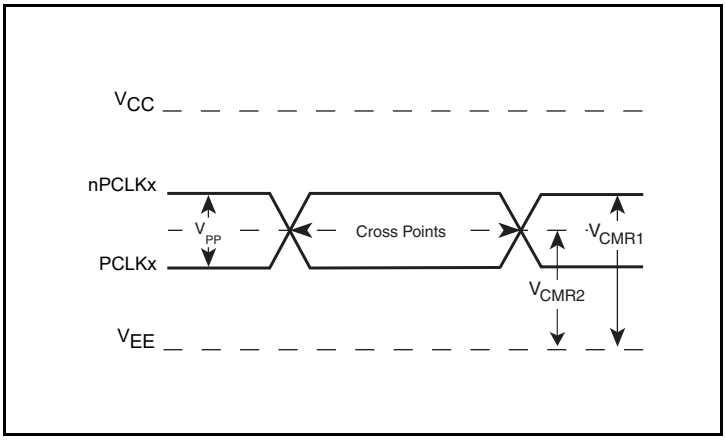
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Rohde & Schwarz SMA100A Signal Generator 9kHz - 6GHz as external input to a Hewlett Packard 8133A 3GHz Pulse Generator.

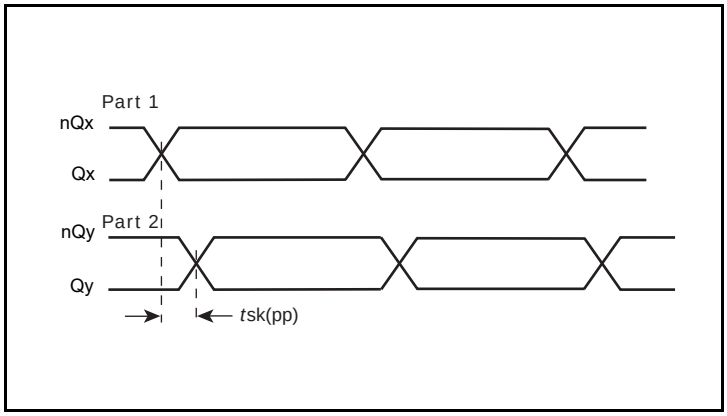
Parameter Measurement Information



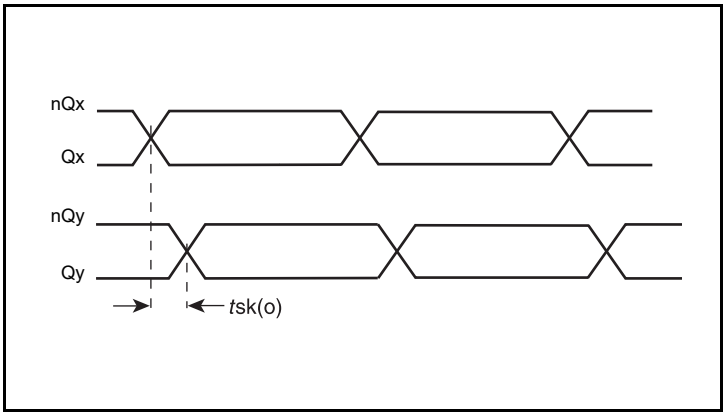
LVPECL Output Load AC Test Circuit



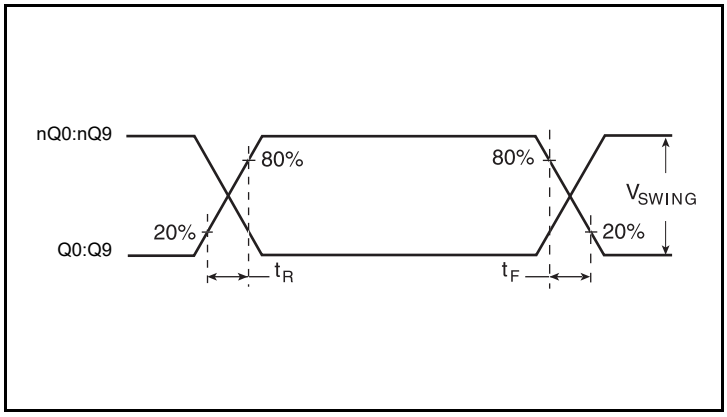
Differential Input Level



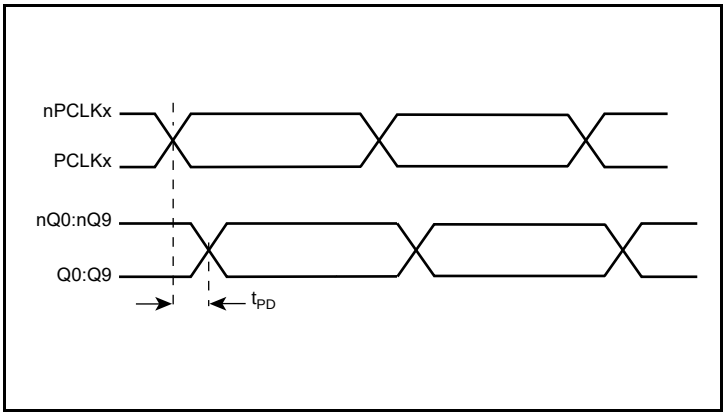
Part-to-Part Skew



Output Skew



Output Rise/Fall Time



Propagation Delay

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

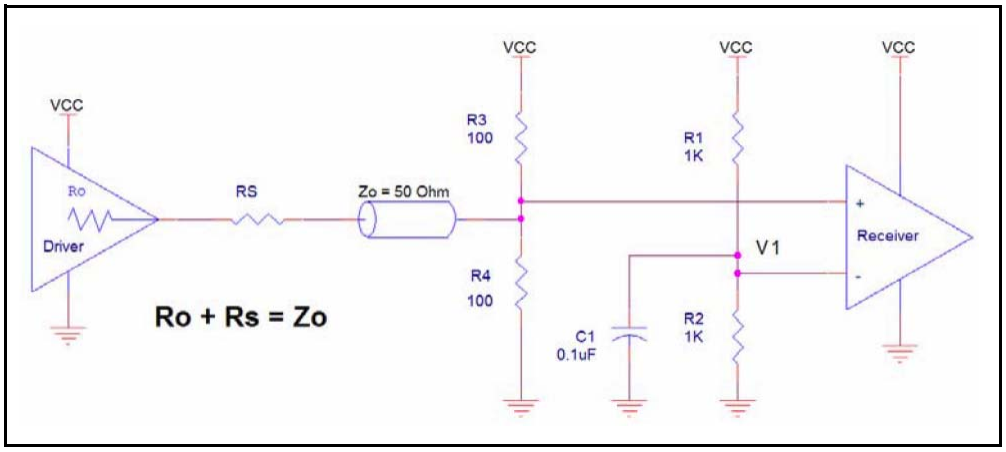


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Wiring the Differential Input to Accept Single-ended LVPECL Levels

Figure 2 shows an example of the differential input that can be wired to accept single-ended LVPECL levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

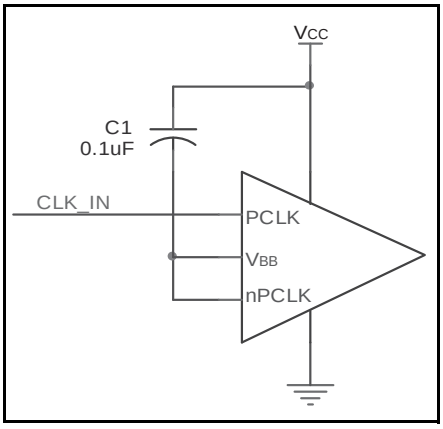


Figure 2. Single-Ended LVPECL Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the PCLK/nPCLK input driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

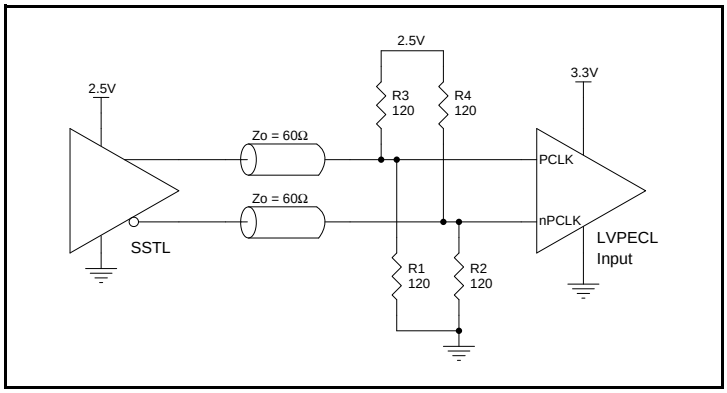


Figure 3A. PCLK/nPCLK Input Driven by an SSTL Driver

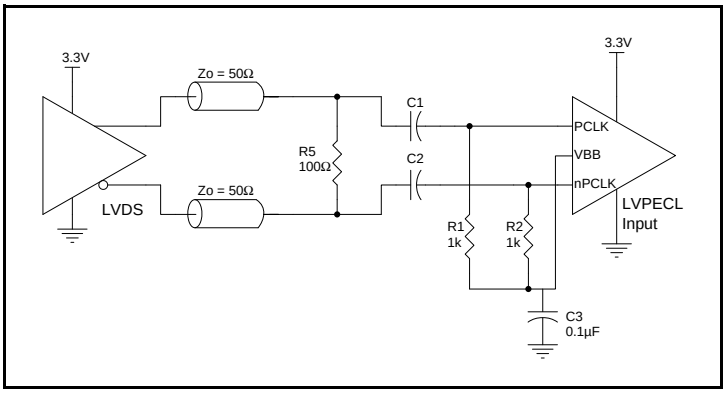


Figure 3B. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

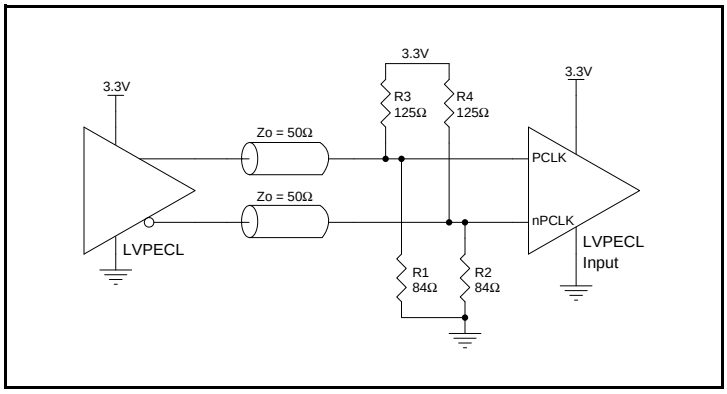


Figure 3C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

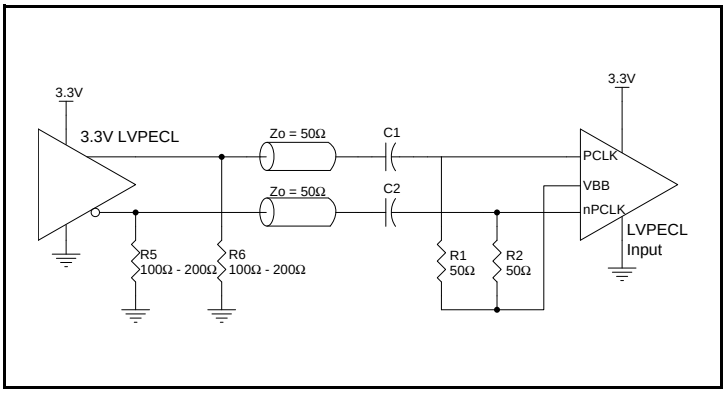


Figure 3D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

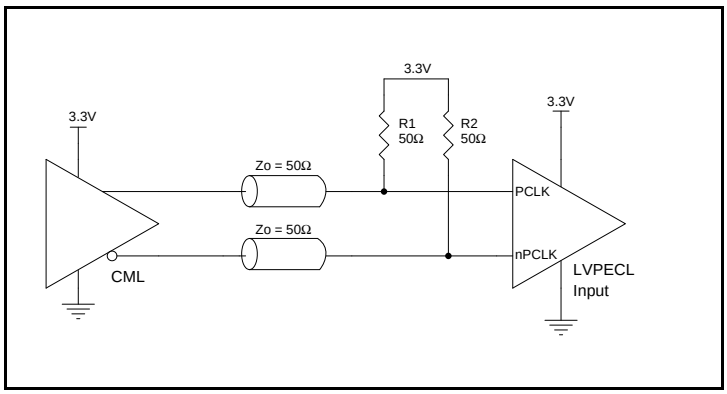


Figure 3E. PCLK/nPCLK Input Driven by a CML Driver

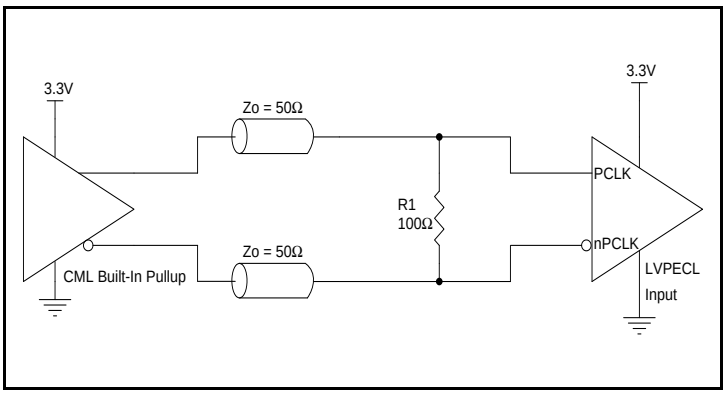


Figure 3F. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

Recommendations for Unused Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

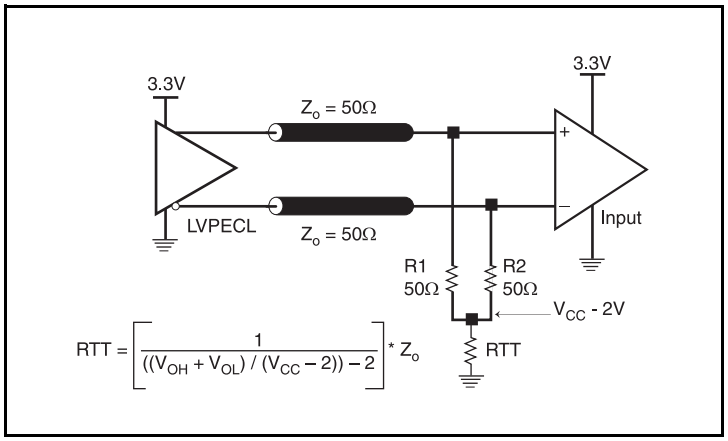


Figure 4A. 3.3V LVPECL Output Termination

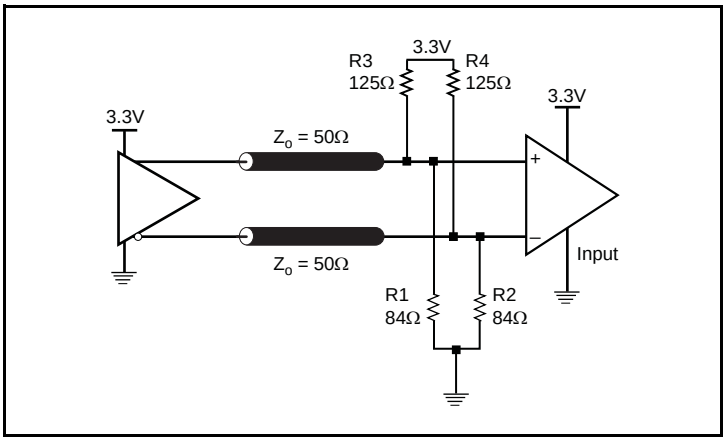


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

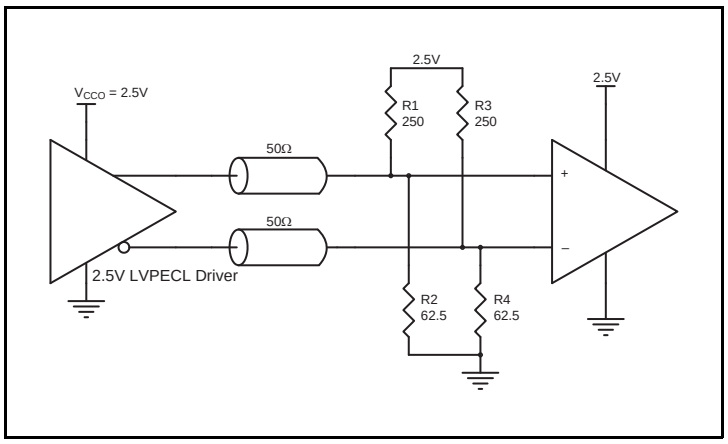


Figure 5A. 2.5V LVPECL Driver Termination Example

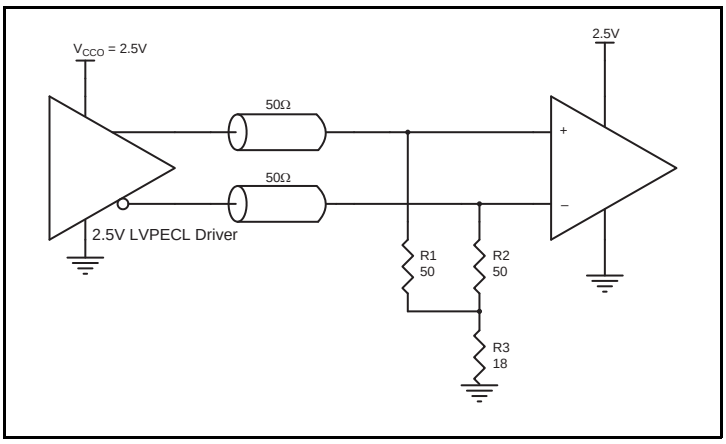


Figure 5B. 2.5V LVPECL Driver Termination Example

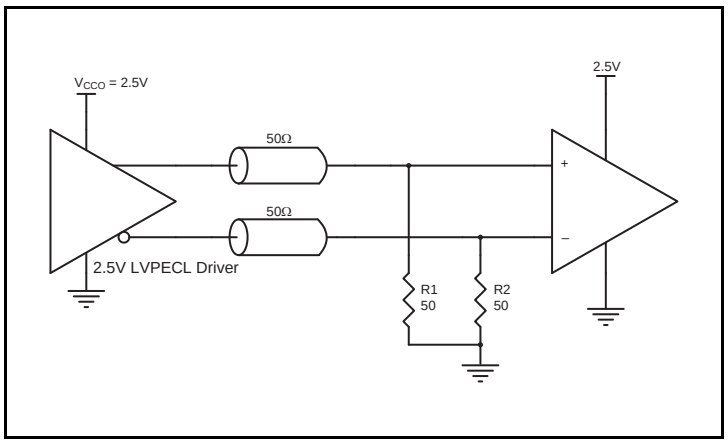


Figure 5C. 2.5V LVPECL Driver Termination Example

ePad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

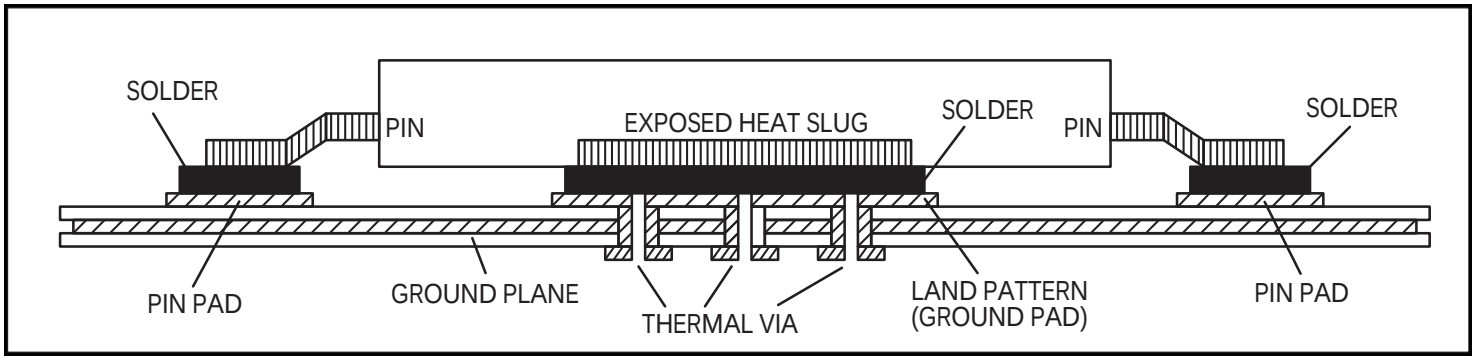


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path - Side View (Drawing not to Scale)

Schematic Example

This application note provides a general design guide using 853S111B LVPECL buffer. *Figure 8* shows a schematic example of the 853S111B LVPECL clock buffer. In this example, the input is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK0, nPCLK0 input.

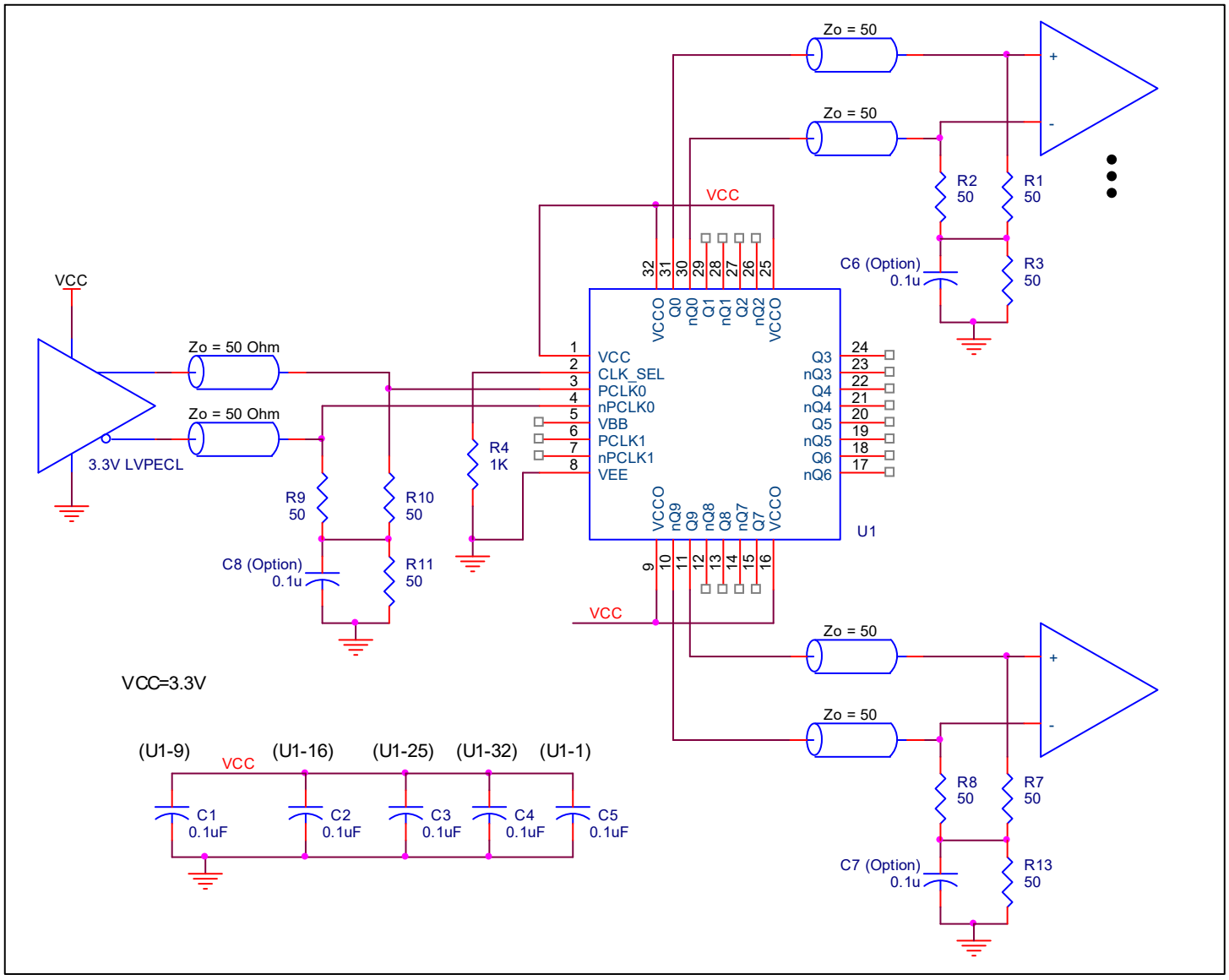


Figure 8. 853S111B Example LVPECL Clock Output Buffer Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 853S111B.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 853S111B is the sum of the core power plus the power dissipated into the load.
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated into the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 124mA = **471.2mW**
- Power $(outputs)_{MAX}$ = **30.78mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 30.78mW = **307.8mW**

Total Power$_{_MAX}$ (3.8V, with all outputs switching) = 471.2mW + 307.8mW = **779mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.779W * 42.7°C/W = 118.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance for 32-TQFP, E-Pad Convection

Thermal Parameters by Velocity[1]			
Meters per Second	**0 m/s**	**1 m/s**	**2.5 m/s**
θ_{JA} (Junction to Ambient)	36.2°C/W	30.6°C/W	29.2°C/W
θ_{JB} (Junction to Board)	1.5°C/W		
θ_{JC} (Junction to Case)	29.5°C/W		

1. Multi-Layer PCB, JEDEC Standard Test Boards

Table 6B. Thermal Resistance for 32-VFQFN, Forced Convection

Thermal Parameters by Velocity[1]			
Meters per Second	**0 m/s**	**1 m/s**	**2.5 m/s**
θ_{JA} (Junction to Ambient)	42.7°C/W	37.3°C/W	33.5°C/W
θ_{JB} (Junction to Board)	1.5°C/W		
θ_{JC} (Junction to Case)	28.4°C/W		

1. Multi-Layer PCB, JEDEC Standard Test Boards

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 9.*

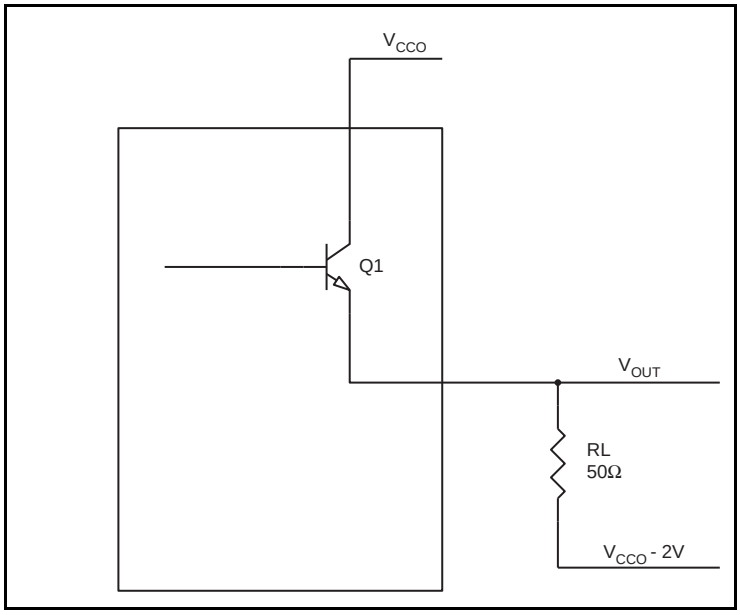


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.89V**
  ($V_{CCO\_MAX} - V_{OH\_MAX}$) = **0.89V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.67V**
  ($V_{CCO\_MAX} - V_{OL\_MAX}$) = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.89V)/50\Omega] * 0.89V =$ **19.76mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.78mW**

Transistor Count

The transistor count for 853S111B is: 448

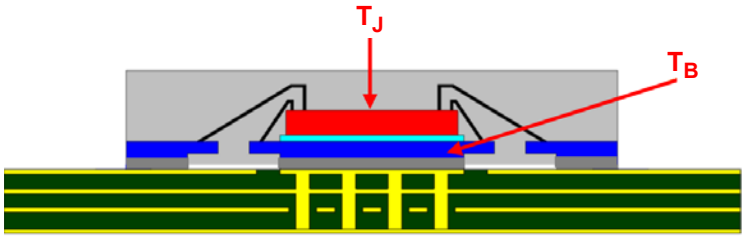
This device is pin and functional compatible with and is the suggested replacement for the 853S111B. Pin compatible with MC100EP111, MC100LVEP111 and 853S111B.

Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, Ψ_{JB}, is calculated using the following equation:

- $T_J = T_B + \Psi_{JB} \times P_d$, where
- T_J = Junction temperature at steady state condition in (^oC).
- T_B = Board or case temperature (Bottom) at steady state condition in (^oC).
- Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.
- P_d = power dissipation (W) in desired operating configuration.



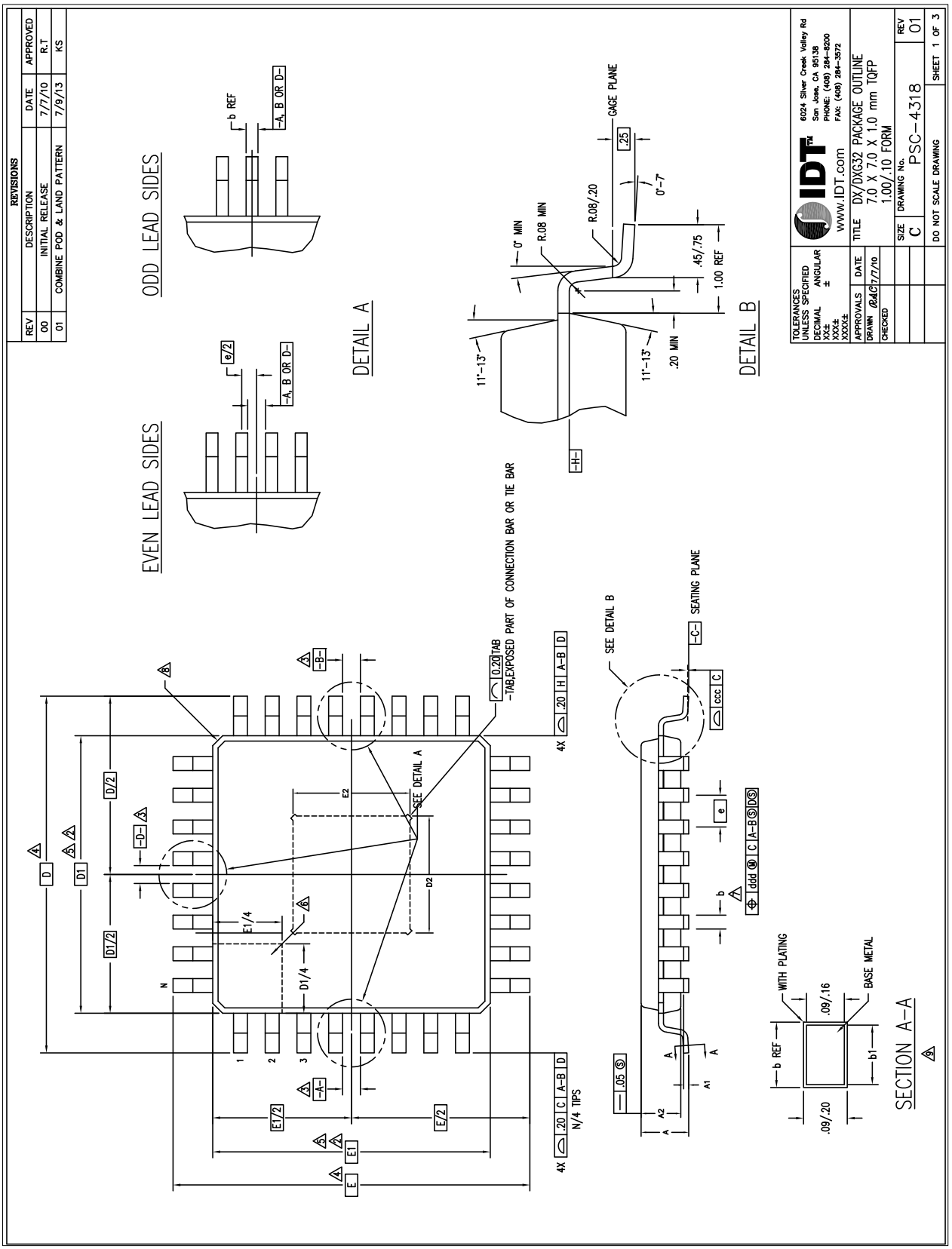
The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC bottom case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_B + \Psi_{JB} \times P_d$

Package type:	32-VFQFN	32-TQFP
Body size:	5 × 5mm	7 × 7mm
ePad size:	3.3 × 3.3mm	3.5 × 3.5mm
Thermal via:	3 × 3 matrix	3 × 3 matrix
Ψ_{JB}	1.5C/W	1.5C/W
T_B	105ºC	105ºC
P_d	0.779W	0.779W

For the variables above, the junction temperature is equal to 106.2^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 118.3^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Package Outline Drawings (TQFP) – Sheet 1



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	7/7/10	R.T
01	COMBINE POD & LAND PATTERN	7/9/13	KS

SYMBOL	JEDEC VARIATION BBC			NOTE
	MIN	NOM	MAX	
A	–	–	1.20	
A1	.05	.10	.15	
A2	0.95	1.00	1.05	
D		9.00 BSC		4
D1		7.00 BSC		5,2
E		9.00 BSC		4
E1		7.00 BSC		5,2
N		32		
e		.80 BSC		
E2		3.5		
D2		3.5		
b	.30	.37	.45	7
b1	.30	.35	.40	
ccc	–	–	.10	
ddd	–	–	.20	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [–C–]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–026, VARIATIONS BBA & BBC.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
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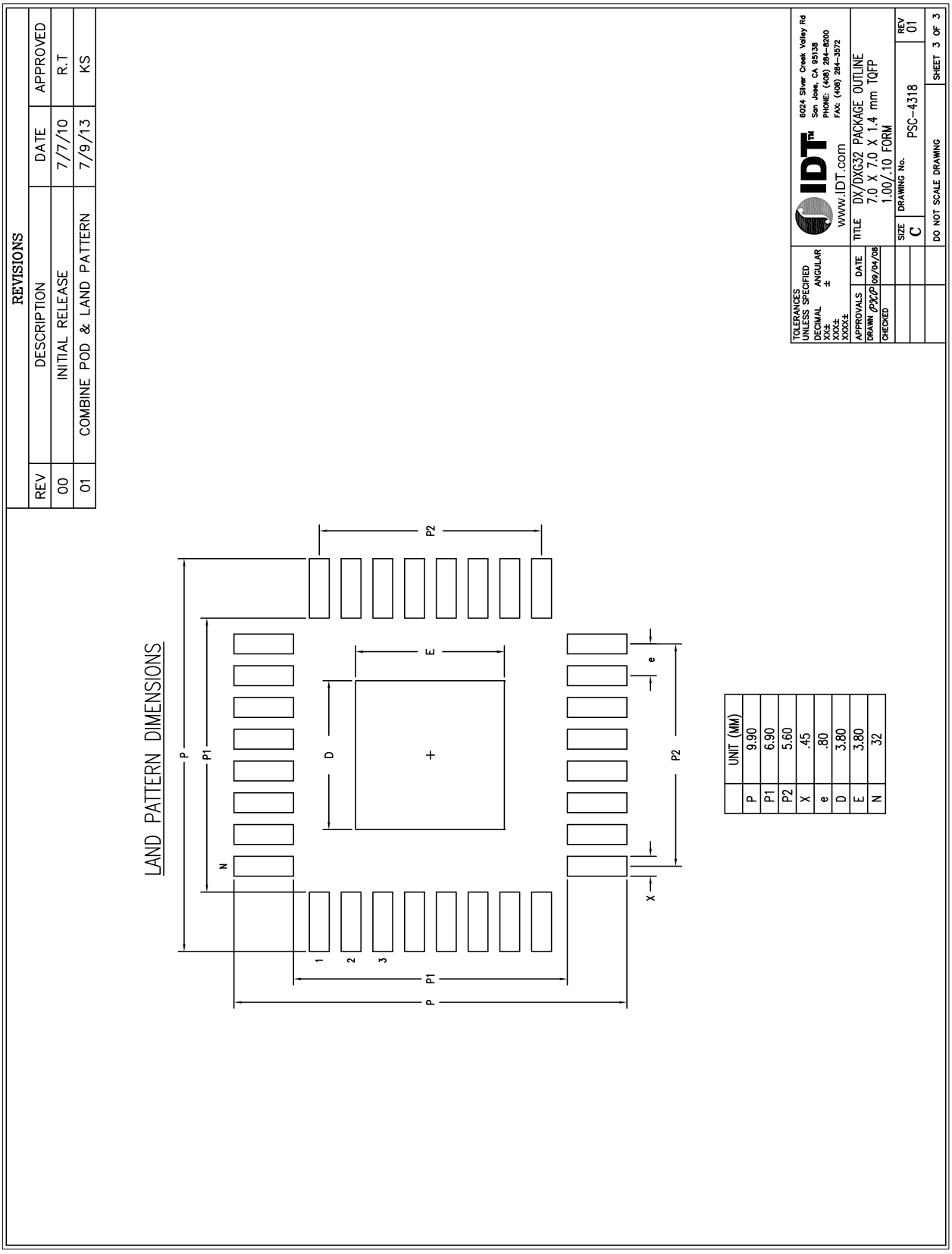
TITLE DX/DXG32 PACKAGE OUTLINE
7.0 X 7.0 X 1.0 mm TQFP
1.00/.10 FORM

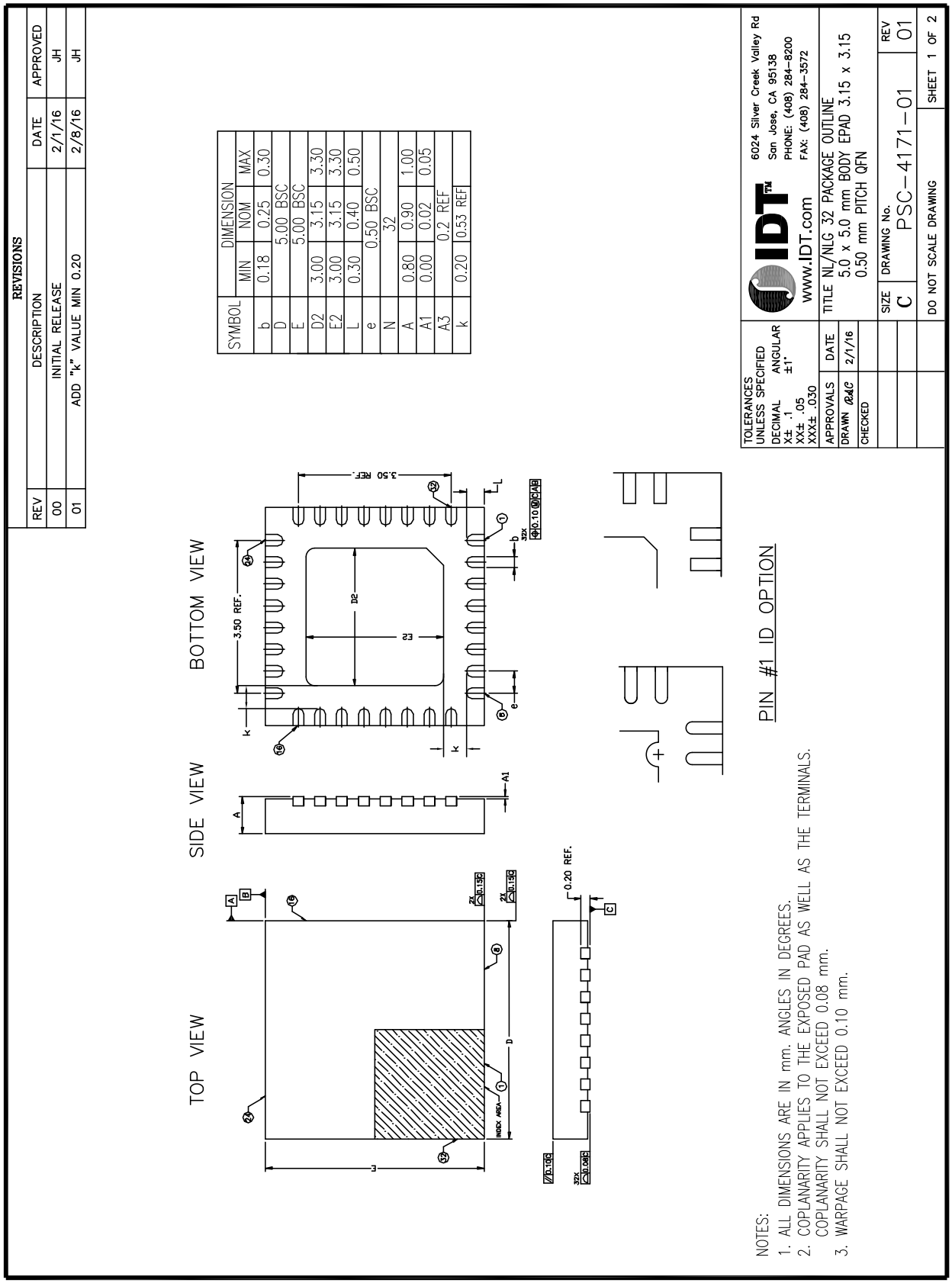
SIZE C | DRAWING No. PSC–4318 | REV 01

DO NOT SCALE DRAWING | SHEET 2 OF 3

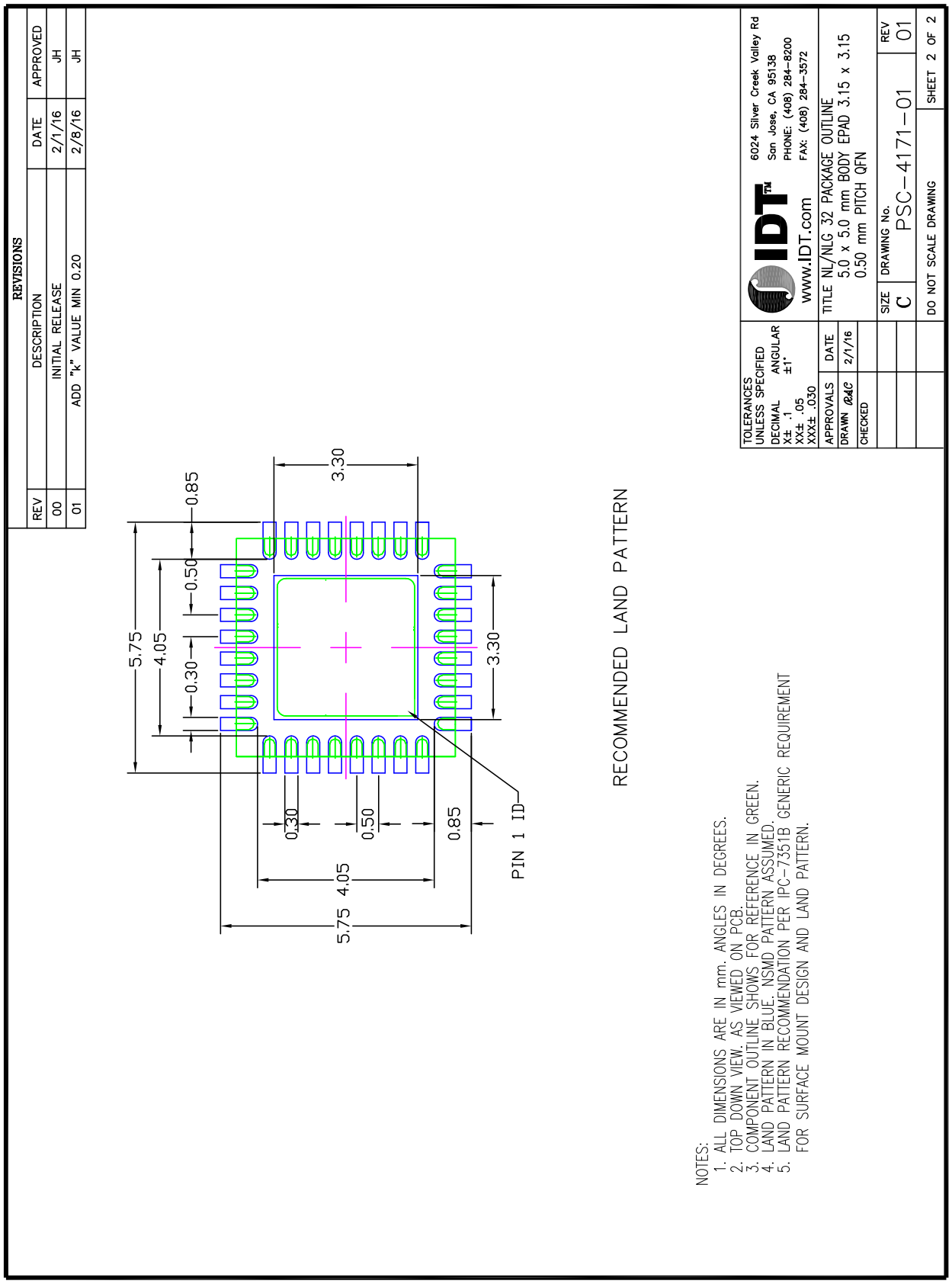
Package Outline Drawings (TQFP) – Sheet 3



Package Outline Drawings (VFQFN) – Sheet 1



Package Outline Drawings (VFQFN) – Sheet 2

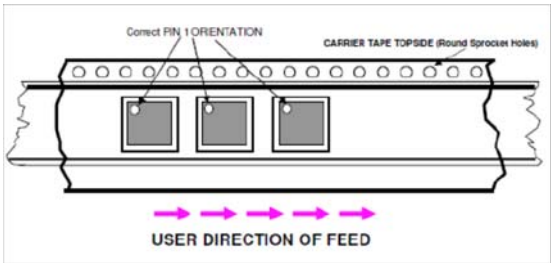
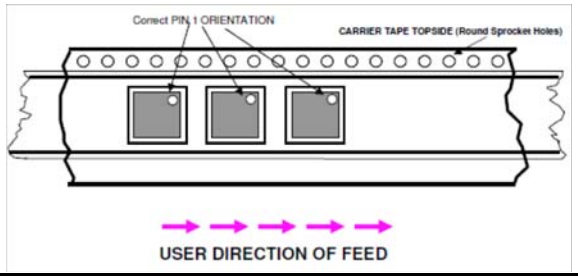


Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S111BYILF	ICS53S111BIL	32-Lead TQFP, E-Pad	Tray	-40°C to 85°C
853S111BYILFT	ICS53S111BIL	32-Lead TQFP, E-Pad	Tape & Reel	-40°C to 85°C
853S111BKILF	ICS3S111BIL	32-Lead VFQFN	Tray	-40°C to 85°C
853S111BKILFT	ICS3S111BIL	32-Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
853S111BKILF/W	ICS3S111BIL	32-Lead VFQFN	Tape & Reel, pin 1 orientation EIA-481-D	-40°C to 85°C

Table 11. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History

Revision Date	Description of Change
November 9, 2017	Replaced operating temperature with junction temperature in Absolute Maximum Ratings; also removed the package thermal information Changed the T_A and T_B temperature ranges to indicate “or” in all electrical table titles
September 8, 2017	Added a new bullet to Features about board temperature. Added “T_B = -40°C to 105°C” to Table 4A, 4B, 4C, 4D, and 5. Added Case Temperature Considerations
August 3, 2017	Updated Tables 6A and 6B with θ_{JB} and θ_{JC} values. Updated the package outline drawings; however, there are no mechanical differences.
January 14, 2016	Applications Information Section - added *Wiring the Differential Input to Accept single-ended LVPECL Levels.* Updated datasheet header/footer.
June 30, 2015	Added P1 orientation for Tape and Reel table. Ordering information Table - Added W part number.
June 15, 2015	LVPECL DC Characteristics Table - added V_{CMR1} and V_{CMR2} specs. Change Note 4, and added Note 5. LVPECL DC Characteristics Table - added V_{CMR1} and V_{CMR2} specs. Change Note 4, and added Note 5. Deleted “ICS” prefix from part number throughout the datasheet.
January 10, 2014	Added $V_{BB,}$ Output Reference row to table 4C.
June 12, 2013	Updated *Wiring the Differential Inputs to Accept Single-ended Levels* application note. Corrected diagrams in application note, *Termination for 2.5V LVPECL Outputs,* Corrected 32-Lead VFQFN Package Outline Ordering Information Table - corrected 32-Lead TQFP packaging column from Tube to Tray.
October 29, 2012	Added CML to 3rd bullet. Added figures 3E and 3F. Deleted quantity from tape and reel.
March 5, 2012	Added 0.13 value to Max columns for tjit Buffer Additive Phase Jitter, RMS.
November 18, 2011	Added 32-Lead VFQFN Pin Assignment and all references throughout the datasheet. Thermal Resistance Table, updated theta ja numbers. Thermal Resistance, updated theta ja numbers. Ordering Information Table - added 32-Lead VFQFN ordering information.