88W8801_SDS

2.4 GHz Single-band 1x1 Wi-Fi 4 Solution

Rev. 2 — 14 December 2020 Product short data sheet

1 Product overview

The 88W8801 is a highly integrated, single-band (2.4 GHz) IEEE 802.11n 1x1 System-on-Chip (SoC), specifically designed to support High Throughput (HT) data rates for Wi-Fi products.

The device provides the combined functions of Direct Sequence Spread Spectrum (DSSS) and Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct conversion Wi-Fi RF radio on a single integrated chip.

For security, the 802.11i security standard is supported through several protocols. And for video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported.

Host interfaces include USB 2.0 and SDIO 2.0 to connect the Wi-Fi radio to the host processor.

The device is available in a 48-pin QFN package.

Figure 1 shows the application block diagram of the device.

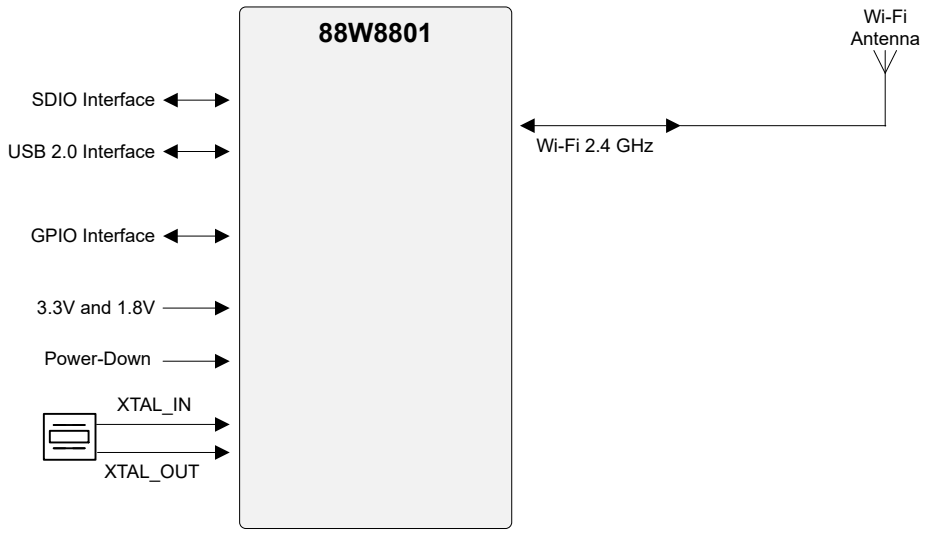


Figure 1. Application block diagram

1.1 Applications

- Internet of Things
- Imaging platforms (printers, digital still cameras, digital picture frames)
- Consumer electronic devices
- Smart Energy systems
- Connected appliances

1.2 Wi-Fi key features

- 1x1 SISO and HT20 operation
- 802.11e Quality of Service (QoS)
- Thick MAC architecture
- Simultaneous operation
  - Mobile AP and STA
  - Wi-Fi direct and STA
- Supports WPA2/WPA2 mixed mode and WPA3 security standards

1.3 Host interfaces

- USB 2.0 with Link Power Management (LPM)
- SDIO 2.0

1.4 Operating characteristics

- Supply voltage: 1.8V and 3.3V
- Operating temperature
  - Commercial: 0 to 70°C
  - Extended: -30 to 85°C
  - Industrial: -40 to 85°C

1.5 General features

- Package: 48-pin QFN (6 mm x 6 mm)
- 26 MHz and 38.4 MHz crystal clock support
  - Supports CMOS and low-swing sine wave input clock
- Low-power operation supporting deep-sleep and standby modes
- ARM-based CPU
- 128 MHz maximum CPU clock speed
- Peripheral interfaces:
  - Clocked serial unit: 2-Wire serial interface
  - UART (debug) interface
  - General Purpose Input Output (GPIO)
- Memory
  - Internal SRAM
  - Boot ROM
  - One Time Programmable (OTP) memory for storing the MAC address and calibration data

1.6 Internal block diagram

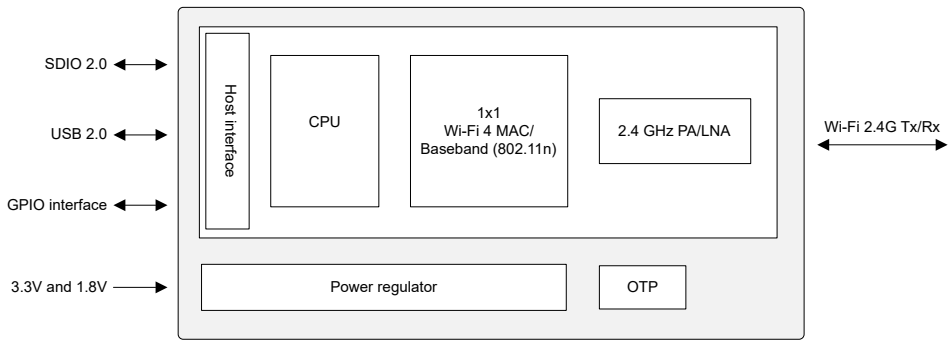


Figure 2. Internal block diagram

2 Ordering information

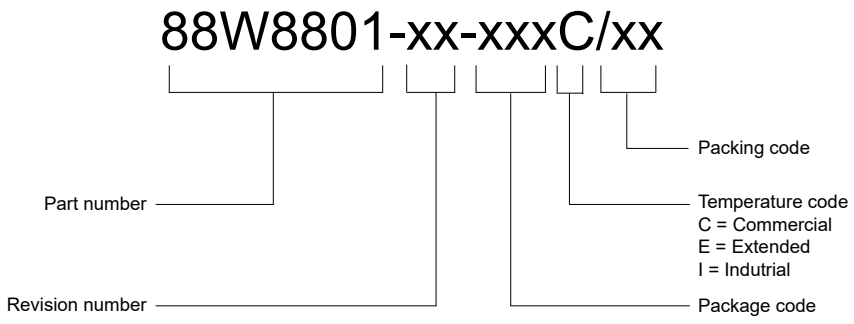


Figure 3. Part numbering scheme

Table 1. Part order codes

Part Order Code	Package Type	Packing
88W8801-B0-NMDC/AK	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tray
88W8801-B0-NMDC/AZ	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tape and Reel
88W8801-B0-NMDE/AK	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tray
88W8801-B0-NMDE/AZ	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tape and Reel
88W8801-B0-NMDI/AK	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tray
88W8801-B0-NMDI/AZ	48-pin QFN - 6 x 6 x 0.85 mm, with 0.4 mm pitch	Tape and Reel

3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11 data rates of 1 and 2 Mbps
- 802.11b data rates of 5.5 and 11 Mbps
- 802.11g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant with maximum data rates up to 72.2 Mbps (20 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11n block acknowledgement extension
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi direct connectivity

3.2 Wi-Fi MAC

- Simultaneous peer-to-peer and infrastructure modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open system and shared key authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgement extension
- Multiple-BSSID and Multiple-Station operation
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Mobile hotspot

3.3 Wi-Fi baseband

- 802.11n 1x1 SISO
- Backward compatibility with legacy 802.11g/b technology
- PHY data rates up to 72.2 Mbit/s
- 20 MHz channel bandwidth
- Modulation and Coding Scheme (MCS)—MCS 0~7
- Radio resource measurement
- Optional 802.11n SISO features:
  - 1 spatial stream STBC reception and transmission
  - Short guard interval
  - RIFS on receive path for 802.11n packets
  - 802.11n greenfield Tx/Rx
- Power save features

3.4 Wi-Fi radio

- Integrated direct-conversion radio
- 20 MHz channel bandwidth
- Integrated Tx/Rx RF switch, PA, and LNA

Wi-Fi Rx path

- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

Wi-Fi Tx path

- Integrated power amplifier with power control
- Optimized Tx gain distribution for linearity and noise performance

Wi-Fi local oscillator

- Fractional-N oscillator for multiple reference clock support
- Fine channel step

3.5 Wi-Fi encryption

- WEP 64- and 128-bit encryption
- AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
- Simultaneous Authentication of Equals (SAE) WPA3
- WLAN Authentication and Privacy Infrastructure (WAPI)

3.6 Wi-Fi host interfaces

- USB 2.0 with Link Power Management (LPM)
- SDIO 2.0

4 Pin information

4.1 Signal diagram

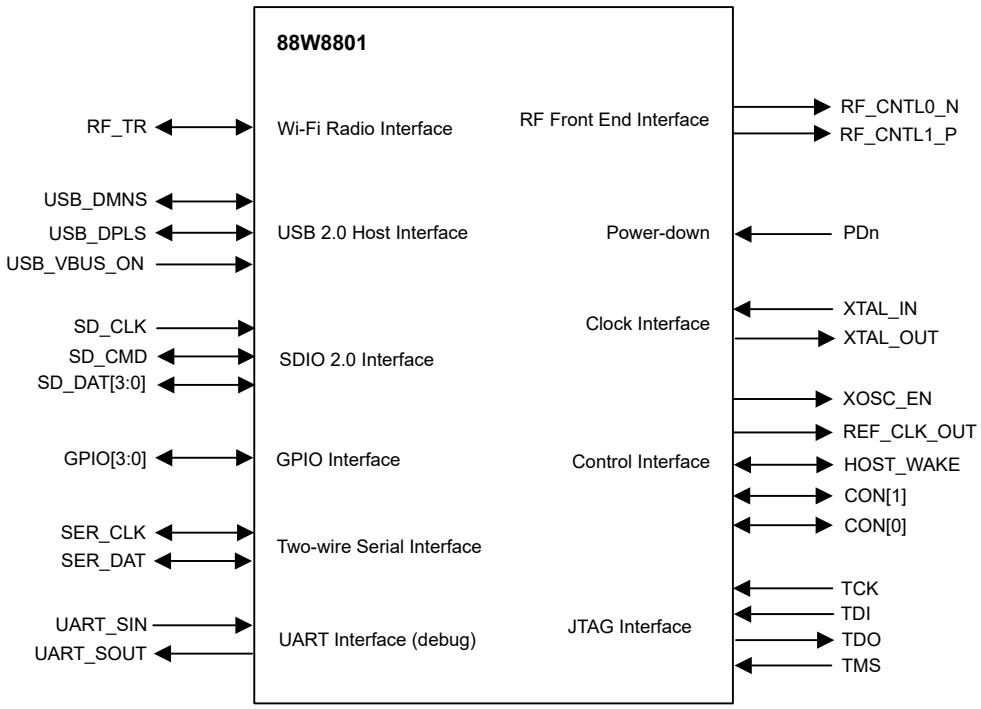


Figure 4. Signal diagram

4.2 Pin assignment

Figure 5 shows the pin assignment on the 48-pin QFN package top view.

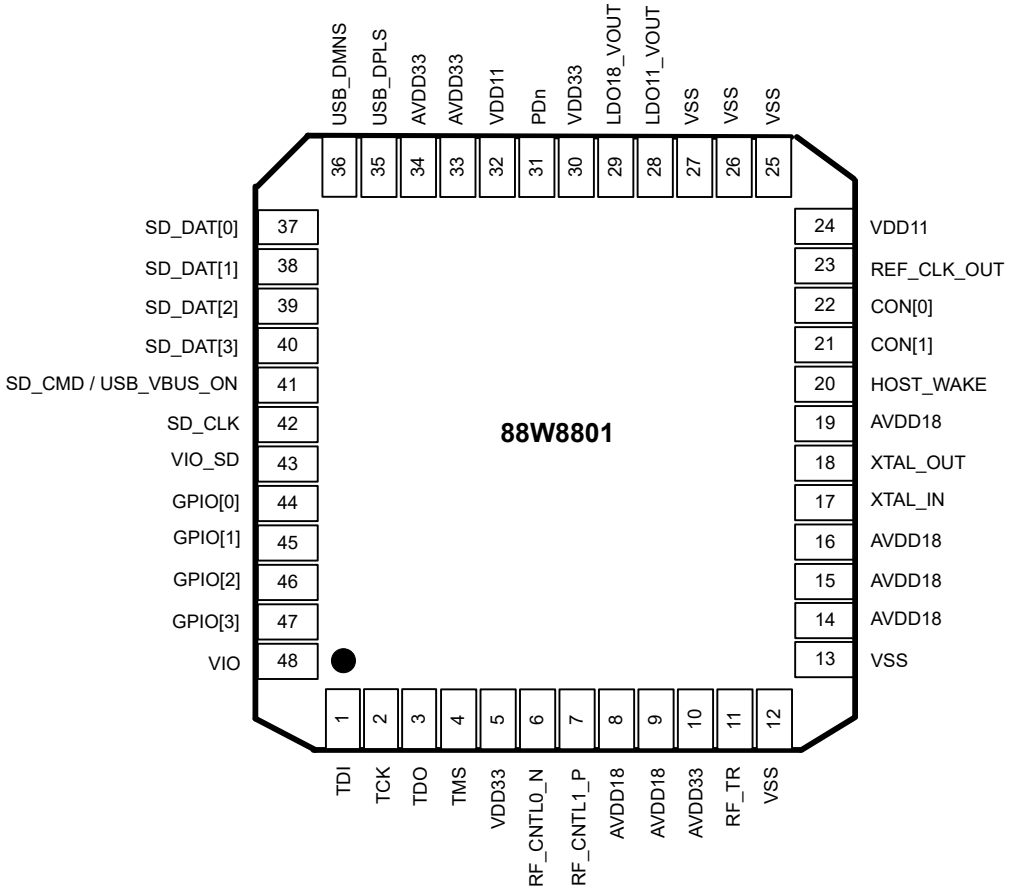


Figure 5. 88W8801 pin assignment (package top view)

4.3 Signal types

Table 2. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output

4.4 Pin list

Table 3 shows the pin list sorted by pin number.

Table 3. Pin list by number

Pin number	Pin name	Supply	Type
1	TDI	VIO	I
2	TCK	VIO	I
3	TDO	VIO	O
4	TMS	VIO	I
5	VDD33	--	Power
6	RF_CNTL0_N	VDD33	O
7	RF_CNTL1_P	VDD33	O
8	AVDD18	--	Power
9	AVDD18	--	Power
10	AVDD33	--	Power
11	RF_TR	AVDD33	A, I/O
12	VSS	--	Ground
13	VSS	--	Ground
14	AVDD18	--	Power
15	AVDD18	--	Power
16	AVDD18	--	Power
17	XTAL_IN	AVDD18	A, I
18	XTAL_OUT	AVDD18	A, O
19	AVDD18	--	Power
20	HOST_WAKE	AVDD18	I
21	CON[1]	AVDD18	I
22	CON[0]	AVDD18	I
23	REF_CLK_OUT	AVDD18	O
24	VDD11	--	Power
25	VSS	--	Power
26	VSS	--	Power
27	VSS	--	Power
28	LDO11_VOUT	--	Power
29	LDO18_VOUT	--	Power
30	VDD33	--	Power
31	PDn	AVDD18	I
32	VDD11	--	Power
33	AVDD33	--	Power
34	AVDD33	--	Power

Table 3. Pin list by number*...continued*

Pin number	Pin name	Supply	Type
35	USB_DPLS	AVDD33	I/O
36	USB_DMNS	AVDD33	I/O
37	SD_DAT[0]	VIO_SD	I/O
38	SD_DAT[1]	VIO_SD	I/O
39	SD_DAT[2]	VIO_SD	I/O
40	SD_DAT[3]	VIO_SD	I/O
41	SD_CMD / USB_VBUS_ON	VIO_SD	I/O
42	SD_CLK	VIO_SD	I
43	VIO_SD	--	Power
44	GPIO[0]	VIO	I/O
45	GPIO[1]	VIO	I/O
46	GPIO[2]	VIO	I/O
47	GPIO[3]	VIO	I/O
48	VIO	--	Power

4.5 Pin description

4.5.1 Pin states

The terminology used for the pin state information in some pin description tables is as follows:

- HW State: Hardware default state after reset
- PD State: Power-down state
- PU/PD: Programmable pull-up/pull-down

Note:

After firmware is downloaded, the pads (GPIO, serial interface, JTAG, and RF control) are programmed in functional mode per the functionality of the pins.

For SDIO, once the command is received from the host, the pads are configured accordingly. Pull-up (PU) and pull-down (PD) are only effective when the pad is in input mode.

4.5.2 Wi-Fi radio interface

Table 4. Wi-Fi radio interface

QFN Pin No.	Pin name	Type	Supply	Description
11	RF_TR	A, I/O	AVDD33	Transmit/Receive RF Input/Output—2.4 GHz Baseband input/output data

4.5.3 RF front-end control interface

Table 5. RF font-end control interface

QFN Pin No.	Pin Name	Supply	No Pad Power State	Reset State	HW State	PD State	Internal PU	PU	PD
6	RF_CNTL0_N	VDD33	tristate	input	output drive low	drive low	weak PU enable	no	no
RF Control 0 - RF control output low									
7	RF_CNTL1_P	VDD33	tristate	input	output drive high	drive high	weak PU enable	no	no
RF Control 1 - RF control output high									

4.5.4 General purpose I/O (GPIO) interface

Table 6. General purpose I/O (GPIO) interface

QFN Pin No.	Pin name	Pad supply	No pad power state	Reset state	HW state	PD state	Internal PU	PU	PD
47	GPIO[3]	VIO	tristate	output drive high	output drive high	tristate	nominal PU enable	yes	yes
GPIO Mode: GPIO[3] **TWSI EEPROM Mode**: SER_DAT Serial interface data (input/output)									
46	GPIO[2]	VIO	tristate	input	output drive high	tristate	weak PU enable	no	no
GPIO Mode: GPIO[2] **TWSI EEPROM Mode**: SER_CLK Serial interface clock (input/output)									
45	GPIO[1]	VIO	tristate	input	output drive high	tristate	weak PU enable	yes	yes
GPIO Mode: GPIO[1] **UART Mode**: UART_SOUT (output), debug only Host Wakeup: SoC-to-Host wakeup (output)									
44	GPIO[0]	VIO	tristate	output	output drive high	tristate	nominal PU enable	yes	yes
GPIO Mode: GPIO[0] **UART Mode**: UART_SIN (input), debug only **Oscillator Mode**: XOSC_EN (output, active high) 0 = disable external oscillator 1 = enable external oscillator									

4.5.5 SDIO 2.0 host interface

Table 7. SDIO host interface

QFN Pin No.	Pin name	Supply	No pad power state	Reset state	HW state	PD state	Internal PU	PU	PD
42	SD_CLK	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Clock input **SDIO 1-bit Mode**: Clock input **SDIO SPI Mode**: Clock input									
41	SD_CMD/ USB_VBUS_ON	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Command/response (input/output) **SDIO 1-bit Mode**: Command line **SDIO SPI Mode**: Data input **USB Mode**: USB_VBUS_ON (input)									
37	SD_DAT[0]	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[0] **SDIO 1-bit Mode**: Data line **SDIO SPI Mode**: Data output									
38	SD_DAT[1]	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[1] **SDIO 1-bit Mode**: Interrupt **SDIO SPI Mode**: Interrupt									
39	SD_DAT[2]	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) **SDIO 1-bit Mode**: Read wait (optional) **SDIO SPI Mode:** Reserved									
40	SD_DAT[3]	VIO_SD	tristate	input	input	tristate	nomi-nal PU enable	yes	yes
SDIO 4-bit Mode: Data line Bit[3] **SDIO 1-bit Mode**: Reserved **SDIO SPI Mode**: Card select (active low)									

4.5.6 USB 2.0 host interface

Table 8. USB host interface[1]

QFN Pin No.	Pin name	Type	Supply	Description
36	USB_DMNS	I/O	AVDD33	USB Serial Differential Data Negative
35	USB_DPLS	I/O	AVDD33	USB Serial Differential Data Positive

[1] For USB_VBUS_ON, see Section 4.5.5 "SDIO 2.0 host interface".

4.5.7 Control interface

Table 9. Control interface

QFN Pin No.	Pin name	Supply	No pad power state	Reset state	HW state	PD state	Internal PU	PU	PD
20	HOST_WAKE	AVDD18	tristate	input	input	tristate	weak PD enable	yes	yes
Host Wakeup Host-to-SoC Wakeup (input)									
21	CON[1]	AVDD18	tristate	input	input	tristate	weak PU enable	yes	yes
Configuration Pin (CON[1]) See Section 4.6 "Configuration pins".									
22	CON[0]	AVDD18	tristate	input	input	tristate	weak PU ena-ble	no	no
Configuration Pin (CON[0]) See Section 4.6 "Configuration pins".									
23	REF_CLK_OUT	AVDD18	tristate	analog	analog	tristate	analog	yes	yes
Reference Clock Output									

4.5.8 Clock interface

Table 10. Clock interface

QFN Pin No.	Pin name	Type	Supply	Description
17	XTAL_IN	A, I	AVDD18	Crystal/Crystal Oscillator / System Clock Input Accepts 26/38.4 MHz clock signals from a crystal oscillator (frequency stability ±20 ppm).
18	XTAL_OUT	A, O	AVDD18	Crystal / Crystal Oscillator Output Connect this pin to ground when an external oscil-lator is used.

4.5.9 Power-down

Table 11. Power-down

QFN Pin No.	Pin name	Type	Supply	Description
31	PDn	I	Input	Full Power-Down (active low) 0 = full power-down mode 1 = normal mode • Connect to power-down pin of host or 3.3V/1.8V • External host required to drive this pin high for normal operation No internal pull-up on this pin.

4.5.10 Power supply and ground pins

Table 12. Power supply and ground pins

QFN Pin No.	Pin name	Type	Description
24 32	VDD11	Power	1.1V Core Power Supply
48	VIO	Power	1.8V/3.3V Digital I/O Power Supply
43	VIO_SD	Power	1.8V/3.3V Digital I/O SDIO Power Supply
5 30	VDD33	Power	3.3V Digital Power Supply
8 9 14 15 16 19	AVDD18	Power	1.8V Analog Power Supply
10 33 34	AVDD33	Power	3.3V Analog Power Supply
28	LDO11_VOUT	Power	1.1V LV LDO Voltage Output
29	LDO18_VOUT	Power	1.8V LV LDO Voltage Output
12 13 25 26 27	VSS	Ground	Ground Connect these pins to ground

4.5.11 UART interface (debug)

Table 13. UART interface (debug)

QFN Pin No.	Pin name	Type	Supply	Description
44	UART_SIN	I	VIO	UART serial input signal. GPIO[0] input/output
45	UART_SOUT	O	VIO	UART serial output signal. GPIO[1] input/output

4.5.12 Two-wire serial interface

Table 14. Two-wire serial interface

QFN Pin No.	Pin name	Type	Supply	Description
46	SER_CLK	I/O	VIO	Serial interface clock signal. GPIO[2] input/output
47	SER_DAT	I/O	VIO	Serial interface data signal. GPIO[3] input/output

4.5.13 JTAG interface

Table 15. JTAG interface

QFN Pin No.	Pin name	Supply	No pad power state	Reset state	HW state	PD state	Internal PU	PU	PD
2	TCK	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
JTAG test clock (input)									
1	TDI	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
JTAG test data (input)									
3	TDO	VIO	tristate	input	output drive low	tristate	weak PU ena-ble	no	no
JTAG test data (output)									
4	TMS	VIO	tristate	input	input	tristate	nominal PU enable	yes	yes
JTAG controller select (input)									

4.6 Configuration pins

Table 16 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 16. Configuration pins

Configuration bits	Pin name	Configuration function
CON[2]	SER_CLK	Oscillator frequency select 0 = 26 MHz 1 = 38.4 MHz (default)
CON[1]	CON[1]	Firmware boot options 00 = UART (debug) 01 = reserved 10 = SDIO 11 = USB (default)
CON[0]	CON[0]	

5 Power information

5.1 Leakage optimization

For applications not using Wi-Fi, the device can be put into a low-leakage mode of operation. Methods used to achieve this include:

- Using PDn pin
  The power-down state provides the lowest leakage mode of operation. Assert PDn low to enter power-down. This must be met to enter a power-down state.
- All rails powered off

Alternatively, all power rails can be powered off. In this case, the state of the PDn pin is irrelevant.

5.2 Power options

5.2.1 Case 1 - Internal 1.1V and internal 1.8V

Figure 6 shows the power option with the internal 1.1V and internal 1.8V supply.

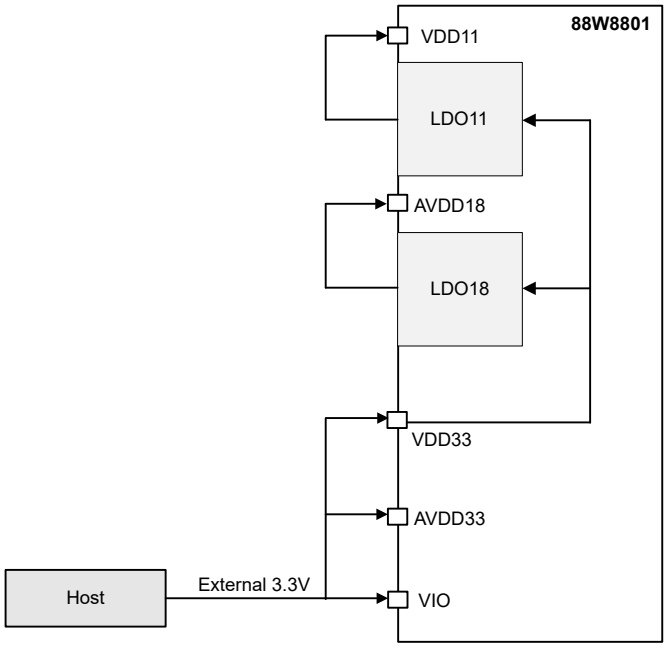


Figure 6. Case 1 - Internal 1.1V and internal 1.8V

5.2.1.1 Power-up sequence for case 1 and PDn driven by host

- External VDD33/VIO/VIO_SD from host
- Internal AVDD18/VDD11 from on-chip LDOs
- PDn driven by host

The following requirements must be met for correct power-up:

- Assert PDn low (active) during VDD33/VIO/VIO_SD ramp-up. Continue to assert low for a minimum of 1 ms after VDD33/VIO/VIO_SD are stable.
- External 3.3V or 1.8V can be used for VIO/VIO_SD as needed by the platform.
- VIO_SD is provided by host if SDIO interface is used.
- VDD33 is used as input to LDO18, which outputs AVDD18.
- VDD33 is used as input to LDO11, which outputs VDD11.
- If an external crystal oscillator is used, then GPIO[0] is used as XOSC_EN.

Figure 7 shows the power-up sequence for case 1 and PDn driven by host.

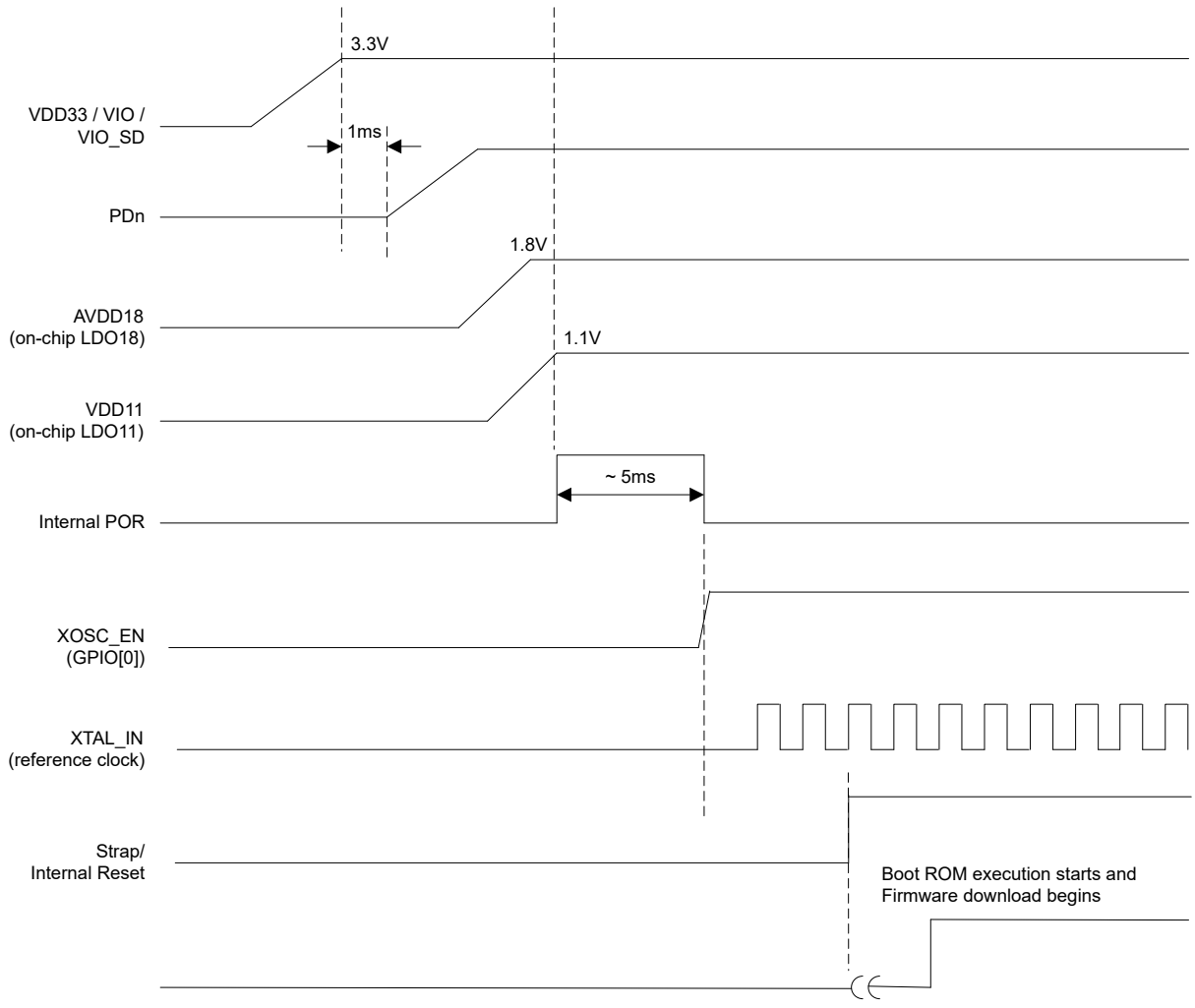


Figure 7. Power-up sequence for case 1 and PDn driven by host

5.2.1.2 Power-up sequence for case 1 and PDn tied to VDD33

- External VDD33/VIO/VIO_SD from host
- Internal AVDD18/VDD11 from on-chip LDOs
- PDn is tied to VDD33

The following requirements must be met for correct power-up:

- Ramp-up time of VDD33 should be < 5 ms.
- VDD33 is used as VIO/VIO_SD.
- VDD33 is used as input to LDO18, which outputs AVDD18.
- VDD33 is used as input to LDO11, which outputs VDD11.
- If an external crystal oscillator is used, then GPIO[0] is used as XOSC_EN.

Figure 8 shows the power-up sequence for case 1 and PDn tied to VDD33.

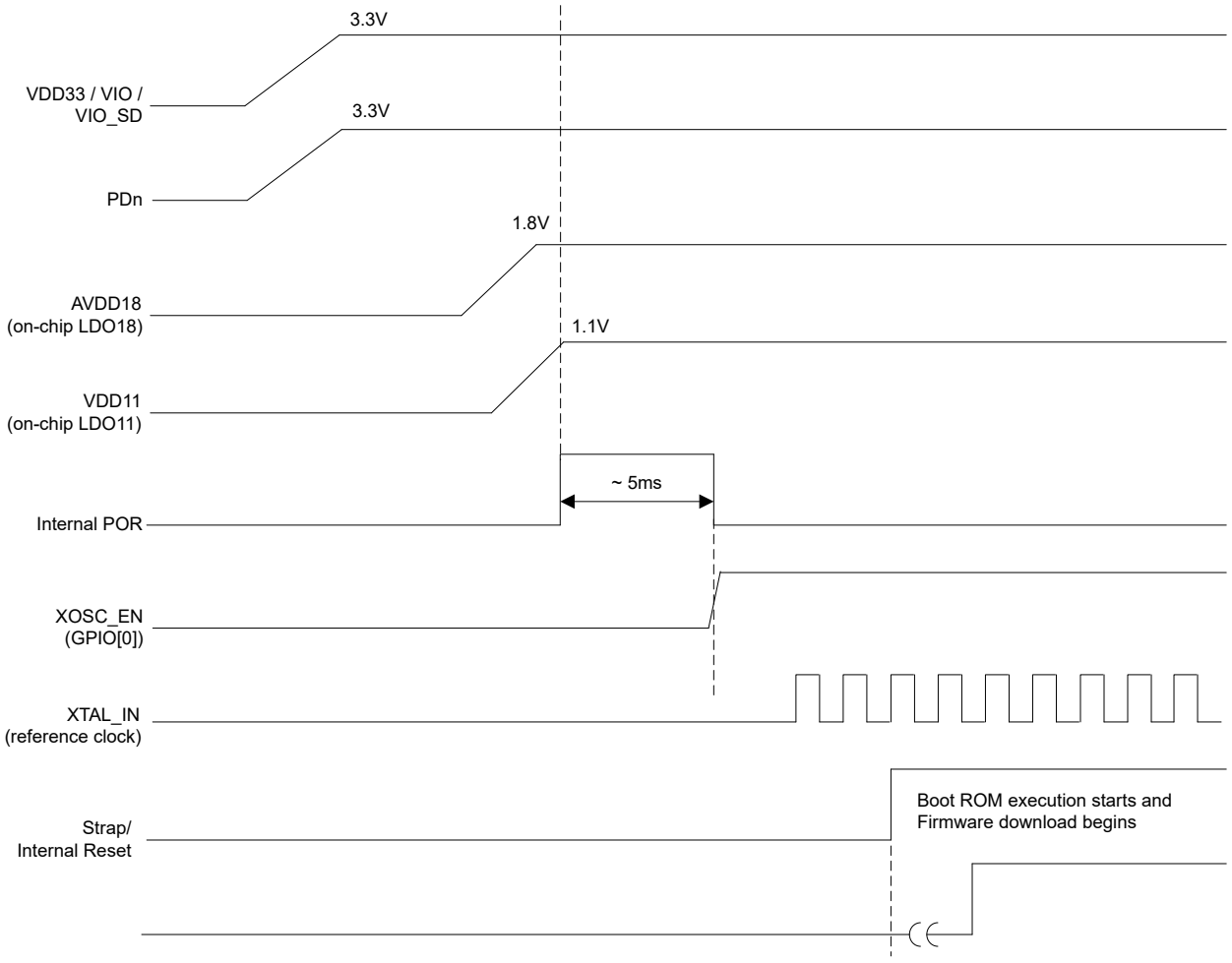


Figure 8. Power-up sequence for case 1 and PDn tied to VDD33

5.2.2 Case 2 - Internal 1.1V and external 1.8V

Figure 9 shows the second power option with 1.1V internal voltage supply and 1.8V external supply.

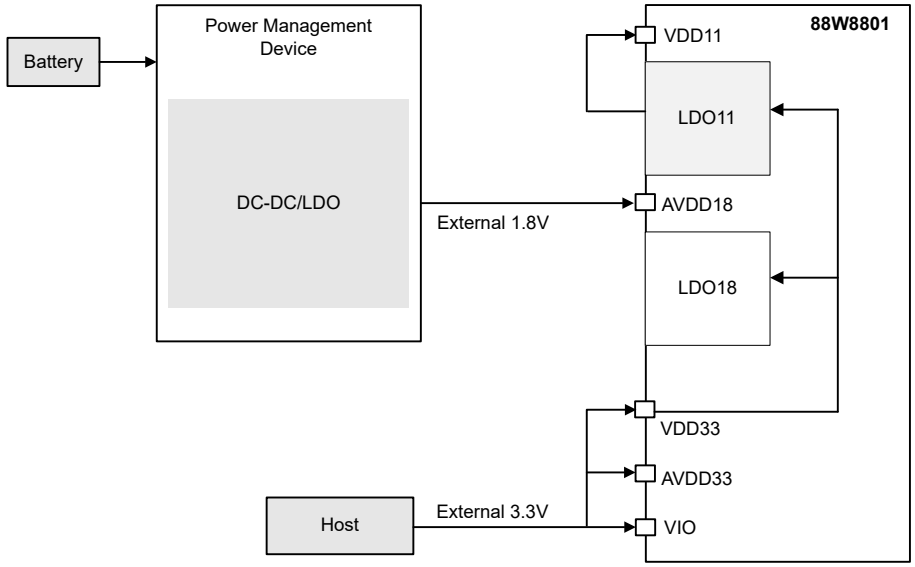


Figure 9. Power options, case 2—Internal 1.1V, external 1.8V

5.2.2.1 Power-up sequence for case 2

- External VDD33/VIO/VIO_SD from host
- External AVDD18
- Internal VDD11 from on-chip LDO
- PDn is driven by host

The following requirements must be met for correct power-up:

- Assert PDn low (active) during VDD33/VIO/VIO_SD and AVDD18 ramp-up. Continue to assert low for a minimum of 1 ms after VDD33/VIO/VIO_SD and AVDD18 are stable.
- External 3.3V or 1.8V can be used for VIO/VIO_SD as needed by the platform.
- VIO_SD is provided by host if SDIO interface is used.
- VDD33 is used as input to LDO11, which outputs VDD11.
- If an external crystal oscillator is used, then GPIO[0] is used as XOSC_EN.

Figure 10 shows the power-up sequence for the power option with internal 1.1V and external 1.8V.

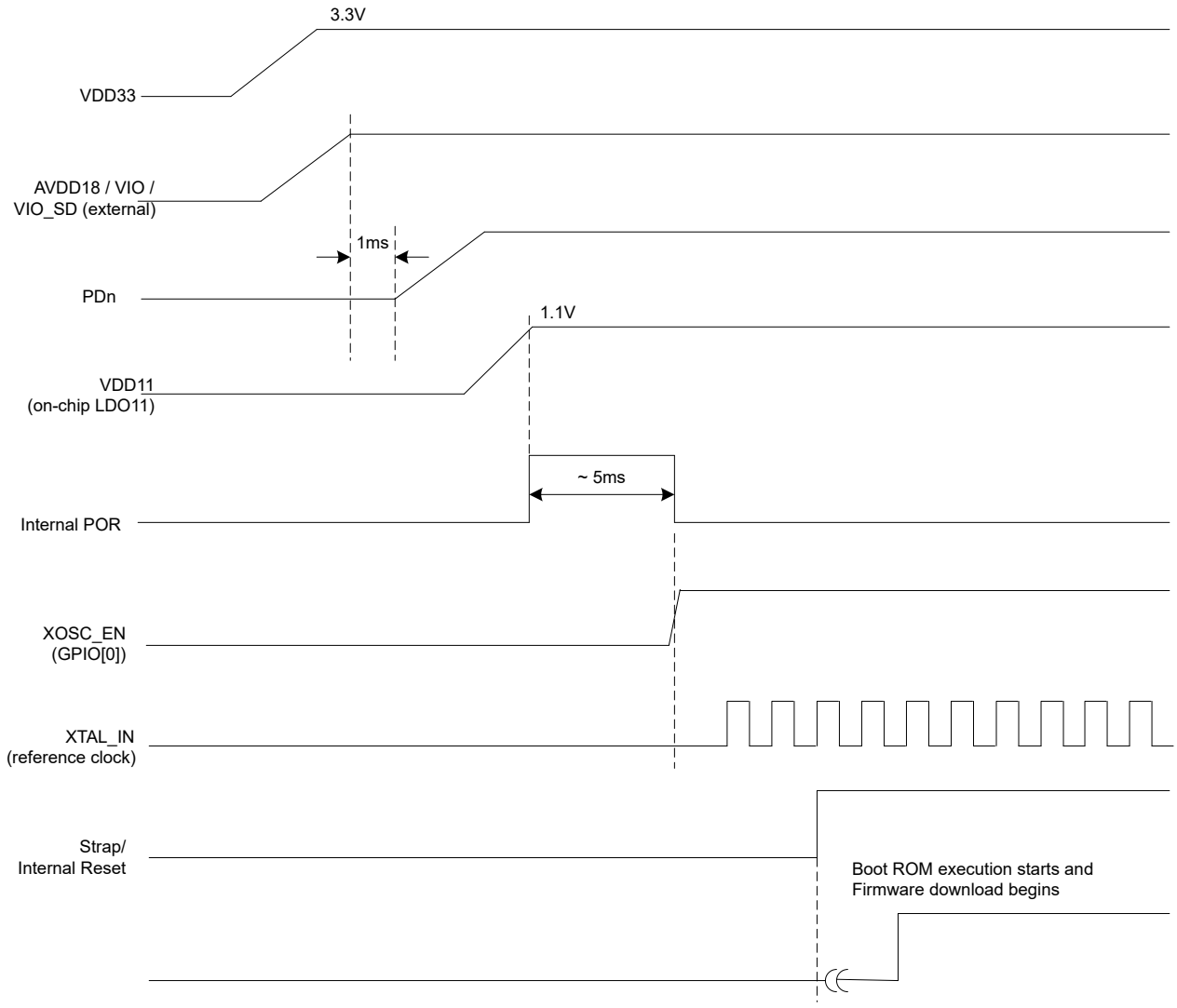


Figure 10. Power-up sequence for case 2

6 Absolute maximum ratings

Table 17. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD11	Power supply voltage with respect to VSS	--	--	1.1	1.26	V
VIO	Power supply voltage with respect to VSS	--	--	1.8	2.2	V
			--	3.3	4.0	V
VIO_SD	Power supply voltage with respect to VSS	--	--	1.8	2.2	V
			--	3.3	4.0	V
VDD33	Power supply voltage with respect to VSS	--	--	3.3	4.0	V
AVDD18	Power supply voltage with respect to VSS	--	--	1.8	1.98	V
AVDD33	Power supply voltage with respect to VSS	--	--	3.3	4.0	V
$T_{STORAGE}$	Storage temperature	--	-55	--	+125	°C
V_{ESD}	electrocstatic discharge voltage	human body model (HBM)[1]	-2	--	+2	kV
		charged device model (CDM)[2]	-500	--	+500	V

[1] According to JESD22-A114F
[2] According to JESD22-C101E

7 Recommended operating conditions

Table 18. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD11	1.1V core power supply	--	--	1.1	1.21	V
VIO	1.8V/3.3V digital I/O power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.63	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.63	V
VDD33	3.3V I/O power supply	--	2.97	3.3	3.63	V
AVDD18	1.8V analog power supply	--	1.71	1.8	1.89	V
AVDD33	3.3V analog power supply	--	2.97	3.3	3.63	V
T_A	Ambient operating temperature	Commercial	0	--	70	°C
		Extended	-30	--	85	°C
		Industrial	-40	--	85	°C
T_J	Maximum junction temperature	--	--	--	125	°C

8 Electrical specifications

8.1 GPIO interface specifications

8.1.1 VIO DC characteristics

8.1.1.1 VIO DC characteristics - 1.8V operation

Table 19. DC electricals—1.8V operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.1.1.2 VIO DC characteristics - 3.3V operation

Table 20. DC electricals—3.3V operation (VIO)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.2 RF front-end control interface specifications

Table 21. DC electricals—3.3V operation (VDD33)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VDD33	--	VDD33+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VDD33	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VDD33-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.3 Wi-Fi radio specifications

8.3.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip output port.

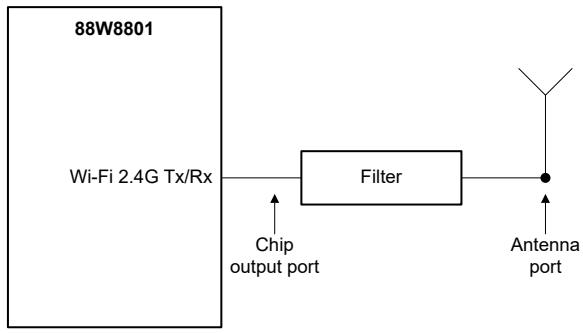


Figure 11. Radio performance measurement points

8.3.2 Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, typical voltage, across frequency range, and at the chip output port. See Section 7 "Recommended operating conditions" for typical voltage levels.*

Table 22. Wi-Fi receiver performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	--	2500	MHz
Receiver input IP3 at RF high gain (In-band)	Rx input IP3 when LNA in high gain mode (24 dB) at chip input	--	-15	--	dBm
Receiver sensitivity 802.11b	1 Mbit/s	--	-98	--	dBm
	2 Mbit/s	--	-95	--	dBm
	5.5 Mbit/s	--	-92	--	dBm
	11 Mbit/s	--	-89	--	dBm
Receiver sensitivity 802.11g	6 Mbit/s	--	-91	--	dBm
	9 Mbit/s	--	-90	--	dBm
	12 Mbit/s	--	-88	--	dBm
	18 Mbit/s	--	-86	--	dBm
	24 Mbit/s	--	-83	--	dBm
	36 Mbit/s	--	-80	--	dBm
	48 Mbit/s	--	-75	--	dBm
	54 Mbit/s	--	-74	--	dBm
Receiver sensitivity 802.11n - HT20	MCS0	--	-91	--	dBm
	MCS1	--	-88	--	dBm
	MCS2	--	-86	--	dBm
	MCS3	--	-84	--	dBm
	MCS4	--	-80	--	dBm
	MCS5	--	-76	--	dBm
	MCS6	--	-74	--	dBm
	MCS7	--	-72	--	dBm

8.3.3 Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, typical voltage, across frequency range, and at chip output port. See Section 7 "Recommended operating conditions" for typical voltage levels.*

Table 23. Wi-Fi transmitter performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	--	2500	MHz
Transmit output saturation power at chip output port	2.4 GHz—IEEE 802.11n/g/b	--	26	--	dBm
Transmit carrier suppression (CW)	--	--	-36	--	dB
Transmit I/Q suppression with IQ calibration	--	--	-45	--	dBc
Transmit power (EVM and mask compliant) 20MHz	802.11b	--	19	--	dBm
	OFDM 64-QAM (MCS7)	--	17	--	dBm
Transmit carrier supression (modulated signal)	802.11g OFDM 54 Mbit/s, at 16dBm	--	29	--	dB

8.3.4 Local oscillator

Table 24. Local oscillator

Parameter	Condition	Min	Typ	Max	Unit
Phase noise	Measured at 2.438 GHz, at 100kHz offset	--	-103	--	dBc/Hz
Integrated RMS phase noise at RF output (from 1 kHz–10 MHz)	Reference clock frequency= 26MHz or 38.4MHz (2.4GHz)	--	0.6	--	degree
Frequency resolution	--	0.02	--	--	kHz

8.4 Current consumption

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, across frequency and typical value. The power consumption data was collected with SDIO interface configuration.*

Table 25. Current consumption

Mode	Conditions	3.3V	Unit
Sleep mode	Wi-Fi in deep sleep mode	0.14	mA
IEEE power save (average)[1] (Beacon interval: 100 msec)	DTIM-1	1.28	mA
	DTIM-3	0.53	mA
	DTIM-5	0.37	mA
Wi-Fi receive	802.11b, 11 Mbit/s	68	mA
	802.11g, 54 Mbit/s	74	mA
	802.11n, HT20 MCS7	82	mA
Wi-Fi transmit	802.11b, 11 Mbit/s at 18 dBm	359	mA
	802.11g, 54 Mbit/s at 15 dBm	290	mA
	802.11n, HT20 MCS7 at 13 dBm	285	mA

[1] Measured using the internal LDO

8.5 SDIO host interface specifications

8.5.1 VIO_SD DC characteristics

8.5.1.1 VIO_SD DC characteristics - 1.8V operation

Table 26. DC electricals—1.8V operation (VIO_SD)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.5.1.2 VIO_SD DC characteristics - 3.3V operation

Table 27. DC electricals—3.3V operation (VIO_SD)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

8.5.2 SDIO host interface specifications

The 88W8801 SDIO host interface pins are powered from the VIO_SD voltage supply.

See the specifications in Section 8.5.1 "VIO_SD DC characteristics".

The SDIO electrical specifications are identical for the 1-bit SDIO and 4-bit SDIO modes.

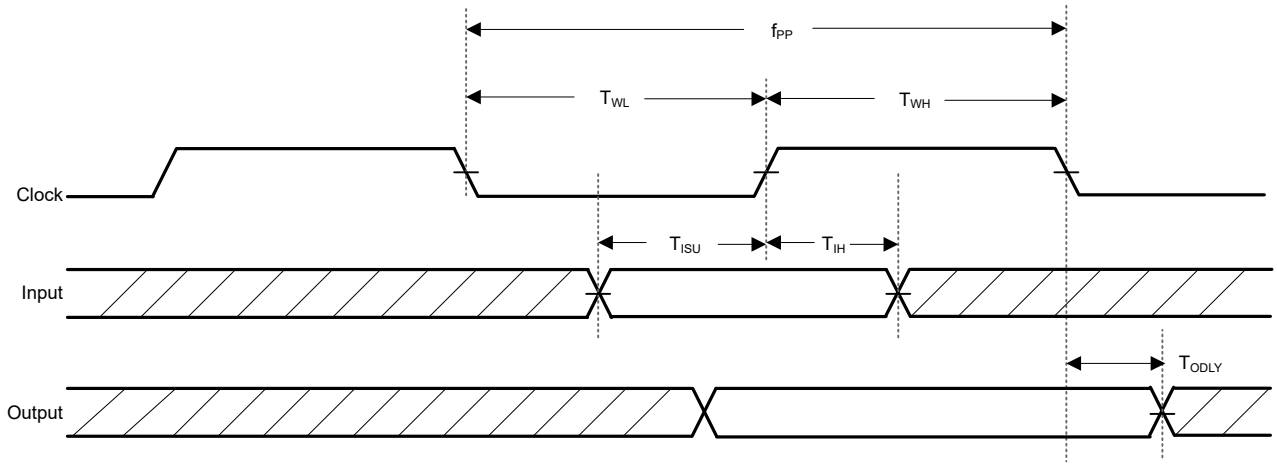


Figure 12. SDIO protocol timing diagram—Normal mode

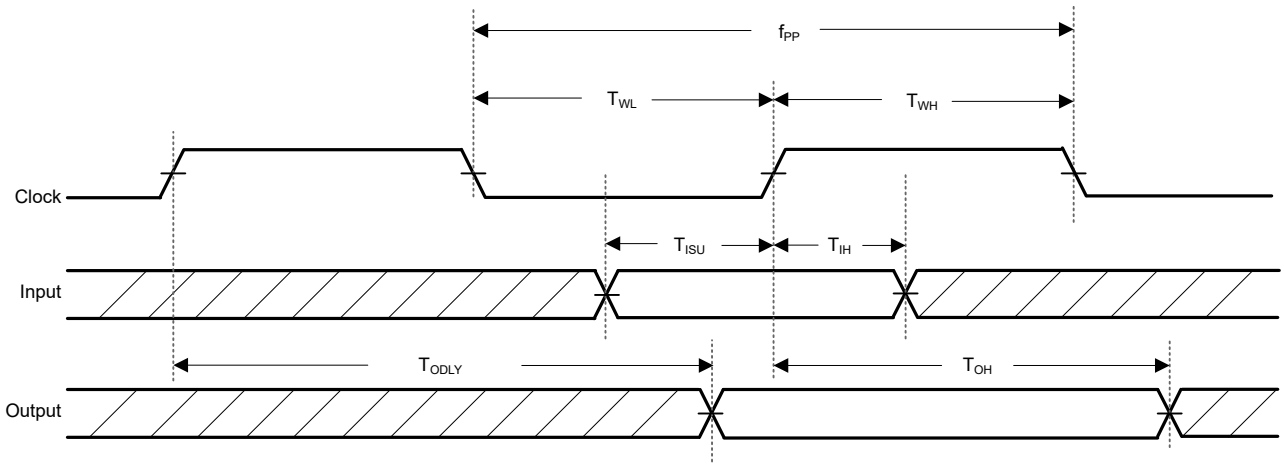


Figure 13. SDIO protocol timing diagram—High-speed mode

Table 28. SDIO timing data[1]

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	14	ns
		High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

[1] The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

8.6 USB 2.0 host interface specifications

The USB 2.0 host interface pins are powered by AVDD33 voltage supply.

Table 29. Electrical characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply current						
I_{CCHPF}	High-power function	--	--	--	500	mA
I_{CCLPF}	Low-power function	--	--	--	100	mA
I_{CCINIT}	Unconfigured function	--	--	--	100	mA
I_{CCSH}	Suspended high-power device	--	--	--	2.5	mA
I_{CCSL}	Suspended low-power device	--	--	--	500	µA
Input levels for low/full-speed						
V_{IH}	Input high voltage (driven)	--	2.0	--	--	V
V_{IHZ}	Input high voltage (floating)	--	2.7	--	3.6	V
V_{IL}	Input low voltage	--	--	--	0.8	V
V_{DI}	Differential input sensitivity	--	0.2	--	--	V
V_{CM}	Differential common mode range	--	0.8	--	2.5	V
Input levels for high-speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	--	100	--	150	mV
V_{HSDSC}	High-speed disconnect detec-tion threshold (differential signal amplitude)	--	525	--	625	mV
--	High-speed differential input signaling levels	Specified by eye pattern templates; see Section 7.1.7.2 in the USB 2.0 specification.	--	--	--	--
V_{HSCM}	High-speed data signaling common mode voltage range	--	-50	--	500	mV
Output levels for low/full-speed						
V_{OL}	Output low voltage	--	0.0	--	0.3	V
V_{OH}	Output high voltage (driven)	--	2.8	--	3.6	V
V_{OSE1}	Output SE1 voltage	--	0.8	--		V
V_{CRS}	Output signal crossover voltage	--	1.3	--	2.0	V

Table 29. Electrical characteristics*...continued*

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels for high-speed						
V_{HSOI}	High-speed idle level	--	-10.0	--	10.0	mV
V_{HSOH}	High-speed data signaling high	--	360	--	440	mV
V_{HSOL}	High-speed data signaling low	--	-10.0	--	10.0	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	--	700	--	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	--	-900	--	-500	mV
Decoupling capacitance						
C_{RPB}	Upstream facing port bypass capacitance	--	1.0	--	10.0	µF
Input capacitance for low/full-speed						
C_{INUB}	Upstream facing port capacitance (without cable)	--	--	--	100	pF
C_{EDGE}	Transceiver edge rate control capacitance	--	--	--	75	pF
Input impedance for high-speed						
--	TDR spec for high-speed termination	Differential impedance	80	--	100	W
Terminations						
R_{PUI}	Bus pull-up resistor on upstream port (idles bus)	--	0.900	--	1.575	kΩ
R_{PUA}	Bus pull-up resistor on upstream port (receiving)	--	1.425	--	3.090	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low/full-speed)	--	300	--	--	kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up resistor (R_{PU})	--	3.0	--	3.6	V
Terminations in high-speed						
V_{HSTERM}	Termination voltage in high-speed	--	-10	--	10	mV

Table 30. High-speed source electrical characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
T_{HSR}	Rise Time (10% - 90%)	--	500	--	--	ps
T_{HSF}	Fall Time (10% - 90%)	--	500	--	--	ps
--	Driver waveform requirements	Specified by eye pattern templates in Section 7.1.2 in the USB 2.0 specification.	--	--	--	--
Z_{HS-DRV}	Driver output resistance (also serves as high-speed termination)	--	40.5	--	49.5	W
Clock timings						
T_{HSDRAT}	High-speed data rate	--	479.760	--	480.240	Mb/s
T_{HSFRAM}	Microframe interval	--	124.9375	--	125.0625	µs
T_{HSRFI}	Consecutive microframe interval difference	--	--	--	4 high-speed bit times	--
High-speed data timings						
--	Data source jitter	Specified by eye pattern templates in Section 7.1.2.2 in the USB 2.0 specification.	--	--	--	--
--	Receiver jitter tolerance	Specified by eye pattern templates in Section 7.1.2.2 in the USB 2.0 specification.	--	--	--	--

Table 31. Full-speed source electrical characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
T_{FR}	Rise time	--	4	--	20	ns
T_{FF}	Fall time	--	4	--	20	ns
T_{FRFM}	Differential rise and fall time matching	T_{FR}/T_{FF}	90	--	111.11	%
Clock timing						
$T_{FDRATHS}$	Full-speed data rate	Average bit rate	11.9940	--	12.0060	Mb/s
T_{FDRATE}	Frame interval	--	0.9995	--	1.00005	ms
T_{RFI}	Consecutive frame interval difference	No clock adjustment	--	--	42	ms
Full-speed data timing						
T_{DJ1}	Source jitter total to next transition (including frequency tolerance)	--	-3.5	--	3.5	ns
T_{DJ2}	Source jitter total for paired tran-sitions (including frequency tolerance)	--	-4	--	4	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition	--	-2	--	5	ns
T_{JR1}	Receiver jitter to next transition	--	-18.5	--	18.5	ns
T_{JR2}	Receiver jitter to next transition	--	-9	--	9	ns
T_{FEOPT}	Source SE0 interval of EOP	--	160	--	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	--	82	--	--	ns
T_{FST}	Width of SE0 interval during differential transition	--	--	--	14	ns

Table 32. Device event timing characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SIGATT}	Time from internal power good to device pulling D +/D- beyond V_{IHZ} (min) (signaling attach)	--	--	--	100	ms
T_{ATTDB}	Debounce interval provided by USB system software after attach	--	--	--	100	ms
T_{2SUSP}	Maximum time a device can draw power > suspend power when bus is continuously in idle state	--	--	--	10	ms
$T_{SUSAVGI}$	Maximum duration of suspend averaging interval	--	--	--	1	s
T_{WTRSM}	Period of idle bus before device can initiate resume	Device must be remote-wake-up enabled	5	--	--	ms
T_{DRSMUP}	Duration of driving resume upstream	--	1	--	15	ms
T_{RSMCY}	Resume recovery time	Provided by USB system software	10	--		ms
T_{RSTRCY}	Reset recovery time	--	--	--	10	ms
T_{IPD}	Inter-packet delay (for low/full-speed)	--	2	--		bit times
$T_{RSPIPD1}$	Inter-packet delay for device response with detachable cable for low/full-speed	--	--	--	6.5	bit times
$T_{RSPIPD2}$	Inter-packet delay for device response with captive cable for low/full-speed	--	--	--	7.5	bit times
$T_{DSETADDR}$	SetAddress() completion time	--	--	--	50	ms
$T_{DRQCMPLTND}$	Time to complete standard request with no data	--	--	--	50	ms
$T_{DRETDATA1}$	Time to deliver first and subsequent (except last) data for standard request	--	--	--	500	ms
$T_{DRETDATAN}$	Time to deliver last data for standard request	--	--	--	50	ms
$T_{HSRSPIPD2}$	Inter-packet delay for device response with captive cable (high-speed)	--	--	--	192 bit times + 52 ns	--
Reset Handshake Protocol						

Table 32. Device event timing characteristics*...continued*

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{FILTSE0}$	Time for which a suspended high-speed capable device must see a continuous SE0 before beginning the high-speed detection handshake	--	2.5	--	--	µs
$T_{WTRSTFS}$	Time for which a high-speed capable device operating in non-suspended full-speed must wait after start of SE0 before beginning the high-speed detection handshake	--	2.5	--	3000	µs
T_{WTREV}	Time for which a high-speed capable device operating in high-speed must wait after start of SE0 before reverting to full-speed	--	3.0	--	3.125	ms
$T_{WTRSTHS}$	Time for which a device must wait after reverting to full-speed before sampling the bus state for SE0 and beginning the high-speed detection handshake	--	100	--	875	µs
T_{UCH}	Minimum duration of a Chirp K from a high-speed capable device within the reset protocol	--	1.0	--	--	ms
T_{UCHEND}	Time after start of SE0 by which a high-speed capable device is required to have completed its Chirp K within the reset protocol	--	--	--	7.01	ms
T_{WTHS}	Time after end of upstream chirp at which device enters the high-speed default state if downstream chirp is detected	--	--	--	500	µs
T_{WTFS}	Time after end of upstream chirp at which device reverts to full-speed default stat if no down-stream chirp is detected	--	1.0	--	2.5	ms

Table 33. LPM timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$TL1_{Residency}$	L1 residency	--	50	--	>50	µs
$TL1_{TokenRetry}$	Device delay before transitioning to L1 after transmitting ACK	--	8	--	10	µs
$TL1_{HubDrvResume1}$	Host initiated L1 exit host drives resume time	--	50 ±1	--	1200 ±1	µs
$TL1_{DevDrvResume}$	Device initiated L1 exit Device drives resume time	--	50 ±1	--	--	µs
$TL1_{ExitDevRecovery}$	L1 exit device recovery time	--	10	--	--	µs
$TL1_{ExitLatency1}$	L1 exit latency (host initiated)	--	60	--	1210	µs
$TL1_{ExitLatency2}$	L1 exit latency (device initiated)	--	70	--	1000	µs

8.7 Clock interface specifications

8.7.1 Single-ended clock input mode

Table 34. CMOS mode[1]

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	AVDD18 - 0.5	AVDD18	1.98	V
V_{IL}	Input low voltage	--	0	0	0.4	V

[1] Typical input capacitance is approximately 2 pF and input resistance is >20 kΩ.

Table 35. Phase noise—2.4 GHz operation

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-137	dBc/Hz
	Offset = 100 kHz	--	--	-143	dBc/Hz
	Offset > 1 MHz	--	--	-143	dBc/Hz
Fref = 38.4 MHz	Offset = 1 kHz	--	--	-123	dBc/Hz
	Offset = 10 kHz	--	--	-134	dBc/Hz
	Offset = 100 kHz	--	--	-140	dBc/Hz
	Offset > 1 MHz	--	--	-140	dBc/Hz

8.7.2 Crystal specifications

Table 36. Crystal specifications

Parameter	Conditions	Min	Typical	Min	Unit
Fundamental frequencies	--	--	26, 38.4	--	MHz
Frequency tolerance	Over operating temperature	--	< ±10	--	ppm
	Over process at 25ºC	--	< ±10	--	ppm
SMD and AT cut height	--	--	<1.2	--	mm
Load capacitor	--	--	10	--	pF
Maximum series resistance	--	--	60	--	Ω
Resonance mode	--	--	A1, Fundamental	--	--

8.8 Two-wire serial interface specifications

The 2-wire serial interface pins are powered by the VIO voltage supply.

See the specifications in Section 8.1.1 "VIO DC characteristics".

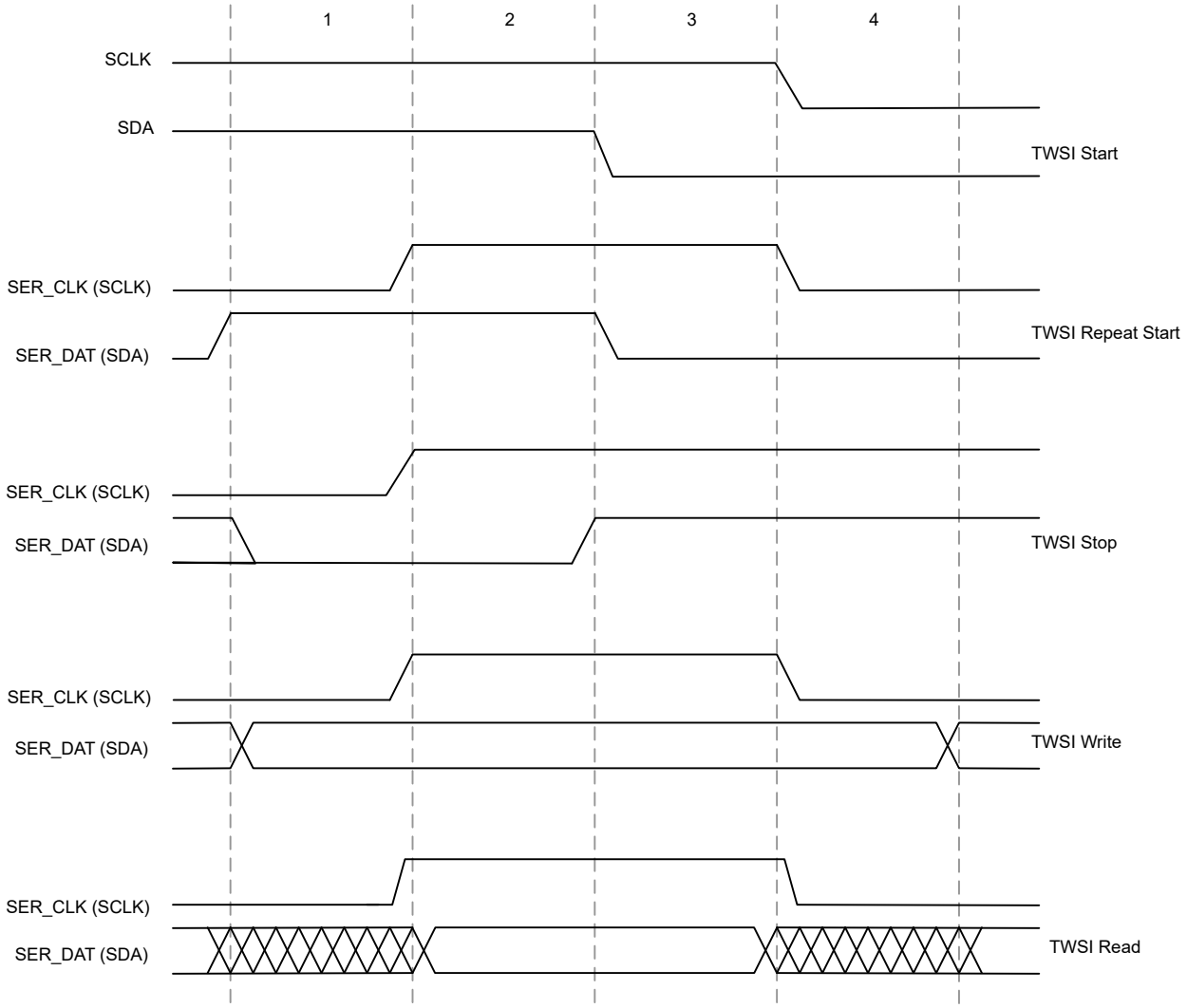


Figure 14. Two-wire serial interface signaling

8.9 UART (debug) interface specifications

The UART pins are powered by the VIO voltage supply.

See the specifications in Section 8.1.1 "VIO DC characteristics".

8.10 JTAG interface specifications

The JTAG test interface pins are powered by VIO voltage supply.

See the specifications in Section 8.1.1 "VIO DC characteristics".

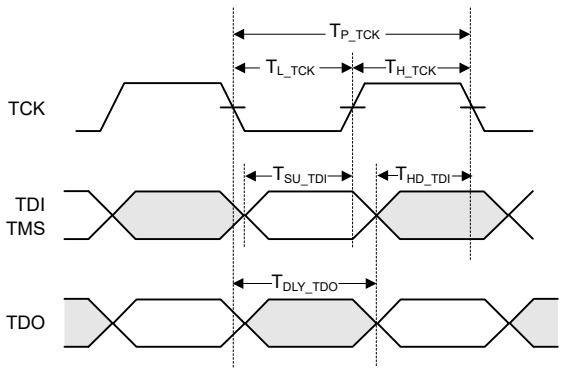


Figure 15. JTAG timing diagram

Table 37. JTAG timing data[1]

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{P_TCK}	TCK period	--	40	--	--	ns
T_{H_TCK}	TCK high	--	12	--	--	ns
T_{L_TCK}	TCK low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO delay	--	0	--	15	ns

[1] Does not apply to CPU JTAG enabled by the TMS_CPU pin.

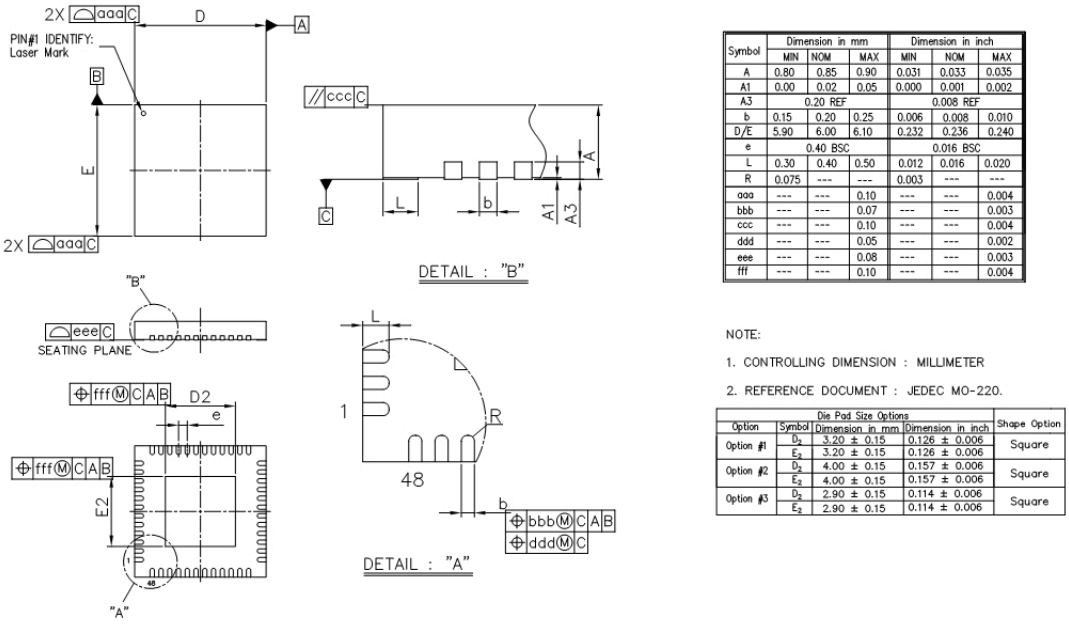
9 Package information

9.1 Package thermal conditions

Table 38. Thermal conditions—QFN

Symbol	Parameter	Conditions	Typ	Unit
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 x 4.5 inch, 4-layer PCB no air flow	34.6	°C/W
		JEDEC 3 x 4.5 inch, 4-layer PCB 1 meter/sec air flow	33.9	°C/W
		JEDEC 3 x 4.5 inch, 4-layer PCB 2 meter/sec air flow	32.8	°C/W
		JEDEC 3 x 4.5 inch, 4-layer PCB 3 meter/sec air flow	32.3	°C/W
Ψ_{JT}	Thermal characteristic parameter[1] Junction to top center of package. $\Psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top center of package	JEDEC 3 x 4.5 inch, 4-layer PCB no air flow	9.4	°C/W
Ψ_{JB}	Thermal characteristic parameter[1] Junction to top center of package. $\Psi_{JT} = (T_J - T_B)/P$ T_B = power dissipation from top center of package	JEDEC 3 x 4.5 inch, 4-layer PCB no air flow	21.4	°C/W
θ_{JC}	Thermal resistance[1] Junction to case of the package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = power dissipation from top of package	JEDEC 3 x 4.5 inch, 4-layer PCB no air flow	23.4	°C/W
θ_{JB}	Thermal resistance[1] Junction to board of package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from bottom of package to PCB surface	JEDEC 3 x 4.5 inch, 4-layer PCB no air flow	21.5	°C/W

9.2 Package mechanical drawing



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
aaa	---	---	0.10	---	---	0.004
bbb	---	---	0.07	---	---	0.003
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

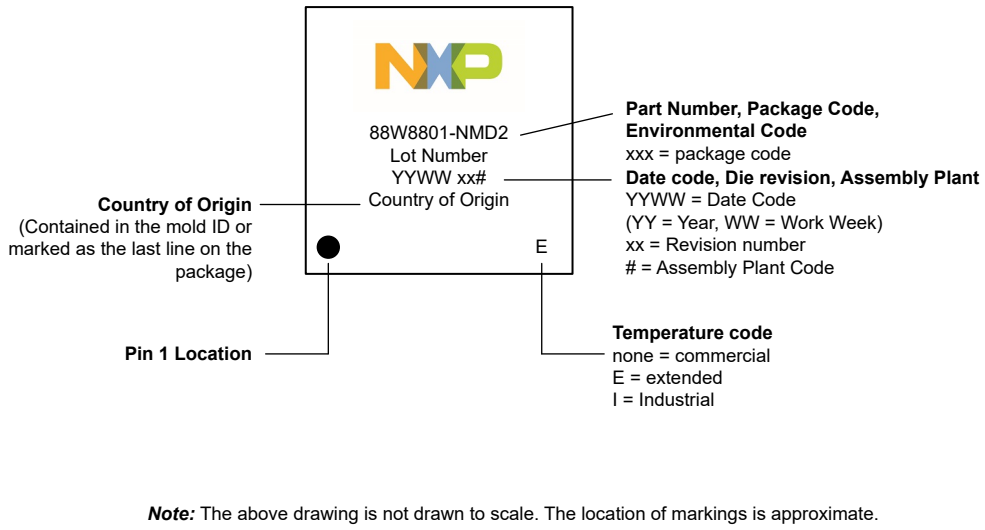
Die Pad Size Options				
Option	Symbol	Dimension in mm	Dimension in inch	Shape Option
Option #1	D_2	3.20 ± 0.15	0.126 ± 0.006	Square
	E_2	3.20 ± 0.15	0.126 ± 0.006	
Option #2	D_2	4.00 ± 0.15	0.157 ± 0.006	Square
	E_2	4.00 ± 0.15	0.157 ± 0.006	
Option #3	D_2	2.90 ± 0.15	0.114 ± 0.006	Square
	E_2	2.90 ± 0.15	0.114 ± 0.006	

Figure 16. Mechanical drawing of 48-pin QFN package

- The QFN package uses Epad size Option #2 only. See Section 9.1 "Package thermal conditions" and Section 9.3 "Package marking".

9.3 Package marking

Figure 17 shows the marking and pin 1 location for 88W8801 parts.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 17. Package marking and pin 1 location

10 Acronyms and abbreviations

Table 39. Acronyms and abbreviations

Acronym	Definition
A2DP	Advanced Audio Distribution Profiles
ABR	Automatic Baud Rate
ACK	Acknowledgment
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Correction
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIFS	Arbitration Interframe Space
AoA	Angle of Arrival
AoD	Angle of Departure
AP	Access Point
APB	Advanced Peripheral Bus
API	Application Program Interface
aQFN	Advanced Quad Flat Non-leaded Package
ARM	Advanced RISC Machine
ATIM	Announcement Traffic Indication Message
BAMR	Base Address Mask Register
BAR	Base Address Register
BBU	Baseband Processor Unit
BCB	Benzocyclobutene (flip chip bump process)
BDR	Basic Data Rate
BER	Bit Error Rate
BOM	Bill of Materials
BR	Baud Rate
BSS	Basic Service Set
BSSID	Basic Service Set Identifier
BTU	Bluetooth Baseband Unit
BRF	Bluetooth RF Unit
BWQ	Bandwidth Queue
CBC	Cipher Block Chaining
CBP	Contention-Based Period
CCA	Clear Channel Assessment

Table 39. Acronyms and abbreviations...*continued*

Acronym	Definition
CCK	Complementary Code Keying
CCMP	Counter Mode CBC-MAC Protocol
CDE	Close Descriptor Enable
CFP	Contention-Free Period
CFQ	Contention-Free Queue
CID	Connection Identifier
CIS	Card Information Structure
CIU	CPU Interface Unit
CMD	Command
CMQ	Control Management Queue
CRC	Cyclic Redundancy Check
CS	Card Select
CSMA/CA	Carrier Sense Multiple Access / Collision Avoidance
CSMA/CD	Carrier Sense Multiple Access / Collision Detection
CSU	Clocked Serial Unit
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCD	Device Controller Driver
DCE	Data Communication Equipment
DCF	Distributed Coordination Function
DCLA	Direct Current Level Adjustment
DCLB	Digital Contactless Bridge
DCU	DMA Controller Unit
DFS	Dynamic Frequency Selection
DIFS	Distributed Interframe Space
DMA	Direct Memory Access
dQH	Device Queue Head
DQPSK	Differential Quadrature Phase Shift Keying
DSM	Distribution System Medium
DSP	Digital Signal Processor
DSRC	Dedicated Short Range Communications
dTD	Linked List Transfer Descriptors
DTIM	Delivery Traffic Indication Message
DVSC	Digital Voltage Scaling Control
EAP	Extensible Authentication Protocol

Table 39. Acronyms and abbreviations...*continued*

Acronym	Definition
EBRAM	Extended Block Random Access Memory
ED	Energy Detect
EDCA	Enhanced Distributed Channel Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EIFS	Extended Interframe Space
EMC	Electromagnetic Compatibility
ERP-OFDM	Extended Rate PHY-Orthogonal Frequency Division Multiplexing
ETSI	European Telecommunications Standards Institute
eWLP	Embedded Wafer Level Package
FAE	Field Application Engineer
FCC	Federal Communications Commission
FIFO	First In First Out
FIPS	Federal Information Processing Standards
FIQ	Fast Interrupt Request
FW	Firmware
GATT	Generic Attribute Profile
GCMP	Galois/Counter Mode Protocol
GI	Guard Interval
GPIO	General Purpose Input/Output
GPL	General Public License
GPU	General Purpose Input/Output Unit
HID	Human Interface Device
HIU	Host Interface Unit
HOGP	HID Over GATT Profile
HSP	Hands-Free Profile
HT	High Throughput
HW	Hardware
I/Q	Inphase/Quadrature
IB	InBand
IBSS	Independent Basic Service Set
ICE	In-Circuit Emulator (or Emulation)
ICR	Interrupt Cause Register
ICU	Interrupt Controller Unit
ICV	Integrity Check Value
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers

Table 39. Acronyms and abbreviations*...continued*

Acronym	Definition
IEMR	Interrupt Event Mask Register
I/F	Interface
IFS	Interframe Space
IMR	Interrupt Mask Register
IPG	Inter-Packet Gap
IPsec	Internet Protocol Security
IR	Infrared
IRQ	Interrupt Request
ISA	Instruction Set Architecture
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific, and Medical
ISMR	Interrupt Status Mask Register
ISR	Interrupt Status Register
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
LDPC	Low Density Parity Check
LE	Low Energy
LED	Light Emitting Diode
LME	Layer Management Entity
LNA	Low Noise Amplifier
LPM	Low Power Management
LQFN	Low Quad Flat Non-leaded
LSb	Least Significant bit
LSB	Least Significant Byte
LSP	Low-Speed Peripheral
LTE	Long Term Evolution
MAC	Media/Medium Access Controller
MC	Memory Controller
MCS	Modulation and Coding Scheme
MCU	MAC Control Unit
MDI	Modem Data Interface
MIB	Management Information Base
MIC	Message Integrity Code
MII	Media Independent Interface
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions Per Second

Table 39. Acronyms and abbreviations...*continued*

Acronym	Definition
MLME	MAC Sublayer Management Entity
MMI	Modem Management Interface
MMPDU	MAC Management Protocol Data Unit
MMU	Memory Management Unit
MPDU	MAC Protocol Data Unit
MSb	Most Significant bit
MSB	Most Significant Byte
MSDU	MAC Service Data Unit
MU-MIMO	Multi-User MIMO
MU-PPDU	Multi-User PPDU
MWS	Mobile Wireless System Multimedia Wireless System
NAV	Network Allocation Vector
NDP	Null Data Packet
NL	No Load
NPTR	Next Descriptor Pointer
OCB	Outside the Context of a BSS
OFDM	Orthogonal Frequency Division Multiplexing
OID	Object Identifier
OOB	Out of Band
OTP	One Time Programmable
P2P	Peer-to-Peer
PA	Power Amplifier
PAD	Packet Assembler/Disassembler
PBU	Peripheral Bus Unit
PC	Point Coordinator
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse Code Modulation
PDn	Power Down
PDU	Protocol Data Unit
PEAP	Protected EAP
PHY	Physical Layer
PIFS	Priority Interframe Space

Table 39. Acronyms and abbreviations...*continued*

Acronym	Definition
PLL	Phase-Locked Loop
PLME	Physical Layer Management Entity
PMU	Power Management Unit
POST	Power-On Self Test
PPDU	PHY Protocol Data Unit
PPK	Per-Packet Key
PPM	Pulse Position Modulation
PSK	Pre-Shared Keys
PTA	Packet Traffic Arbitration
PWK	Pairwise Key
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non-leaded Package
QoS	Quality of Service
RA	Receiver Address
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RFID	Radio Frequency Identification
RIFS	Reduced Interframe Space
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSSI	Receiver Signal Strength Indication
RTS	Request to Send
RTU	General Purpose Timer Unit
RU	Resource Unit
SA	Source Address
SAP	Service Access Point
SCLK	Serial Interface Clock
SDA	Serial Interface Data
SE	Secure Element
SFD	Start of Frame Delimiter
SIFS	Short Interframe Space
SISO	Single Input Single Output
SIU	Serial Interface Unit (UART)
SJU	System/Software JTAG Controller Unit
SM	Switch Module

Table 39. Acronyms and abbreviations*...continued*

Acronym	Definition
SMI	Serial Management Interface
SNR	Signal-to-Noise Ratio
SO	Serial Out
SoC	System-on-Chip
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SQU	Internal SRAM Unit
SRWB	Serial Interface Read Write
SS	Service Set
SSID	Service Set Identifier
STA	Station
STBC	Space-Time Block Code
SWD	Serial Wire Debug
SWP	Single Wire Protocol
TA	Transmitter Address
TBG	Time Base Generator
TBTT	Target Beacon Transmission Time
TCM	Tightly Coupled Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TCQ	Traffic Category Queue
TIM	Traffic Indication Map
TKIP	Temporal Key Integrity Protocol
TPC	Transmit Power Control
TQFP	Thin Quad Flat Pack
TRPC	Transmit Rate-based Power Control
TSC	TKIP Sequence Counter
TSF	Timing Synchronization Function
TWT	Target Wait Time
UART	Universal Asynchronous Receiver/Transmitter
UBM	Under Bump Metal
UDP	User Datagram Protocol
UNII	Unlicensed National Information Infrastructure
VCO	Voltage Controlled Oscillator
VIF	Voice Interface
VHT	Very High Throughput
WAP	Wireless Application Protocol

Table 39. Acronyms and abbreviations...*continued*

Acronym	Definition
WAVE	Wireless Access in Vehicular Environments
WCI-2	Wireless Coexistence Interface 2
WEP	Wired Equivalent Privacy
WI	Wired Interface
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless Local Area Network
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPA2	Wi-Fi Protected Access 2
WPA2-PSK	Wi-Fi Protected Access 2-Pre-Shared Key
WPA-PSK	Wi-Fi Protect Access-Pre-Shared Key
XFQFN	Extra-Fine Quad Flat Non-leaded
XOSC	Crystal Oscillator

11 Revision history

Table 40. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
88W8801_SDS v.2.0	20201214	Product short data sheet	202007006F01	88W8801 v.1.0
Modifications	• Changed **88W8801** document ID to **88W8801_SDS**. • Figure 17 "Package marking and pin 1 location": updated. • Section 2 "Ordering information": moved to the beginning of the document (no other changes).			
88W8801 v.1.0	20200713	Product short data sheet	-	-

12 Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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