General Description

The IDT8T49N366I is a triple PLL with FemtoClock® NG technology. The IDT8T49N366I integrates low phase noise Frequency Translation / Synthesis and Jitter attenuation. It includes alarm and monitoring functions suitable for networking and communications applications. The device has three fully independent PLLs. Each PLL is able to generate any output frequency in the 0.98MHz - 312.5MHz range and most output frequencies in the 312.5MHz - 1,300MHz range (see Table 3 for details). A wide range of input reference clocks may be used as the source for the output frequency.

Each PLL of IDT8T49N366I has three operating modes to support a very broad spectrum of applications:

1) Frequency Synthesizer
   - Synthesizes output frequencies from an external reference clock REFCLK.
   - Fractional feedback division is used, so there are no requirements for any specific input reference clock frequency to produce the desired output frequency with a high degree of accuracy.
2) High-Bandwidth Frequency Translator
   - Applications: PCI Express, Computing, General Purpose
   - Translates any input clock in the 16MHz - 710MHz frequency range into any supported output frequency.
   - This mode has a high PLL loop bandwidth in order to track input reference changes, such as Spread-Spectrum Clock modulation.
3) Low-Bandwidth Frequency Translator
   - Applications: Networking & Communications.
   - Translates any input clock in the 8kHz -710MHz frequency range into any supported output frequency.
   - This mode supports PLL loop bandwidths in the 10Hz - 580Hz range and makes use of an external REFCLK to provide significant jitter attenuation.

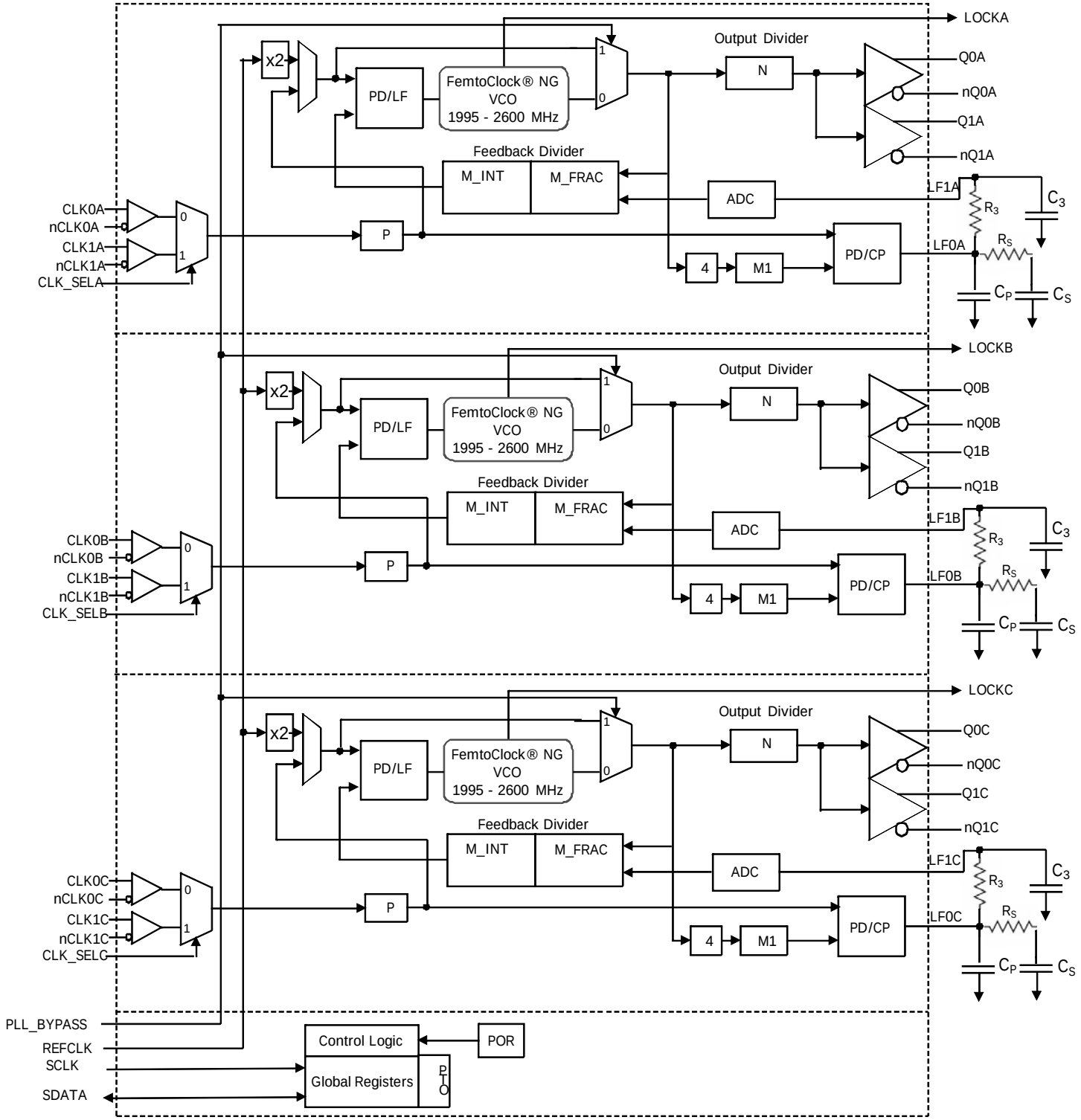
Each PLL provides factory-programmed default power-up configuration burned into One-Time Programmable (OTP) memory. The configuration is specified by customer and are programmed by IDT during the final test phase from an on-hand stock of blank devices.

To implement other configurations, these power-up default settings can be overwritten after power-up using the I^2C interface and the device can be completely reconfigured.

Features

- Fourth generation FemtoClock® NG technology
- Three fully independent PLLs
- Universal Frequency Translator™/Frequency Synthesizer and Jitter attenuator
- Outputs are programmable as LVPECL or LVDS
  - Programmable output frequency: 0.98MHz up to 1,300MHz
- Two differential inputs per PLL support the following input types: LVPECL, LVDS, LVHSTL, HCSL
- Input frequency range: 8kHz - 710MHz (Low-Bandwidth mode)
- Input frequency range: 16MHz - 710MHz (High-Bandwidth mode)
- REFCLK frequency range: 16MHz - 40MHz
- Input clock monitor on each PLL will smoothly switch between redundant input references
- Factory-set register configuration for power-up default state
  - Power-up default configuration
  - Configuration customized via One-Time Programmable ROM
  - Settings may be overwritten after power-up via I^2C
  - I^2C Serial interface for register programming
- RMS phase jitter at 161.1328125MHz, using 40MHz REFCLK (12kHz - 20MHz): 465fs (typical), Low Bandwidth Mode (FracN)
- RMS phase jitter at 400MHz, using 40MHz REFCLK (12kHz - 20MHz): 333fs (typical), Synthesizer Mode (Integer FB)
- Full 2.5V ±5% supply mode
- -40°C to 85°C ambient operating temperature
- 10mm x 10mm CABGA package
- Lead-free (RoHS 6) packaging

Complete Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
E5	REFCLK	Input	Pulldown	Reference clock for device operation.
B7, C7	CLK0A, CLK1A	Input	Pulldown	Non-inverting differential clock inputs.
B6, C6	nCLK0A, nCLK1A	Input	Pullup/ Pulldown	Inverting differential clock inputs. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors).
G8, G7	CLK0B, CLK1B	Input	Pulldown	Non-inverting differential clock inputs.
F8, F7	nCLK0B, nCLK1B	Input	Pullup/ Pulldown	Inverting differential clock inputs. $V_{CC}/2$ default when left floating (set by the internal pullup and pulldown resistors).
H3, G3	CLK0C, CLK1C	Input	Pulldown	Non-inverting differential clock inputs.
H4, G4	nCLK0C, nCLK1C	Input	Pullup/ Pulldown	Inverting differential clock inputs. $V_{CC}2$ default when left floating (set by the internal pullup and pulldown resistors).
C8	Rsvd	Input		Reserved, connect to $V_{EE.}$
H7	Rsvd	Input		Reserved, connect to $V_{EE.}$
G2	Rsvd	Input		Reserved, connect to $V_{EE.}$
D6	CLK_SELA	Input	Pulldown	Input clock select. Selects the active differential clock input. 0 = CLK0A, nCLK0A (default) 1 = CLK1A, nCLK1A
F6	CLK_SELB	Input	Pulldown	Input clock select. Selects the active differential clock input. 0 = CLK0B, nCLK0B (default) 1 = CLK1B, nCLK1B
F4	CLK_SELC	Input	Pulldown	Input clock select. Selects the active differential clock input. 0 = CLK0C, nCLK0C (default) 1 = CLK1C, nCLK1C
E6	PLL_BYPASS	Input	Pulldown	Bypasses the DCXO PLL. 0 = PLL Mode (default) 1 = PLL Bypassed
G5	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.
D9, E9,	LF0A, LF1A	Analog I/O		Loop filter connection node pins. LF0A is the output, LF1A is the input.
J6, J5	LF0B, LF1B	Analog I/O		Loop filter connection node pins. LF0B is the output, LF1B is the input.
F1, E1	LF0C, LF1C	Analog I/O		Loop filter connection node pins. LF0C is the output, LF1C is the input.
G6	SDATA	I/O	Pullup	I^2C Data Input/Output. Open drain.
A9, B9	Q0A, nQ0A	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
D8, F9	Q1A, nQ1A	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
J9, J8	Q0B, nQ0B	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
H6, J4	Q1B, nQ1B	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
J1, H1	Q0C, nQ0C	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
F2, D1	Q1C, nQ1C	Output		Differential output pair. Output type is programmable to LVDS or LVPECL interface levels.
C5	LOCKA	Output		Lock Indicator - indicates that PLLA is in a locked condition. LVCMOS/LVTTL interface levels.

Table 1. Pin Descriptions

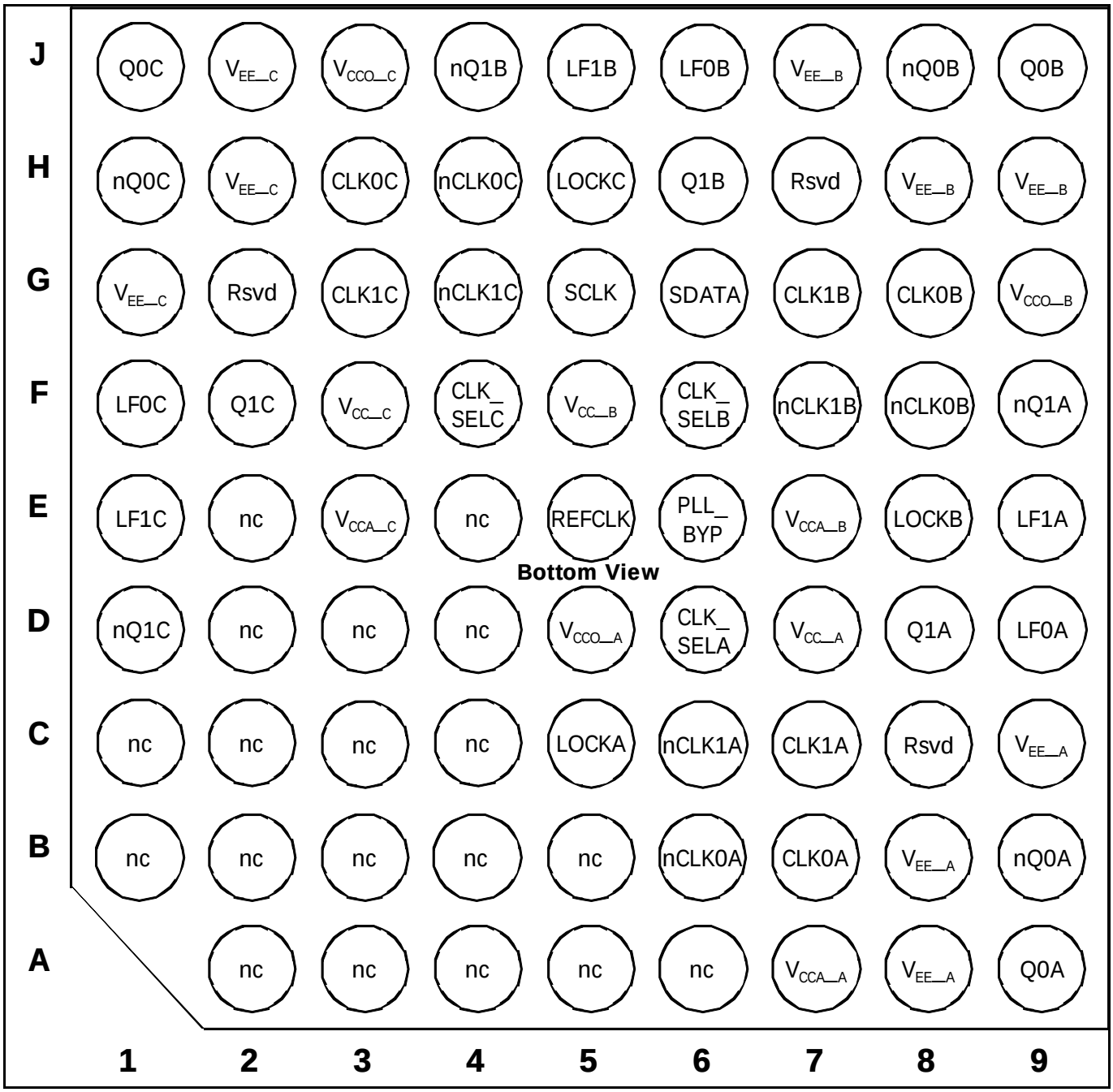
Number	Name	Type		Description
E8	LOCKB	Output		Lock Indicator - indicates that PLLB is in a locked condition. LVCMOS/LVTTL interface levels.
H5	LOCKC	Output		Lock Indicator - indicates that PLLC is in a locked condition. LVCMOS/LVTTL interface levels.
A7	V_{CCA_A}	Power		Analog power supply for PLLA.
D5	V_{CCO_A}	Power		Output power supply for PLLA.
D7	V_{CC_A}	Power		Core power supply for PLLA.
E7	V_{CCA_B}	Power		Analog power supply for PLLB.
G9	V_{CCO_B}	Power		Output power supply for PLLB.
F5	V_{CC_B}	Power		Core power supply for PLLB.
E3	V_{CCA_C}	Power		Analog power supply for PLLC.
J3	V_{CCO_C}	Power		Output power supply for PLLC.
F3	V_{CC_C}	Power		Core power supply for PLLC.
A8, B8, C9	V_{EE_A}	Power		Negative supply for PLLA.
H8, H9, J7	V_{EE_B}	Power		Negative supply for PLLB.
G1, H2, J2	V_{EE_C}	Power		Negative supply for PLLC.
A2-A6, B1-B5, C1-C4, D2-D4, E2, E4	nc			No connect. These pins may be left unconnected.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				3.5		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	REFCLK, PLL_BYPASS			16.66		kΩ
R_{PULLUP}	Input Pullup Resistor	SDATA, SCLK			16.66		kΩ

Pin Assignment



IDT8T49N366I Pin Map

80-Ball Lead
10mm x 10mm x1mm package body
CABGA Package
(bottom view)

Functional Description

The IDT8T49N366I is a three PLL device. The three PLLs are fully independent and identical. Each PLL can generate desired outputs frequency (0.98MHz - 1300MHz) from any input source in the operating range (8kHz - 710MHz). It is capable of synthesizing frequencies from REFCLK source. The output frequency is generated regardless of the relationship to the input frequency. Each PLL of IDT8T49N366I can translate the desired output frequency from input clock. In this frequency translation mode, a low-bandwidth, jitter attenuation option is available that makes use of an external fixed-frequency REFCLK to translate from a noisy input source. If the input clock is known to be fairly clean or if some modulation on the input needs to be tracked, then the high-bandwidth frequency translation mode can be used, without the need for the external clock source.

The input clock references and REFCLK input are monitored continuously and appropriate alarm outputs are raised by register bits and hard-wired pins in the event of any out-of-specification conditions arising. Clock switching is supported in manual, revertive & non-revertive modes.

Each PLL of IDT8T49N366I has a factory-programmed configuration as the default operating state after reset. These defaults may be over-written by I^2C register access at any time, but those over-written settings will be lost on power-down. Please contact IDT if a specific set of power-up default settings is desired.

The following sections apply individually to each PLL. Signal and register bit names have a lowercase ‘x’ on the end where ‘x’ should be ‘A’, ‘B’ or ‘C’ as appropriate for the PLL being controlled.

Operating Modes

Each PLL of IDT8T49N366I has three operating modes which are set by the MODE_SEL[1:0] bits. There are two frequency translator modes - low bandwidth and high bandwidth and a frequency synthesizer mode.

Please make use of IDT-provided configuration applications to determine the best operating settings for the desired configuration of the device.

Output Dividers & Supported Output Frequencies

The internal VCO is capable of operating in a range anywhere from 1.995GHz - 2.6GHz. It is necessary to choose an integer multiplier of the desired output frequency that results in a VCO operating frequency within that range. The output divider stage N[10:0] is limited to selection of integers from 2 to 2046. Please refer to Table 3 for the values of N applicable to the desired output frequency.

Table 3. Output Divider Settings & Frequency Ranges

Register Setting	Frequency Divider	Minimum f_{OUT}	Maximum f_{OUT}
Nn[10:0]	N	(MHz)	(MHz)
0000000000x	2	997.5	1300
00000000010	2	997.5	1300
00000000011	3	665	866.7
00000000100	4	498.75	650
00000000101	5	399	520
0000000011x	6	332.5	433.3
0000000100x	8	249.4	325
0000000101x	10	199.5	260
0000000110x	12	166.3	216.7
0000000111x	14	142.5	185.7
0000001000x	16	124.7	162.5
0000001001x	18	110.8	144.4
...	Even N	1995 / N	2600 / N
1111111111x	2046	0.98	1.27

Frequency Synthesizer Mode

This mode of operation allows an arbitrary output frequency to be generated from external REFCLK input. For improved phase noise performance, the REFCLK input frequency is doubled. As can be seen from the block diagram in *Figure 1,* only the upper feedback loop is used in this mode of operation. It is recommended that CLK0 and CLK1 be left unused in this mode of operation.

The upper feedback loop supports a delta-sigma fractional feedback divider. This allows the VCO operating frequency to be a non-integer multiple of the REFCLK frequency. By using an integer multiple only, lower phase noise jitter on the output can be achieved, however the use of the delta-sigma divider logic will provide excellent performance on the output if a fractional divisor is used.

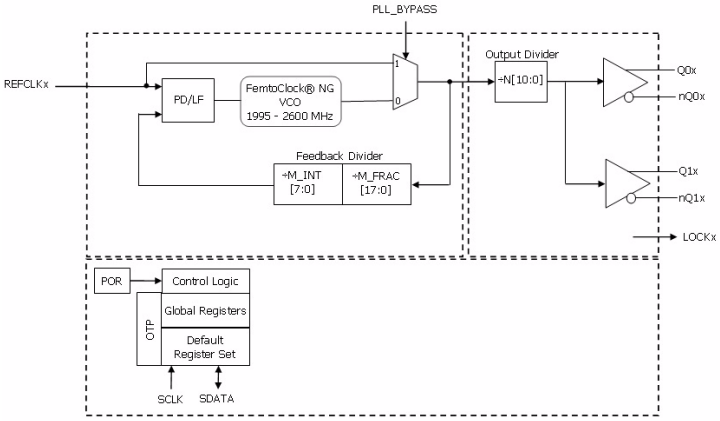


Figure 1. Frequency Synthesizer Mode Block Diagram

High-Bandwidth Frequency Translator Mode

This mode of operation is used to translate one of two input clocks of the same nominal frequency into an output frequency. As can be seen from the block diagram in Figure 2, similarly to the Frequency Synthesizer mode, only the upper feedback loop is used.

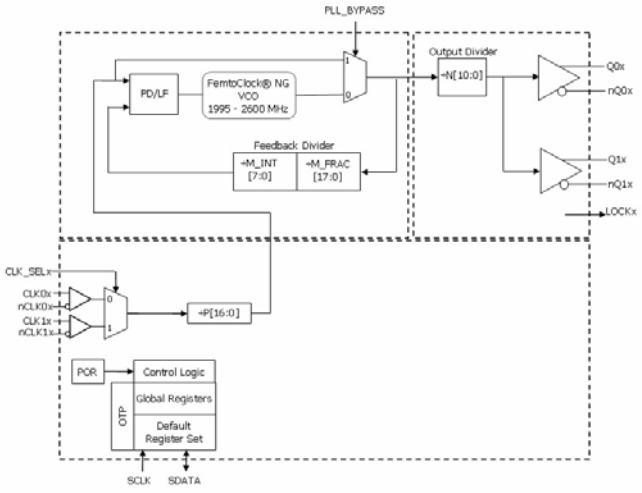


Figure 2. High Bandwidth Frequency Translator Mode Block Diagram

The input reference frequency range is now extended up to 710MHz. A pre-divider stage P is needed to keep the operating frequencies at the phase detector within limits.

Low-Bandwidth Frequency Translator Mode

As can be seen from the block diagram in Figure 3, this mode involves two PLL loops. The lower loop with the large integer dividers is the low bandwidth loop and it sets the output-to-input frequency translation ratio.This loop drives the upper DCXO loop (digitally controlled crystal oscillator) via an analog-digital converter.

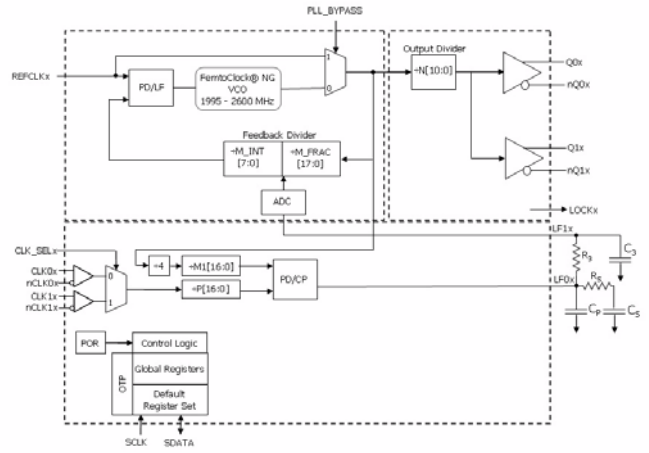


Figure 3. Low Bandwidth Frequency Translator Mode Block Diagram

The phase detector of the lower loop is designed to work with frequencies in the 8kHz - 16kHz range. The pre-divider stage is used to scale down the input frequency by an integer value to achieve a frequency in this range. By dividing down the fed-back VCO operating frequency by the integer divider M1[18:0] to as close as possible to the same frequency, exact output frequency translations can be achieved.

Alarm Conditions & Status Bits

Each PLL of IDT8T49N366I monitors a number of conditions and reports their status via both output pins and/or register bits. All alarms will behave as indicated below in all modes of operation, but some of the conditions monitored have no valid meaning in some operating modes. For example, the status of CLK0BADx, CLK1BADx and CLK_ACTIVEx are not relevant in Frequency Synthesizer mode. The outputs will still be active and it is left to the user to determine which to monitor and how to respond to them based on the known operating mode.

CLK_ACTIVEx - indicates which input clock reference is being used to derive the output frequency.

LOCKx - This status is asserted on the pin & register bit when the PLL is locked to the appropriate input reference for the chosen mode of operation. The status bit will not assert until frequency lock has been achieved, but will de-assert once lock is lost.

REFBAD - indicates if valid edges are being received on the REFCLK input. Detection is performed by comparing the input to the feedback signal at the upper loop's Phase / Frequency Detector (PFD). If three edges are received on the feedback without an edge on the REFCLK input, the REFBAD alarm is asserted in register bit. Once an edge is detected on the REFCLK input, the alarm is immediately deasserted.

CLK0BADx - indicates if valid edges are being received on the CLK0 reference input. Detection is performed by comparing the input to the feedback signal at the appropriate Phase / Frequency Detector (PFD). When operating in high-bandwidth mode, the feedback at the upper PFD is used. In low-bandwidth mode, the feedback at the lower PFD is used. If three edges are received on the feedback without an edge on the divided down (÷P) CLK0x reference input, the CLK0BADx alarm is asserted on register bit. Once an edge is detected on the CLK0x reference input, the alarm is deasserted.

CLK1BADx - indicates if valid edges are being received on the CLK1x reference input. Behavior is as indicated for the CLK0BADx alarm, but with the CLK1x input being monitored and the CLK1BADx register bits being affected.

HOLDOVERx - indicates that the device is not locked to a valid input reference clock. This can occur in Manual switchover mode if the selected reference input has gone bad, even if the other reference input is still good. In automatic mode, this will only assert if both input references are bad.

Input Reference Selection and Switching

When operating in Frequency Synthesizer mode, the CLK0x and CLK1x inputs are not used and the contents of this section do not apply. Except as noted below, when operating in either High or Low Bandwidth Frequency Translator mode, the contents of this section apply equally when in either of those modes.

Both input references CLK0x and CLK1x must be the same nominal frequency. These may be driven by any type of clock source. A difference in frequency may cause the PLL to lose lock when switching between input references. Please contact IDT for the exact limits for your situation.

Each PLL has global control bits AUTO_MANx[1:0] to dictate the order of priority and switching mode to be used between the CLK0x and CLK1x inputs.

Manual Switching Mode

When the AUTO_MANx[1:0] field is set to Manual via Pin, then each PLL of IDT8T49N366I will use the CLK_SELx input pin to determine which input to use as a reference. Similarly, if set to Manual via Register, then the device will use the CLK_SELx register bit to determine the input reference. In either case, the PLL will lock to the selected reference if there is a valid clock present on that input.

If there is not a valid clock present on the selected input, each PLL of IDT8T49N366I will go into holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state. In either case, the HOLDOVERx alarm will be raised. This will occur even if there is a valid clock on the non-selected reference input. The device will recover from holdover / free-run state once a valid clock is re-established on the selected reference input.

Each PLL of IDT8T49N366I will only switch input references on command from the user. The user must either change the CLK_SELx register bit (if in Manual via Register) or CLK_SELx input pin (if in Manual via Pin).

Automatic Switching Mode

When the AUTO_MANx[1:0] field is set to either of the automatic selection modes (Revertive or Non-Revertive), each PLL of IDT8T49N366I determines which input reference it prefers / starts from by the state of the CLK_SELx register bit only. The CLK_SELx input pin is not used in either Automatic switching mode.

When starting from an unlocked condition, the device will lock to the input reference indicated by the CLK_SELx register bit. It will not pay attention to the non-selected input reference until a locked state has been achieved. This is necessary to prevent ‘hunting’ behavior during the locking phase.

Once the PLL of IDT8T49N366I has achieved a stable lock, it will remain locked to the preferred input reference as long as there is a valid clock on it. If at some point, that clock fails, then the device will automatically switch to the other input reference as long as there is a valid clock there. If there is not a valid clock on either input reference, each PLL of IDT8T49N366I will go into holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state. In either case, the HOLDOVERx alarm will be raised.

The PLL will recover from holdover / free-run state once a valid clock is re-established on either reference input. If clocks are valid on both input references, the device will choose the reference indicated by the CLK_SELx register bit.

If running from the non-preferred input reference and a valid clock returns, there is a difference in behavior between Revertive and Non-revertive modes. In Revertive mode, the device will switch back to the reference indicated by the CLK_SELx register bit even if there is still a valid clock on the non-preferred reference input. In Non-revertive mode, each PLL IDT8T49N366I will not switch back as long as the non-preferred input reference still has a valid clock on it.

Switchover Behavior of the PLL

Even though the two input references have the same nominal frequency, there may be minor differences in frequency and potentially large differences in phase between them. Each PLL of IDT8T49N366I will adjust its output to the new input reference. It will use Phase Slope Limiting to adjust the output phase at a fixed maximum rate until the output phase and frequency are now aligned to the new input reference. Phase will always be adjusted by extending the clock period of the output so that no unacceptably short clock periods are generated on the output.

Holdover / Free-run Behavior

When both input references have failed (Automatic mode) or the selected input has failed (Manual mode), each PLL of IDT8T49N366I will enter holdover (Low Bandwidth Frequency Translator mode) or free-run (High Bandwidth Frequency Translator mode) state if. In both cases, once the input reference is lost, the PLL will stop making adjustments to the output phase.

If operating in Low Bandwidth Frequency Translation mode, the PLL will continue to reference itself to the local reference and will hold its output phase and frequency in relation to that source. Output stability is determined by the stability of the local reference REFCLK in this case.

However, if operating in High Bandwidth Frequency Translation mode, the PLL no longer has any frequency reference to use and output stability is now determined by the stability of the internal VCO.

If the device is programmed to perform Manual switching, once the selected input reference recovers, the IDT8T49N366I will switch back to that input reference. If programmed for either Automatic mode, the device will switch back to whichever input reference has a valid clock first.

Output Configuration

The two outputs of each PLL both provide the same clock frequency.

The two outputs are individually selectable as LVDS or LVPECL output types via the Q0_TYPE and Q1_TYPE register bits. when the output is disabled, it will show a high impedance condition.

The two outputs can be enabled individually also via register control bit OE0x and OE1x respectively. When the differential output is in the disabled state, it will show a high impedance condition.

Serial Interface Configuration Description

The IDT8T49N366I has an I^2C-compatible configuration interface to access any of the internal registers (Table 4D) for frequency and PLL parameter programming. Each PLL acts as a slave device on the I^2C bus and has the address 0b11011xx, where xx is set to fixed value by A0 & A1 (see Table 4A for details). The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 4D) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see table 4B, 4C). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate I^2C the read or write transfer after accessing byte #23 of each PLL.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK.

Note: if a different device slave address is desired, please contact IDT.

Table 4A. I^2C Device Slave Address

	A6	A5	A4	A3	A2	A1	A0	R/W
PLLA	1	1	0	1	1	0	1	R/W
PLLB	1	1	0	1	1	1	0	R/W
PLLC	1	1	0	1	1	1	1	R/W

Table 4B. Block Write Operation

Bit	**1**	**2:8**	**9**	**10**	**11:18**	**19**	**20:27**	**28**	**29-36**	**37**	**...**	**...**	**...**
Description	START	Slave Address	W (0)	ACK	Address Byte (P)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 4C. Block Read Operation

Bit	**1**	**2:8**	**9**	**10**	**11:18**	**19**	**20**	**21:27**	**28**	**29**	**30:37**	**38**	**39-46**	**47**	**...**	**...**	**...**
Description	START	Slave Address	W (0)	ACK	Address Byte (P)	ACK	Repeated START	Slave Address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

Register Descriptions

Please consult IDT fro configuration software and/or guides to assist in selection of optimal register settings for the desired configurations. The below register map applies to each PLL. Register bit names have 'x' at the end of the name. This should be replaced by 'A', 'B' or 'C' as appropriate to the PLL being addressed at the time.

Table 4D. I²C Register Map

Reg	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	MFRACx[17]	MFRACx[16]	MFRACx[15]	MFRACx[14]	MFRACx[13]	MFRACx[12]	MFRACx[11]	MFRACx[10]
1	00001	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	00010	MFRACx[9]	MFRACx[8]	MFRACx[7]	MFRACx[6]	MFRACx[5]	MFRACx[4]	MFRACx[3]	MFRACx[2]
3	00011	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
4	00100	MFRACx[1]	MFRACx[0]	MINTx[7]	MINTx[6]	MINTx[5]	MINTx[4]	MINTx[3]	MINTx[2]
5	00101	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
6	00110	MINTx[1]	MINTx[0]	Px[16]	Px[15]	Px[14]	Px[13]	Px[12]	Px[11]
7	00111	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
8	01000	Px[10]	Px[9]	Px[8]	Px[7]	Px[6]	Px[5]	Px[4]	Px[3]
9	01001	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	01010	Px[2]	Px[1]	Px[0]	M1_x[16]	M1_x[15]	M1_x[14]	M1_x[13]	M1_x[12]
11	01011	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
12	01100	M1_x[11]	M1_x[10]	M1_x[9]	M1_x[8]	M1_x[7]	M1_x[6]	M1_x[5]	M1_x[4]
13	01101	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
14	01110	M1_x[3]	M1_x[2]	M1_x[1]	M1_x[0]	Nx[10]	Nx[9]	Nx[8]	Nx[7]
15	01111	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
16	10000	Nx[6]	Nx[5]	Nx[4]	Nx[3]	Nx[2]	Nx[1]	Nx[0]	BWx[6]
17	10001	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
18	10010	BWx[5]	BWx[4]	BWx[3]	BWx[2]	BWx[1]	BWx[0]	Q1_TYPEx	Q0_TYPEx
19	10011	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
20	10100	MODE_SELx[1]	MODE_SELx[0]	0	1	OE1x	OE0x	Rsvd	Rsvd
21	10101	CLK-SELx	AUTO_MANx[1]	AUTO_MANx[0]	HOLD_OFF	ADC_RATEx[1]	ADC_RATEx[0]	LCK_WINx[1]	LCK_WINx[0]
22	10110	1	0	1	0	DBL_REFCLKx	0	0	1
23	10111	CLK_ACTIVEx	HOLDOVERx	CLK1BADx	CLK0BADx	REFBADx	LOCKx	Rsvd	Rsvd

NOTE: "x" denotes A, B or C.

Table 4E. Configuration-Specific Control Bits

Register Bits	Function
Q0_TYPEx	Determines the output type for output pair Q0, nQ0 for PLLx 0 = LVPECL 1 = LVDS
Q1_TYPEx	Determines the output type for output pair Q1, nQ1 for PLLx. 0 = LVPECL 1 = LVDS
Px[16:0]	Reference Pre-Divider for PLLx.
M1_x[16:0]	Integer Feedback Divider in Lower Feedback Loop for PLLx.
M_INTx[7:0]	Feedback Divider, Integer Value in Upper Feedback Loop for PLLx.
M_FRACx[17:0]	Feedback Divider, Fractional Value in Upper Feedback Loop for PLLx.
Nx[10:0]	Output Divider for PLLx.
BWx[6:0]	Internal Operation Settings for PLLx. Please use IDT IDT8T49N366I Configuration Software to determine the correct settings for these bits for the specific configuration. Alternatively, please consult with IDT directly for further information on the functions of these bits.The function of these bits are explained in Tables 4J and 4K.

Table 4F. Global Control Bits

Register Bits	Function
MODE_SELx[1:0]	PLL Mode Select for PLLx 00 = Low Bandwidth Frequency Translator 01 = Frequency Synthesizer 10 = High Bandwidth Frequency Translator 11 = High Bandwidth Frequency Translator
OE0x	Output Enable Control for Output 0 for PLLx. 0 = Output Q0, nQ0 disabled 1 = Output Q0, nQ0 enabled
OE1x	Output Enable Control for Output 1 for PLLx. 0 = Output Q1, nQ1 disabled 1 = Output Q1, nQ1 enabled
Rsvd	Reserved bits - user should write a ‘0’ to these bit positions if a write to these registers is needed
AUTO_MANx[1:0]	Selects how input clock selection is performed for PLLx. 00 = Manual Selection via pin only 01= Automatic, non-revertive 10 = Automatic, revertive 11= Manual Selection via register only
CLK_SELx	In manual clock selection via register mode for PLLx, this bit will command which input clock is selected. In the automatic modes, this indicates the primary clock input. In manual selection via pin mode, this bit has no effect. 0 = CLK0 1 = CLK1
ADC_RATEx[1:0]	Sets the ADC sampling rate in Low-Bandwidth Mode as a fraction of the REFCLK input frequency for PLLx 00 = REFCLK Frequency / 16 when doubler is disabled 01 = REFCLK Frequency / 8 when doubler is disabled 10 = REFCLK Frequency / 4 (recommended) when doubler is disabled 11 = REFCLK Frequency / 2 when doubler is disabled
LCK_WINx[1:0]	Sets the width of the window in which a new reference edge must fall relative to the feedback edge for PLLx: 00 = 2usec (recommended), 01 = 4usec, 10 = 8usec, 11 = 16usec
DBL_REFCLKx	When set, this bit will double the frequency of the REFCLK input before applying it to the Phase-Frequency Detector for PLLx

Table 4G. Global Status Bits

Register Bits	Function
CLK0BADx	Status Bit for input clock 0 for PLLx. 0 = input 0 good 1 = input 0 bad. Self clears when input clock returns to good status
CLK1BADx	Status Bit for input clock 1 for PLLx. 0 = input 0 good 1 = input 0 bad. Self clears when input clock returns to good status
REFBADx	Status Bit for PLLx. 0= REFCLK input good 1 = REFCLK input bad. Self-clears when the REFCLK clock returns to good status
LOCKx	Status bit for PLLx. This bit is mirrored on LOCKx pin. 0 = PLL unlocked 1 = PLL locked
HOLDOVERx	Status Bit for PLLx. 0 = Input to phase detector is within specifications and device is tracking to it 1 = Phase detector input not within specifications and DCXO is frozen at last value
CLK_ACTIVEx	Status Bit for PLLx. Indicates which input clock is active. Automatically updates during fail-over switching.

Table 4H. BW[6:0] Bits

Mode	BWx[6]	BWx[5]	BWx[4]	BWx[3]	BWx[2]	BWx[1]	BWx[0]
Synthesizer Mode	PLL2_LF x[1]	PLL2_LF x[0]	DSM_ORDx	DSM_ENx	PLL2_CP x[1]	PLL2_CP x[0]	PLL2_LOW _ICPx
High-Bandwidth Mode	PLL2_LF x[1]	PLL2_LF x[0]	DSM_ORDx	DSM_ENx	PLL2_CP x[1]	PLL2_CP x[0]	PLL2_LOW _ICPx
Low-Bandwidth Mode	ADC_GAIN x[3]	ADC_GAIN x[2]	ADC_GAIN x[1]	ADC_GAIN x[0]	PLL1_CP x[1]	PLL1_CP x[0]	PLL2_LOW _ICPx

Table 4I. Functions of Fields in BW[6:0]

Register Bits	Function
PLL2_LFx[1:0]	Sets loop filter values for upper loop PLL in Frequency Synthesizer & High-Bandwidth modes for PLLx. Defaults to setting of 00 when in Low Bandwidth Mode. See Table 4L for settings.
DSM_ORDx	Sets Delta-Sigma Modulation to 2nd (0) or 3rd order (1) operation for PLLx.
DSM_ENx	Enables Delta-Sigma Modulator for PLLx: 0 = Disabled - feedback in integer mode only 1 = Enabled - feedback in fractional mode
PLL2_CPx[1:0]	Upper loop PLL charge pump current settings for PLLx: 00 = 173µA (defaults to this setting in Low Bandwidth Mode) 01 = 346µA 10 = 692µA 11 = reserved
PLL2_LOW_ICPx	Reduces Charge Pump current by 1/3 to reduce bandwidth variations resulting from higher feedback register settings or high VCO operating frequency (>2.4GHz) for PLLx.
ADC_GAINx[3:0]	Gain setting for ADC in Low Bandwidth Mode.
PLL1_CPx[1:0]	Lower loop PLL charge pump current settings (lower loop is only used in Low Bandwidth Mode) for PLLx: 00 = 800µA 01 = 400µA 10 = 200µA 11 = 100µA

Table 4J. Upper Loop (PLL2) Bandwidth Settings

Desired Bandwidth	PLL2_CP		PLL2_LOW_ICP	PLL2_LF					
Frequency Synthesizer Mode									
200kHz	00		1	00					
400kHz	01		1	01					
800kHz	10		1	10					
2MHz	10		1	11					
High Bandwidth Frequency Translator Mode									
200kHz	00		1	00					
400kHz	01		1	01					
800kHz	10		1	10					
4MHz	10		0	11					

NOTE: To achieve 4MHz bandwidth, reference to the phase detector should be 80MHz.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.6V
Inputs, V_I	-0.5V to V_{CC_X} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{CCO_X} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	12.4°C/W (0 mps)
Package Thermal Impedance, θ_{JC}	12.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. LVPECL Power Supply DC Characteristics, $V_{CC\_X} = V_{CCO\_X} = 2.5V±5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC_X}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA_X}	Analog Power Supply Voltage		V_{CC_X} – 0.26	2.5	V_{CC_X}	V
V_{CCO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				880	mA
I_{CCA}	Analog Power Supply Current				78	mA

NOTE: X denotes: A, B or C.

Table 5B. LVDS Power Supply DC Characteristics, $V_{CC\_X} = V_{CCO\_X} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC_X}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA_X}	Analog Power Supply Voltage		V_{CC_X} – 0.26	2.5	V_{CC_X}	V
V_{CCO_X}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				750	mA
I_{CCA}	Analog Power Supply Current				78	mA
I_{CCO}	Output Power Supply Current				128	mA

NOTE: X denotes: A, B or C.

Table 5C. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC_X} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC_X} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current; NOTE 1	PLL_BYPASS, REFCLK, CLK_SELx	V_{CC_X} = V_{IN} = 2.625V			150	µA
		SCLK, SDATA	V_{CC_X} = V_{IN} = 2.625V			5	µA
I_{IL}	Input Low Current; NOTE 1	PLL_BYPASS, REFCLK, CLK_SELx	V_{CC_X} = 2.625V, V_{IN} = 0V	-5			µA
		SCLK, SDATA	V_{CC_X} = 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	SDATA, LOCKx	V_{CCO_X} = 2.625V, I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage	SDATA, LOCKx	V_{CCO_X} = 2.625V, I_{OH} = 12mA			0.5	V

NOTE1: For PLL_BYPASS/REFCLK/SCLK/SDATA pins, specification is for each individual PLL and is guaranteed by design. Production Test is performed all PLLs combined.
NOTE: X denotes: A, B or C.

Table 5D. Differential DC Characteristics, V_{CC_X} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0[B:D], nCLK0[B:D], CLK1[B:D], nCLK1[B:D],	V_{CC_X} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK0[B:D], CLK1[B:D],	V_{CC_X} = 2.625V, V_{IN} = 0V	-5			µA
		nCLK0[B:D], nCLK1[B:D]	V_{CC_X} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE} + 0.5		V_{CC_X} – 1.0	V

NOTE: X denotes: A, B or C.
NOTE 1: Common mode input voltage is defined at the crosspoint.

Table 5E. LVPECL DC Characteristics, V_{CCO_X} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO_X} – 1.1		V_{CCO_X} – 0.7	V
V_{OL}	Output Low Voltage NOTE 1		V_{CCO_X} – 2.0		V_{CCO_X} – 1.5	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE: X denotes: A, B or C.
NOTE 1: Outputs terminated with 50Ω to V_{CCO_X} – 2V.

Table 5F. LVDS DC Characteristics, V_{CCO_X} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: X denotes: A, B or C.

Table 6. Input Frequency Characteristics, V_{CC_X} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	REFCLK; NOTE 1		16		40	MHz
		CLK0[A:C], nCLK0[A:C] CLK1[A:C], nCLK1[A:C]	High Bandwidth Mode	16		710	MHz
			Low Bandwidth Mode	0.008		710	MHz
		SCLK				5	MHz

NOTE: X denotes: A, B or C.
NOTE 1: For the input REFCLK and CLK0x, nCLK0x, CLK1x, nCLK1x frequency range, the Mx value must be set for the VCOx to operate within the 1995MHz to 2600MHz range.

AC Electrical Characteristics

Table 7. AC Characteristics, $V_{CC\_X} = V_{CCO\_X} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$*

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			0.98		1300	MHz
f_{VCO}	VCO Frequency			1995		2600	MHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random), Integer Divide Ratio; NOTE 1		Synth Mode (Integer FB), f_{OUT} = 400MHz, 40MHz REFCLK, Integration Range: 12kHz – 20MHz		333	435	fs
			Synth Mode (FracN FB), f_{OUT} = 698.81MHz, 40MHz REFCLK, Integration Range: 12kHz – 20MHz		408	665	fs
			HBW Mode, f_{IN} = 133.33MHz, f_{OUT} = 400MHz, Integration Range: 12kHz – 20MHz		338	490	fs
			LBW Mode (near integer), 40MHz REFCLK, f_{IN} = 19.44MHz, f_{OUT} = 622.08MHz, Integration Range: 12kHz – 20MHz		444	680	fs
			LBW Mode (FracN), 40MHz REFCLK, f_{IN} = 25MHz, f_{OUT} = 161.1328125MHz, Integration Range: 12kHz – 20MHz		465	680	fs
$t_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 2, 3		Frequency Synthesizer Mode			35	ps
			Frequency Translator Mode			40	ps
t_R / t_F	Output Rise/Fall Time; NOTE 3	LVPECL Outputs	20% to 80%	100		520	ps
		LVDS Outputs	20% to 80%	100		520	ps
odc	Output Duty Cycle; NOTE 3		f_{OUT} < 600MHz	45		55	%
			$f_{OUT} \geq$ 600MHz	40		60	%

NOTE: X denotes: A, B or C.

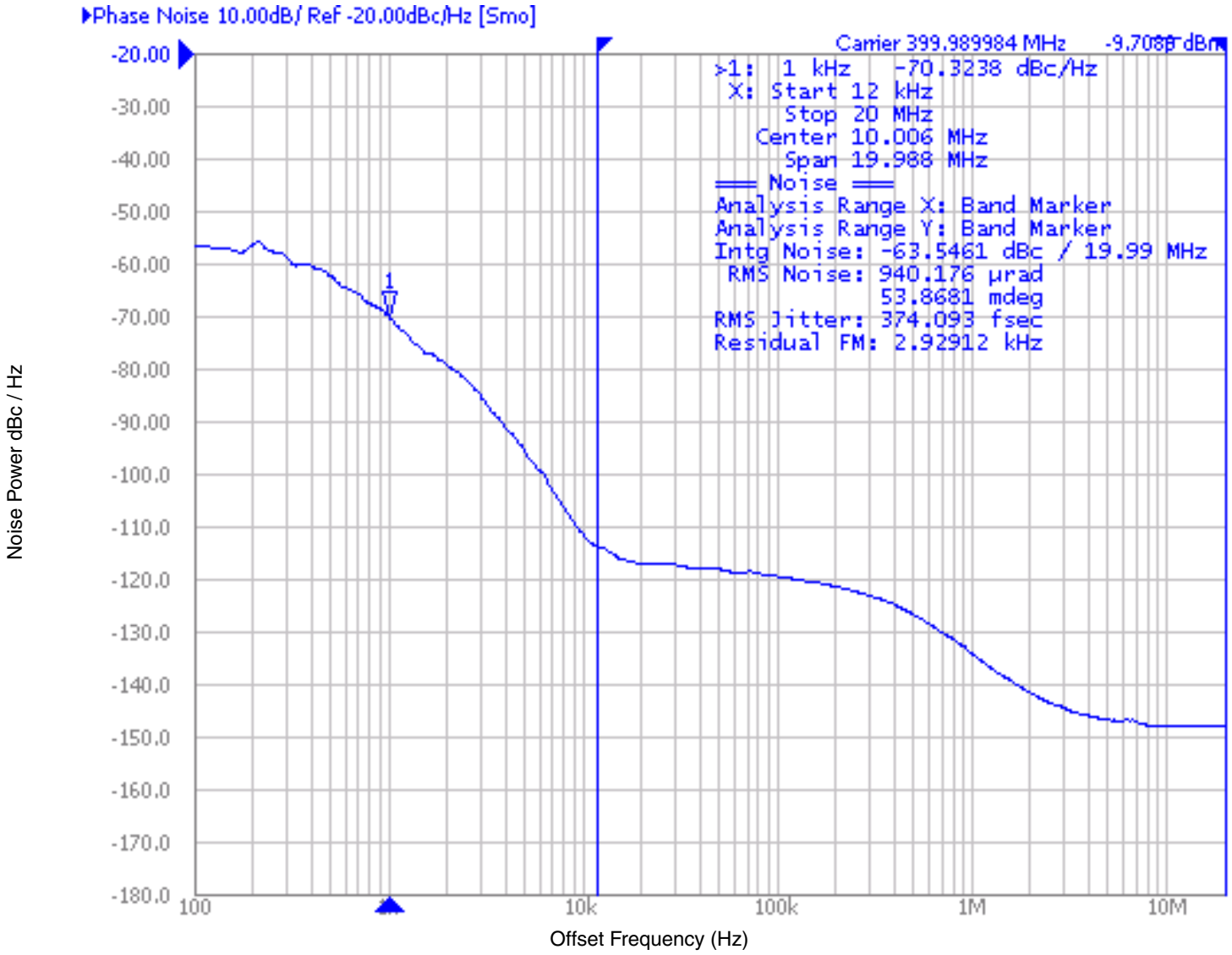
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: For RMS phase jitter measurement in Synth and HBW mode, all 4 PLLs are programmed with the same configuration. For the LBW mode, only the PLL under test is programmed with LBW configuration, the other PLLs are programmed with Synth mode with the same output frequency. A Rohde & Schwarz SMA-100 Signal generator, 9kHz to 6GHz, is used as the REFCLK source All configurations are with DBL_REFCLK bit set to 1.

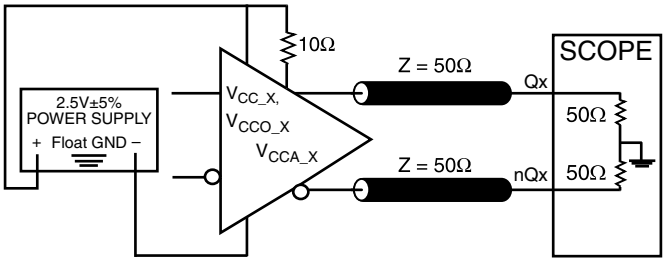
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Measurements are collected with the following output frequencies: 66.6667MHz, 125MHz, 156.25MHz, 161.138125MHZ, 400MHz, 622.08MHz, 698.81MHz, 1300MHz.

Typical Phase Noise at 400MHz (HBW Mode)

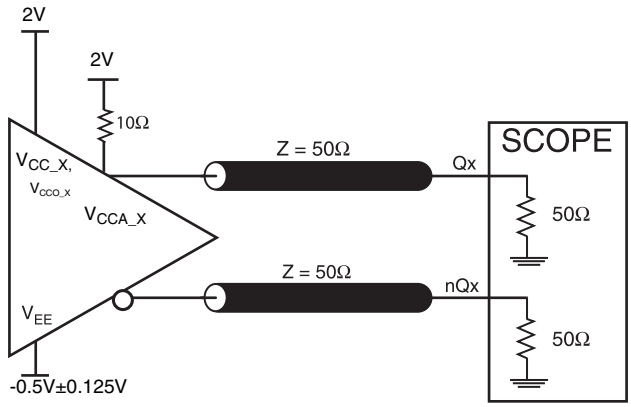


Parameter Measurement Information



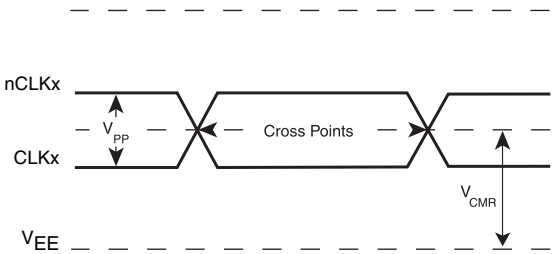
"X" denotes A, B, and C

2.5V Core/2.5V LVDS Output Load Test Circuit

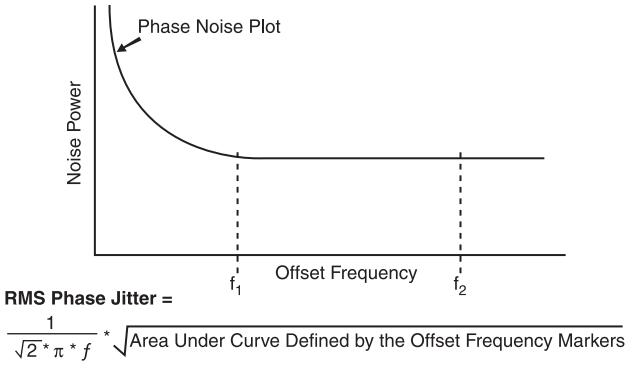


"X" denotes A, B, and C

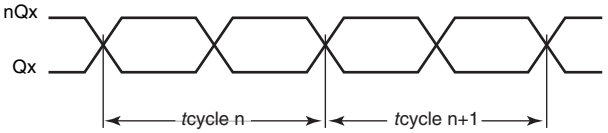
2.5V Core/2.5V LVPECL Output Load Test Circuit



Differential Input Levels

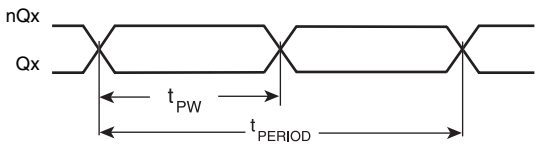


RMS Phase Jitter



$$tjit(cc) = |tcycle\ n - tcycle\ n+1|$$
1000 Cycles

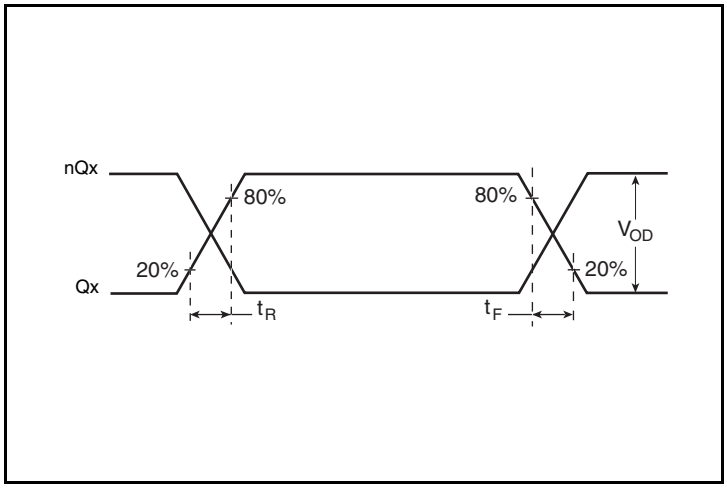
Cycle-to-Cycle Jitter



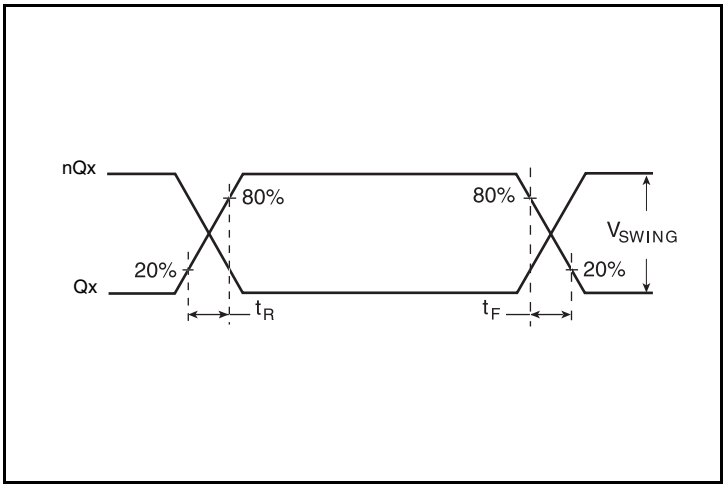
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Differential Output Duty Cycle/Output Pulse Width/Period

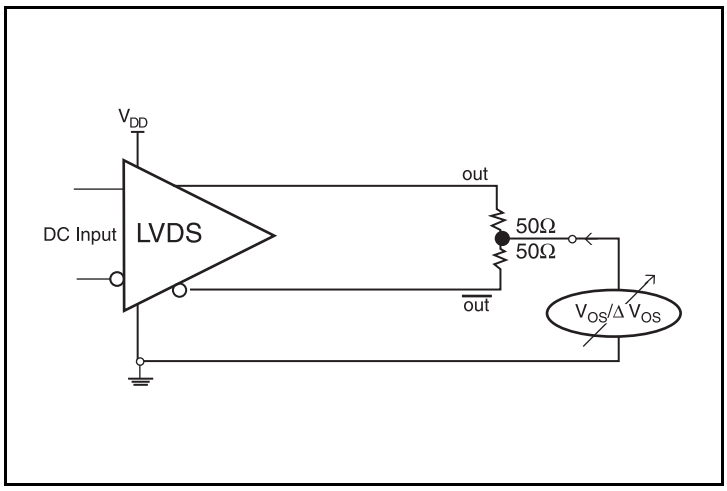
Parameter Measurement Information, continued



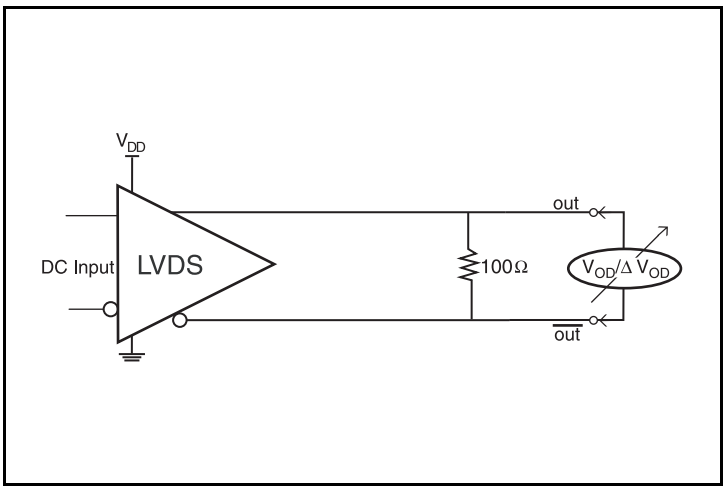
LVDS Output Rise/Fall Time



LVPECL Output Rise/Fall Time



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Inputs

For applications not requiring the use of either differential input, both CLKnx and nCLKnx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx be left unconnected in frequency synthesizer mode.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Recommended Values for Low-Bandwidth Mode Loop Filter

External loop filter components are not needed in Frequency Synthesizer or High-Bandwidth modes. In Low-Bandwidth mode, the loop filter structure and components are recommended, refer to the Application Schematic. Please consult IDT if other values are needed.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 4 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

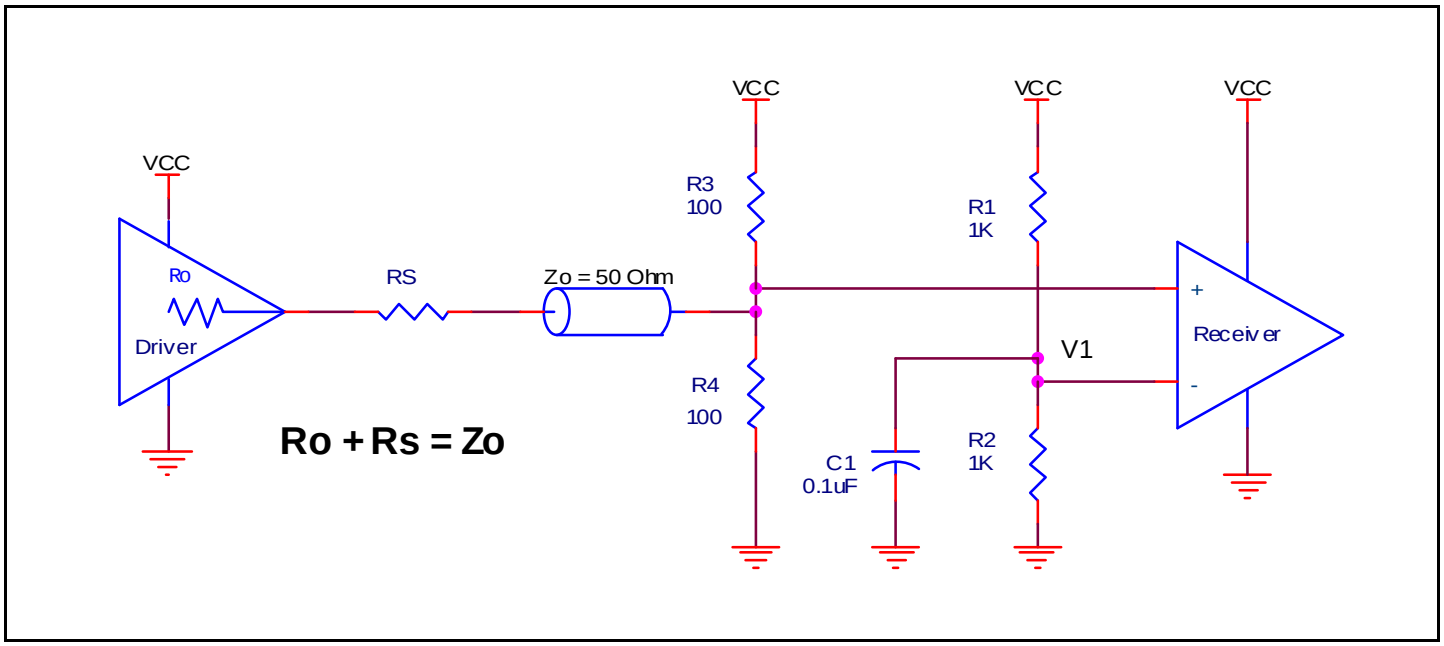


Figure 4. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLKx / nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the CLKx / nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 5A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

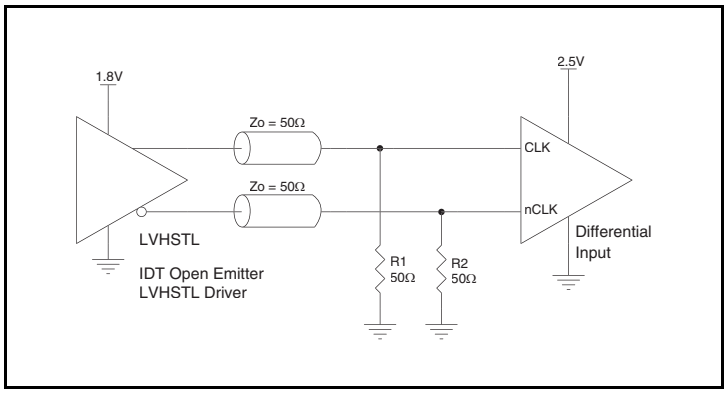


Figure 5A. CLKx/ nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

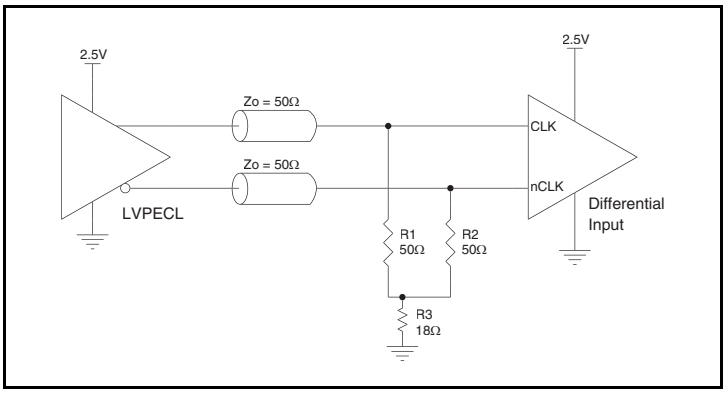


Figure 5B. CLKx/ nCLKx Input Driven by a 2.5V LVPECL Driver

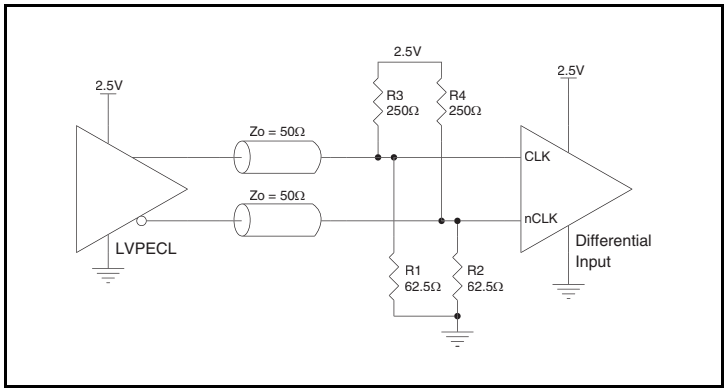


Figure 5C. CLKx/ nCLKx Input Driven by a 2.5V LVPECL Driver

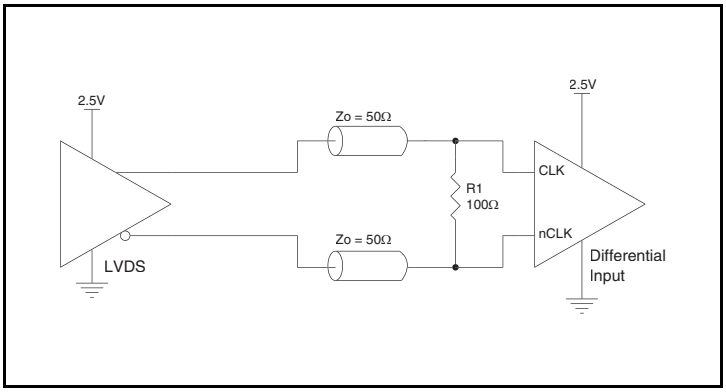


Figure 5D. CLKx/ nCLKx Input Driven by a 2.5V LVDS Driver

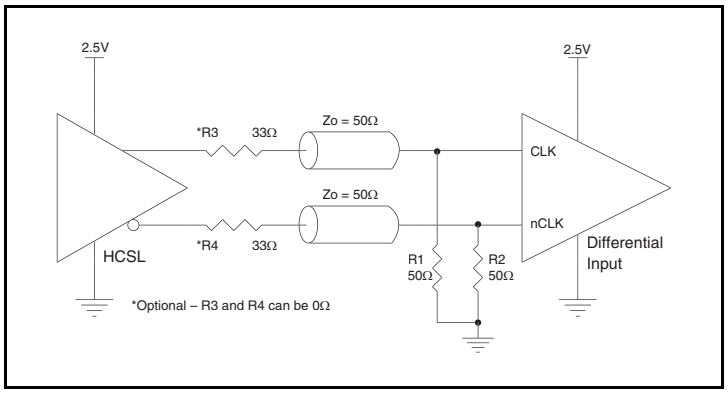


Figure 5E. CLKx/ nCLKx Input Driven by a 2.5V HCSL Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 6A* can be used with either type of output structure. *Figure 6B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

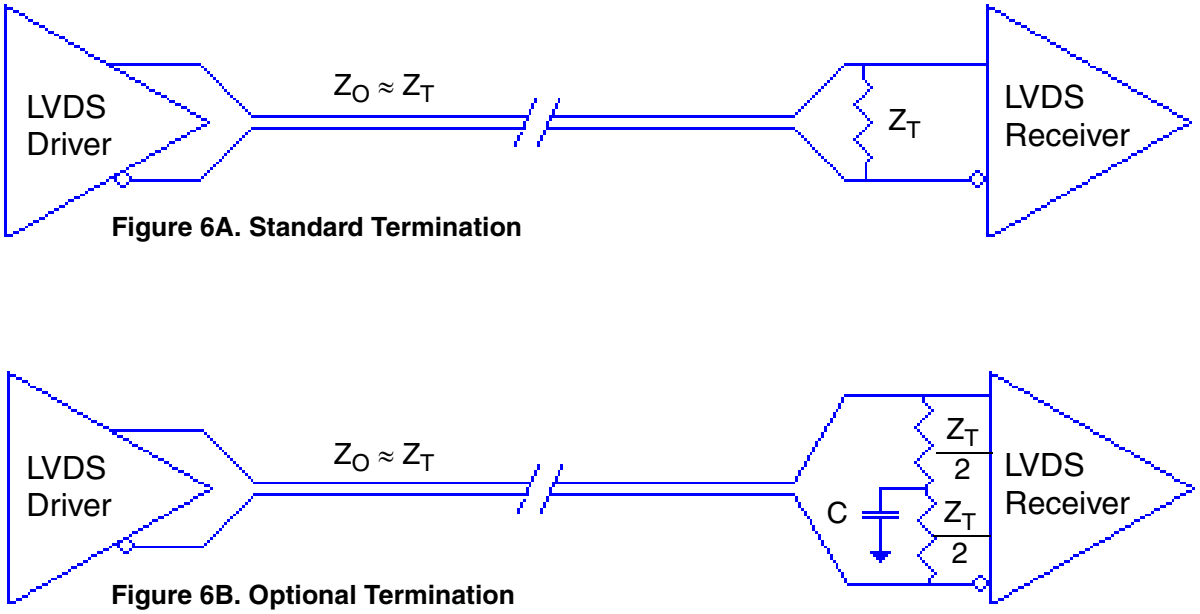


Figure 6A. Standard Termination

Figure 6B. Optional Termination

LVDS Termination

Termination for 2.5V LVPECL Outputs

Figure 7A and *Figure 7B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

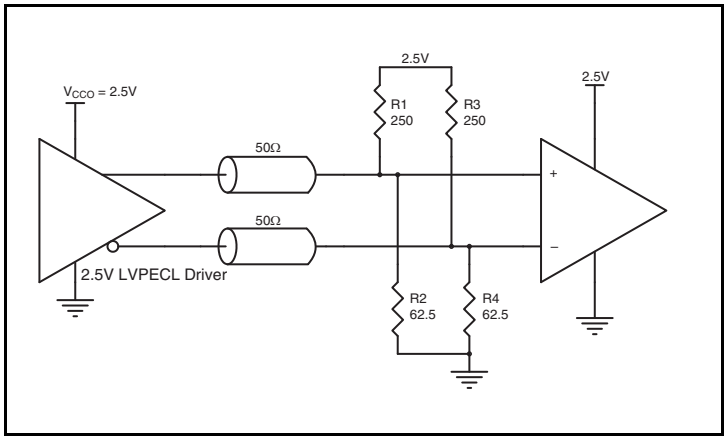


Figure 7A. 2.5V LVPECL Driver Termination Example

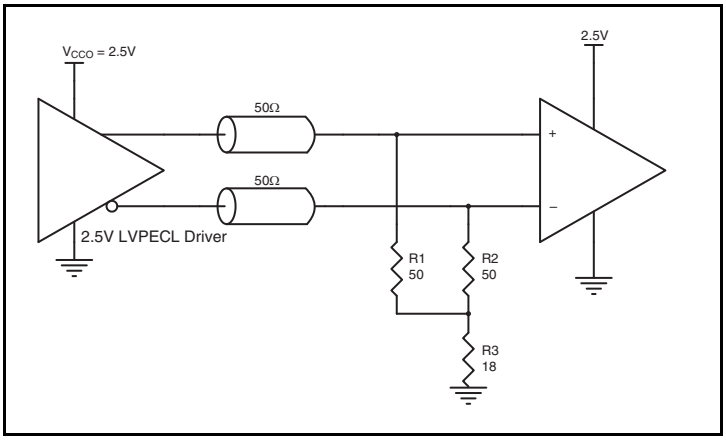


Figure 7B. 2.5V LVPECL Driver Termination Example

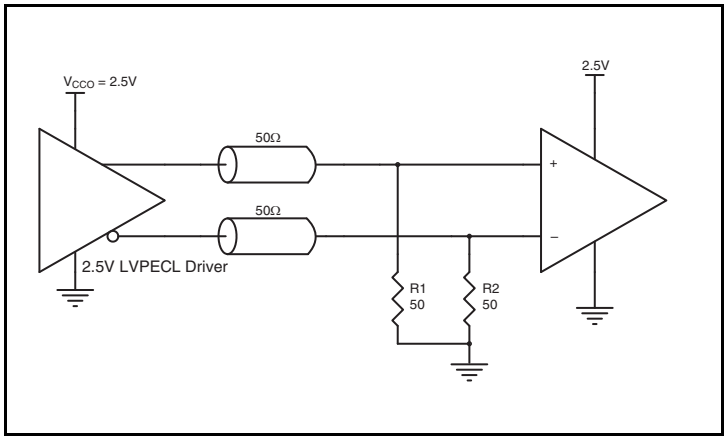


Figure 7C. 2.5V LVPECL Driver Termination Example

Schematic Layout

Figure 8 shows an example IDT8T49N366I application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that PLL_BYPASS and CLK_SEL_x pins are properly set. Input and output terminations shown are intended as examples only and may not match the exact user application. To promote readability in this schematic, only Jitter Attenuator B and the global pins PLL_BYPASS, REF_CLK and SDATA and SCLK are shown connected. Jitter Attenuators A and C are recommended to be connected similarly to Jitter Attenuator B; however different connections may be used as the four jitter attenuators are fully independent.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N366I provides separate V_{CC_X}, V_{CCA_X} and V_{CCO_X} power supplies for each jitter attenuator to isolate any high switching noise from coupling into the internal PLLs.

In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uf and 0.1uF capacitor connected to 2.5V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

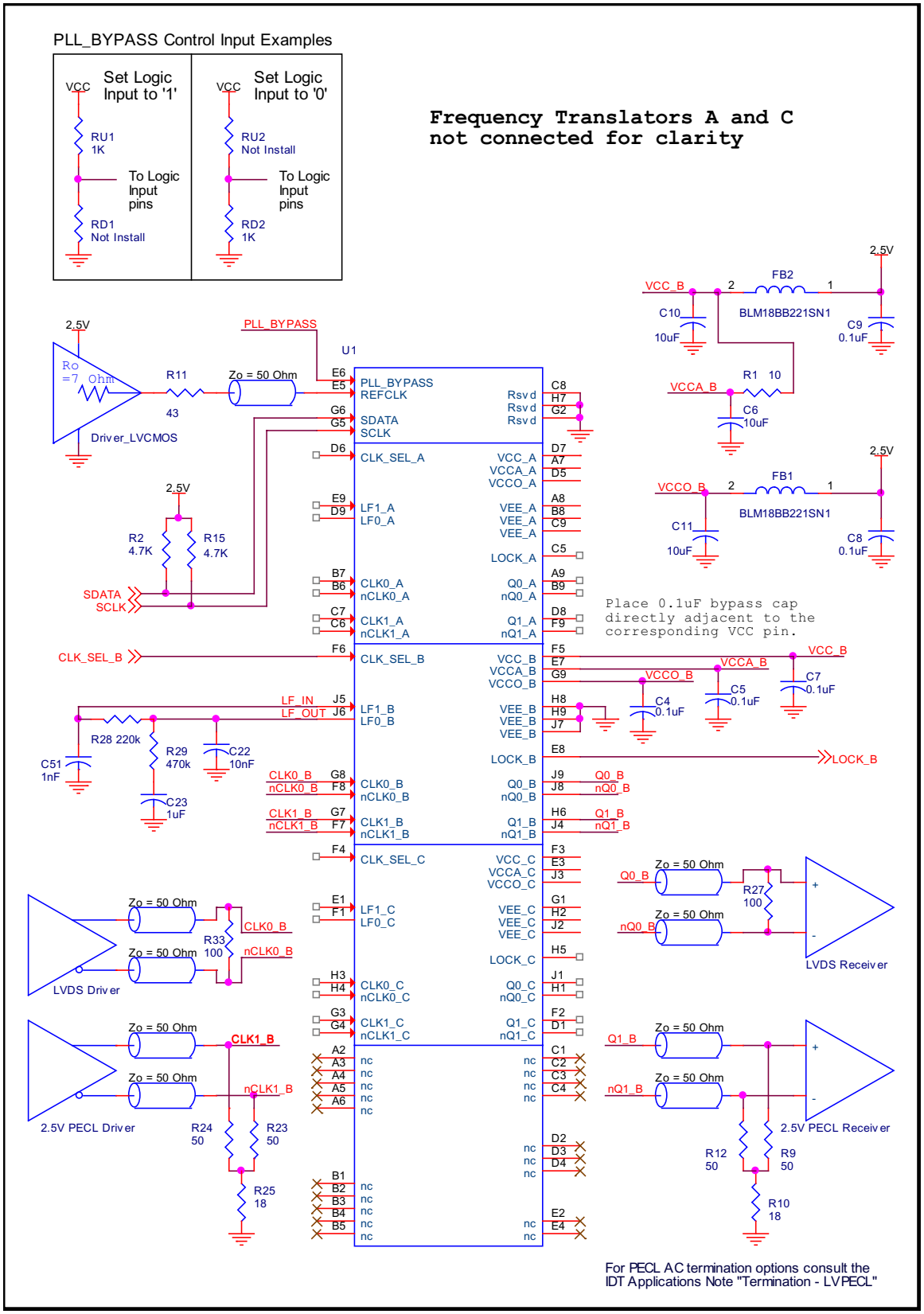


Figure 8. IDT8T49N366I Schematic Example

2.5V LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N366I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N366I is the sum of the core power plus the output power dissipated due to the load.
The following is the power dissipation for V_{CC} = 2.5V + 5% = 2.625V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 2.625V * 880mA = **2310W**
- Power (outputs)$_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 33.2mW = **199.2mW**

Total Power$_{\_MAX}$ (2.625V, with all outputs switching) = 2310mW + 199.2mW = **2509.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 12.4°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 2.509W * 12.4°C/W = 116.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. θ_{JA} vs. Air FlowTable for an 80-Ball CABGA

θ_{JA} vs. Air Flow				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE 1: θ_{JA} simulation is performed with 8-layers, 8in. x 8in. PCB for the 10x10, 1mm ball pitch BGA package.

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 9.*

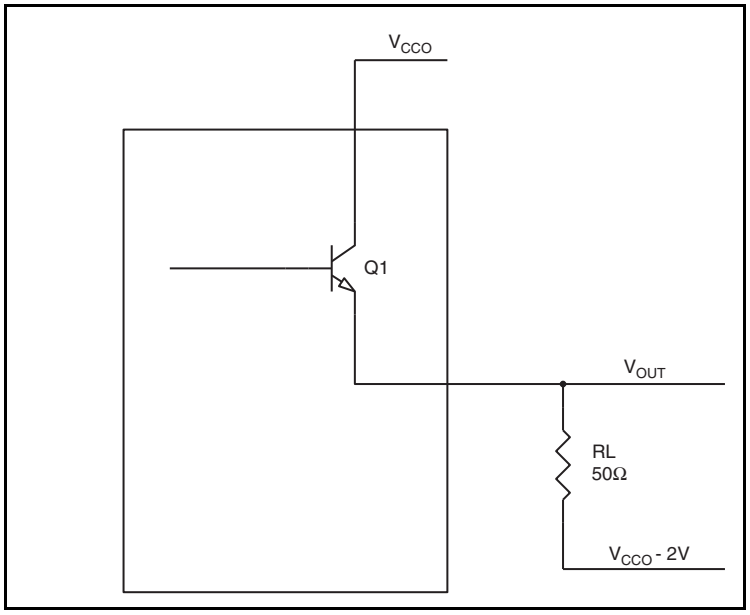


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.7V**
  ($V_{CCO\_MAX} – V_{OH\_MAX}$) = **0.7V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX} – 1.5V**
  ($V_{CCO\_MAX} – V_{OL\_MAX}$) = **1.5V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$ $[(2V – 0.7V)/50Ω] * 0.7V =$ **18.2mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CCO\_MAX} – V_{OL\_MAX}) =$ $[(2V – 1.5V)/50Ω] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N366I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N366I is the sum of the core power plus the analog power plus the output power dissipated due to loading. The following is the power dissipation for V_{CC} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power $(core)_{MAX} = V_{CC\_MAX} * (I_{CC\_MAXI} + I_{CCA\_MAX})$ = 2.625V * (750mA + 78mA) = **2173.5mW**
- Power $(outputs)_{MAX} = V_{CCO\_MAX} * I_{CCO\_MAX}$ = 2.625V * 128mA = **336mW**

Total Power$_{\_MAX}$ = 2173.5mW + 336mW = **2509.5mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 12.4°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 2.510W * 12.4°C/W = 116.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. θ_{JA} vs. Air FlowTable for an 80-Ball CABGA

θ_{JA} **vs. Air Flow**				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE 1: θ_{JA} simulation is performed with 8-layers, 8in. x 8in. PCB for the 10x10, 1mm ball pitch BGA package.

Reliability Information

Table 10. θ_{JA} vs. Air Flow Table for an 80-Ball CABGA

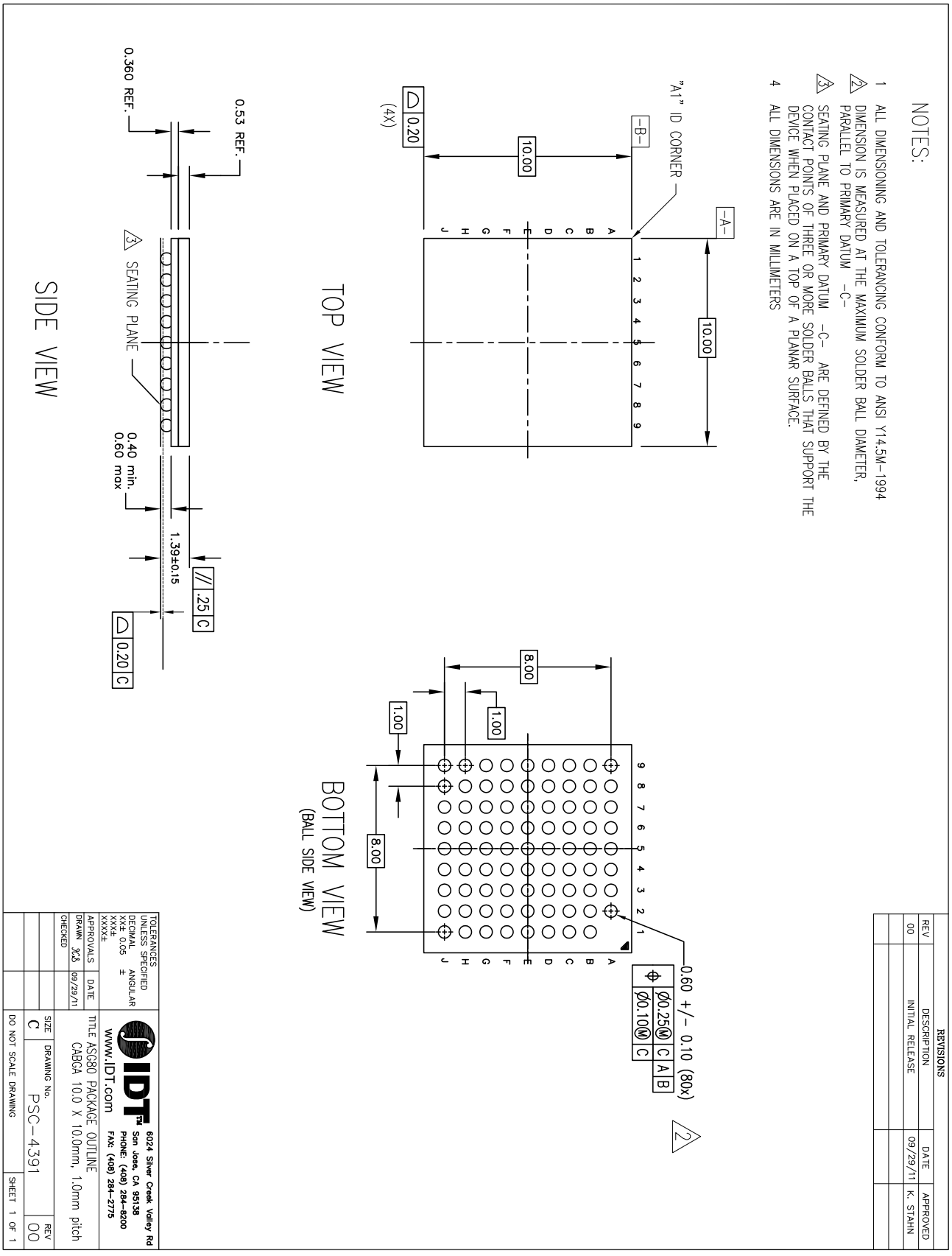
θ_{JA} vs. Air Flow				
Meters per Second	0	1	2	3
Multi-Layer PCB, NOTE 1	12.4°C/W	11°C/W	10.3°C/W	10°C/W

NOTE: The θ_{JA} simulation is performed with 8-layers, 8” x 8” PCB for the 10mm x 10mm, a 1mm ball pitch BGA package and a die size of 6mm x 6mm.

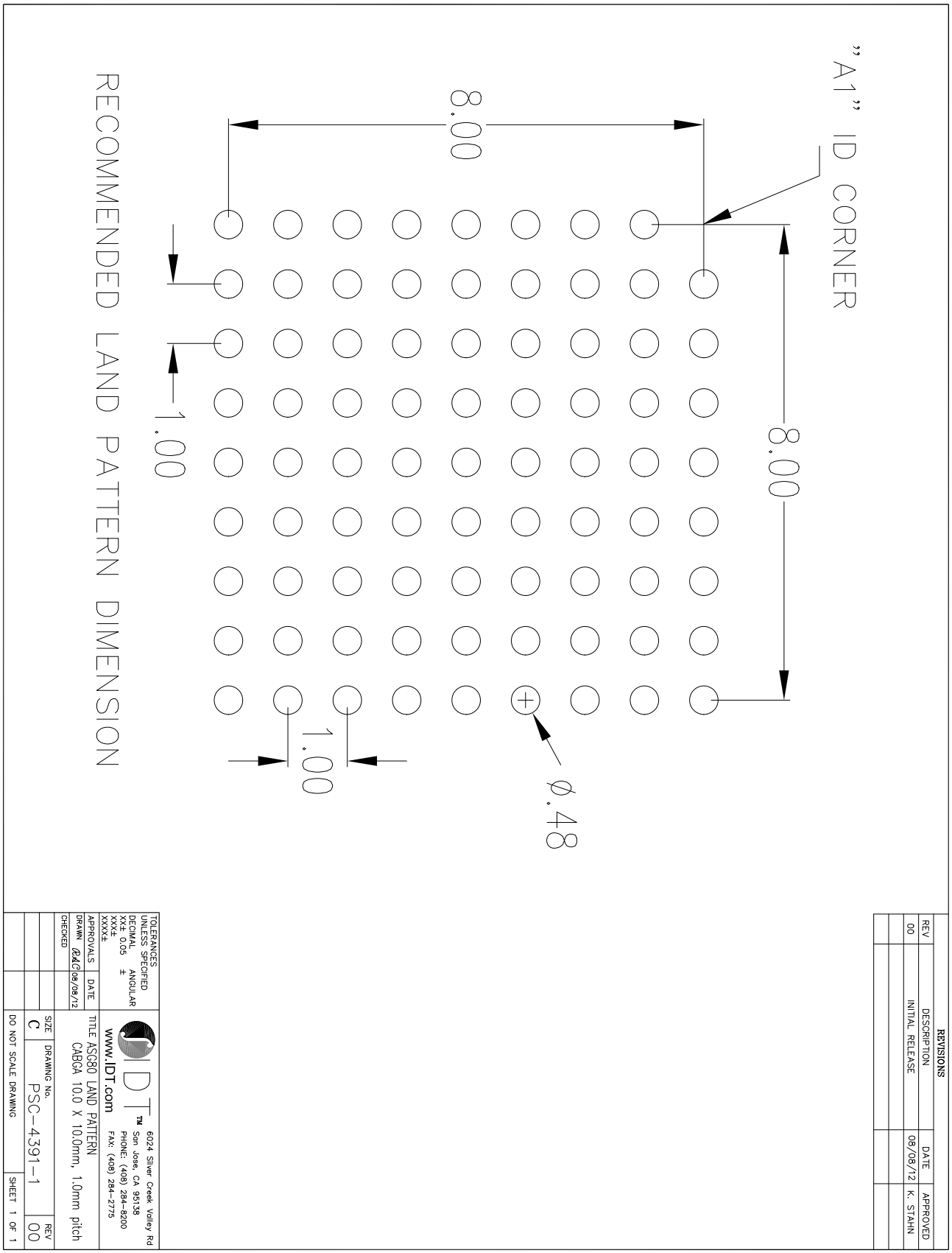
Transistor Count

The transistor count for IDT8T49N366I is: 151,929

80-Ball CABGA Package Outline and Package Dimensions



80-Ball CABGA Package Land Pattern



Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N366A-dddASGI	IDT8T49N366A-dddASGI	“Lead-Free” Plastic 80-Ball CABGA	Tray	-40°C to +85°C
8T49N366A-dddASGI8	IDT8T49N366A-dddASGI	“Lead-Free” Plastic 80-Ball CABGA	Tape & Reel	-40°C to +85°C

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T2 T5C	6 17	$R_{PULLDOWN}$, Input Pulldown Resistor, REFCLK: added PLL_BYPASS. I_{IH}, I_{IL}: added NOTE 1	2/8/2013
A	T4E	11	Corrected typo: M_INTx[8:0] to M_INTx[7:0]	6/28/13