

SINGLE CHIP PC AUDIO SYSTEM

CODEC+ STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

92HD87

Description

The 92HD87 single-chip audio system is a low power optimized, high fidelity, 4-channel audio codec with integrated speaker amplifier, capless headphone amplifier, and low drop out voltage regulator.

The high integration of the 92HD87 and the 40QFN package enables the smallest PCB footprint with the lowest system BOM count and cost.

The 92HD87 provides high quality HD Audio capability to notebook and business desktop PC applications.

Features

- **4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
 - Supports full-duplex stereo audio and simultaneous VoIP
- **2W/channel stereo speaker amplifier @ 4 ohms and 4.75V**
- **Two headphone amplifiers**
 - One capless and one non-capless retaskable
- **Internal LDO for digital core supply**
- **+5 V analog power supply option**
- **Dedicated BTL high pass filter for speaker protection (RA revision only)**
- **Full HDA015-B low power support**
 - Audio inactivity transitions codec from D0 to D3 low power mode
 - Resume from D3 to D0 with audio activity in < 10 msec
 - D3 to D0 transition with < -65dB pop/click
 - Port presence detect in D3 with or without bit clock
 - Optional analog PC beep in D3
 - Additional vendor specific modes for even lower power
- **Microsoft WLP premium logo compliant, as defined in WLP 3.9**
- **Support for 1.5V and 3.3V HDA signaling**
- **Digital microphone inputs (mono or stereo)**
- **Aux Audio Mode** (see orderable part numbers for support)
- **High performance analog mixer**
- **2 adjustable VREF Out pins for analog microphone bias**
- **5 analog ports with port presence detect + stereo speaker differential output)**
- **Analog and digital PC Beep support**
- **40-pad QFN RoHS package**

Software Support

- Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings
- 12 band fully parametric equalizer
 - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
 - System-level effects automatically disabled when external audio connections made
- Dynamics Processing
 - Enables improved voice articulation
 - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- IDT Vista APO wrapper
 - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
 - Improved multi-streaming user experience with less support calls
- Broad 3rd party branded software including Creative, Dolby, DTS, and SRS

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

1. DESCRIPTION

1.1. Overview

The 92HD87 is a high fidelity, 4-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD87 codec provides high quality, HD Audio capability to notebooks and business desktops.

The 92HD87 is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program as indicated in WLP 3.09.

The 92HD87 provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. The 92HD87 supports a wide range of notebook and business desktop 4-channel configurations.

An integrated BTL stereo amplifier is ideal for driving an integrated speaker in mobile, ultra-mobile, business or desktop computers.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD87 has 2 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and a better user experience. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD87 operates with a 1.5V, 1.8V or 3.3V digital supply and a 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling.

The 92HD87 is available in a 40-pin QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

| 4 channel, stereo BTL, 40QFN, Aux mode, 3.3V HDA signaling | |
|--|--|
| 92HD87B2X5NDGX RAX | HP CY12 specific models (Ando 1.X, Butternut 1.X, Miatta 2.X) |
| 92HD87B2X5NDGX RA1 | HP CY12 bNB and cNB models, MIC SW included |
| 92HD87B1X5NDGX RDX | HP CY11 models, drop-in replacement option of 92HD87B1X5NDGX TBX |

yy = silicon stepping/revision, contact sales for current data
Add an "8" to the end for tape and reel delivery. Min/Mult order quantity 2.5ku.

2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 3 or 4 bi-directional ports, 2 headphone ports, and a high power BTL amplifier support a wide variety of consumer desktop and mobile system use models.

For the codec the port capabilities are as follows

- Port A supports
 - Headphone
 - Line Out
 - Line Input
 - Mic with 0/10/20/30 dB Boost and Vref_Out
- Port B supports
 - Capless Headphone Out
 - Capless Line Out
- Port C supports
 - Line Out (not available on TB revision)
 - Line In
 - Mic with 0/10/20/30 dB boost and Vref_Out
- Port D supports
 - BTL (L+/L-) stereo out
- Port F supports
 - Line Out
 - Line In
 - Mic with 0/10/20/30 dB boost

| Pins | Port | Input | Output | Headphone | BTL | Mic Bias (Vref pin) | Input boost amp |
|-------|-------|-------|--------|-----------|-----|---------------------|-----------------|
| 24/23 | A | Yes | Yes | Yes | | Yes | Yes |
| 27/26 | B | | Yes | Yes | | | |
| 15/16 | C | Yes | Yes | | | Yes | Yes |
| 35/36 | D | | Yes | | Yes | | |
| 13/14 | F | Yes | Yes | | | | Yes |
| 3 | DMIC0 | Yes | | | | | Yes |

Table 1. Port Functionality

2.1.1. Port Characteristics

Universal (Bi-directional) jacks are supported on ports C (input only on TB revision) and F. Port A is bidirectional also. Ports A and B are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 50K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are 1V rms at 5V. Line output ports and Headphone output ports on the codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in power state D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use the codec, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

| AFG Power State | Input Enable | Output Enable | Port Behavior |
|-----------------|--------------|---------------|---|
| D0-D2 | 1 | 1 | Not allowed. Port is active as output. Input path is mute. |
| | 1 | 0 | Active - Port enabled as input |
| | 0 | 1 | Active - Port enabled as output |
| | 0 | 0 | Inactive -port is powered on (low output impedance) but drives silence only. |
| D3 | - | 0 | Inactive (lower power) - Port keeps output coupling caps charged if port uses caps. |
| | - | 1 | Low power state. If enabled, Beep will output from the port |
| D3cold | - | - | Inactive (lower power) - Port keeps output coupling caps charged if port uses caps. |
| D4 | - | - | Inactive (lower power) - Port keeps output coupling caps charged if port uses caps. |
| D5 | - | - | Off - Charge on coupling caps (if used) will not be maintained. |

Table 2. Analog Output Port Behavior

2.1.2. Vref_Out

Ports C & A support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

2.1.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C are detected using SENSE_A. Plugs inserted to a jack on Ports F, DMIC0, are detected using SENSE_B. Per HDA015-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per HDA015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages.

| AVdd Nominal Voltage (+/- 5%) | Resistor Tolerance Pull-Up | Resistor Tolerance SENSE_A/B |
|-------------------------------|----------------------------|------------------------------|
| 4.75V | 1% | 1% |

| Resistor | SENSE_A | SENSE_B |
|----------|-----------------|-----------------|
| 39.2K | PORT A (HP0) | NA |
| 20.0K | PORT B (HP1) | PORT F |
| 10.0K | PORT C | DMIC0 |
| 5.11K | | |
| 2.49K | Pull-up to AVDD | Pull-up to AVDD |

See reference design for more information on Jack Detect implementation.

2.2. Analog Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available:

- Port A
- Port C
- Port F

2.3. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of 7 possible inputs:

- Port A
- Port C
- Port F
- Mixer Output
- DMIC 0

2.4. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG), all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

| Function | D0 | D1 ¹ | D2 | D3 | D3cold | Vendor Specific D4 | Vendor Specific D5 |
|---------------------------|----|-----------------|-----|------------------------|------------------------|------------------------|--------------------|
| Digital Microphone inputs | On | Off | Off | Off | Off | Off | Off |
| DAC | On | Off | Off | Off | Off | Off | Off |
| D2S | On | Off | Off | Off | Off | Off | Off |
| ADC | On | Off | Off | Off | Off | Off | Off |
| ADC Volume Control | On | Off | Off | Off | Off | Off | Off |
| Ref ADC | On | Off | Off | Off | Off | Off | Off |
| Analog Clocks | On | Off | Off | Off | Off | Off | Off |
| GPIO pins | On | On | On | On ⁵ | On | On | Off |
| VrefOut Pins | On | On | Off | Off | Off | Off | Off |
| Input Boost | On | On | Off | Off | Off | Off | Off |
| Analog mixer | On | On | Off | Off | Off | Off | Off |
| Mixer Volumes | On | On | Off | Off | Off | Off | Off |
| Analog PC_Beep | On | On | On | On | Off | Off | Off |
| Digital PC_Beep | On | On | On | On ⁵ | Off | Off | Off |
| Lo/HP Amps | On | On | On | Low Drive ² | Low Drive ² | Low Drive ² | Off |
| Capless HP Amps | On | On | On | Low Drive ² | Low Drive ² | Low Drive ² | Off |
| BTL Amp | On | On | On | Low Drive ² | Off | Off | Off |
| VAG amp | On | On | On | Low Drive ³ | Low Drive | Low Drive | Off |

Table 3. Power Management

| Function | D0 | D1 ¹ | D2 | D3 | D3cold | Vendor Specific D4 | Vendor Specific D5 |
|--------------------------|----|-----------------|----|-----------------|---------|--------------------|--------------------|
| Port Sense | On | On | On | On ⁴ | Off | Off | Off |
| Reference Bias generator | On | On | On | On | On | On | Off |
| Reference Bandgap core | On | On | On | On | On | On | Off |
| HD Audio-Link | On | On | On | On ⁵ | Limited | Off | Off |

Table 3. Power Management

1. No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2. VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance.
3. VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. Both AVDD and DVDD must be available for Port Sense to operate.
5. Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under IDT Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.5. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.6. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from the D1 to the D0 state within 1 mS.

2.7. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.8. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To

enable this use model, the CODEC must resume within 10mS and not pop. Intel HDA015-B / Low Power White paper power goals are < 30mW when analog PC_Beep is not enabled, and < 60mW when analog PC_Beep is enabled. (Charge pump and BTL amplifier power excluded.)

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the HDA015-B section for more information):

| Function | HDA Bus active | HDA Bus stopped |
|-----------------------------------|----------------------|---|
| Port Presence Detect state change | Unsolicited Response | Wake Event ¹ followed by an unsolicited response |
| GPIO state change | Unsolicited Response | Wake Event followed by an unsolicited response |

1. The Port Presence detect circuit is currently dependent on a clock and must be changed to generate a wake event.

2.8.1. AFG D3cold

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus HDA015-B, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.

2.9. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and HDA015-B. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5. The preferred method is to request D3cold, then select D4 or D5 as desired. This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.10. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; the voltage selection is done dynamically based on the input voltage of DVDD_IO.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.11. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

| | | |
|--------------|--------------|--------|
| ADC1 CnvtrID | (NID = 0x08) | |
| | [3:0] | Ch = 2 |
| ADC0 CnvtrID | (NID = 0x07) | |
| | [3:0] | Ch=0 |

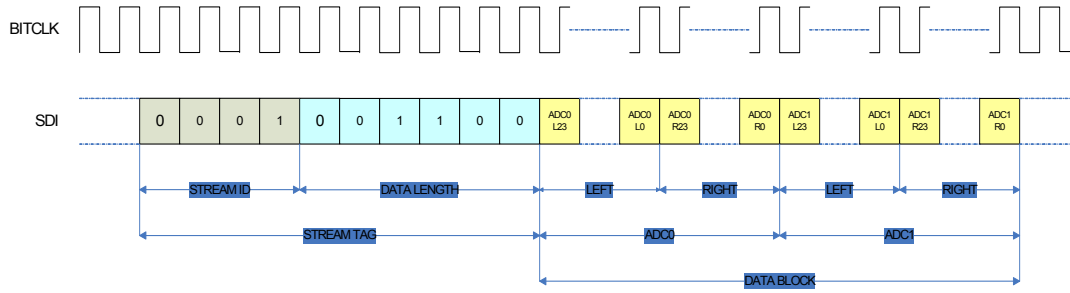
Table 4. Example channel mapping

Figure 1. Multi-channel capture

| | | | | | | |
|--------------------------|-----------|-------------|--------------|---------------|--------------|---------------|
| ADC0.CnvtrID.Channel = 0 | Stream ID | Data Length | ADC0 | ADC0 | ADC1 | ADC1 |
| ADC1.CnvtrID.Channel = 2 | | | Left Channel | Right Channel | Left Channel | Right Channel |
| ADC0.CnvtrID.Channel = 2 | Stream ID | Data Length | ADC1 | ADC1 | ADC0 | ADC0 |
| ADC1.CnvtrID.Channel = 0 | | | Left Channel | Right Channel | Left Channel | Right Channel |

The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 2. Multi-channel timing diagram



| ADC[1:0] Cnvtr | Bit Number | Sub Field Name | Description |
|----------------|------------|----------------|--|
| | [15] | StrmType | Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported) |
| | [14] | FrmtSmplRate | Sample Base Rate 0= 48kHz 1=44.1KHz |
| | [13:11] | SmplRateMultp | Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 100-111= Reserved |
| | [10:8] | SmplRateDiv | Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported) |

Table 5: Mult-channel

| | | | |
|--|-------|-------------|---|
| | [6:4] | BitsPerSmpl | Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved |
| | [3:0] | NmbrChan | Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels ... 1111= 16 channels. |
| | [7:4] | Strm | Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused. |
| | [3:0] | Ch | Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2. |

Table 5: Mult-channel

2.12. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, and DMIC_CLK 3-pin interface. The DMIC0 signal is an input that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The DMIC data input is reported as a stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-B input.

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

The codec supports the following digital microphone configurations:

| Digital Mics | Data Sample | ADC Conn. | Notes |
|--------------|-----------------------------------|-----------|--|
| 0 | N/A | N/A | No Digital Microphones |
| 1 | Single Edge | 0, or 1 | When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for "Left" and select mono operation using the vendor specific verb. "Left" D-mic data is used for ADC left and right channels. |
| 2 | Double Edge on either DMIC_0 or 1 | 0, or 1 | External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge (multiplexed output) capability. |

| Power State | DMIC Widget Enabled? | DMIC_CLK Output | DMIC_0,1 | Notes |
|-------------|----------------------|-----------------|----------------|---|
| D0 | Yes | Clock Capable | Input Capable | DMIC_CLK Output is Enabled when either DMIC_0 or Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low |
| D1-D3 | Yes | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D0-D3 | No | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D4 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D5 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |

Figure 3. Single Digital Microphone (data is ported to both left and right channels)

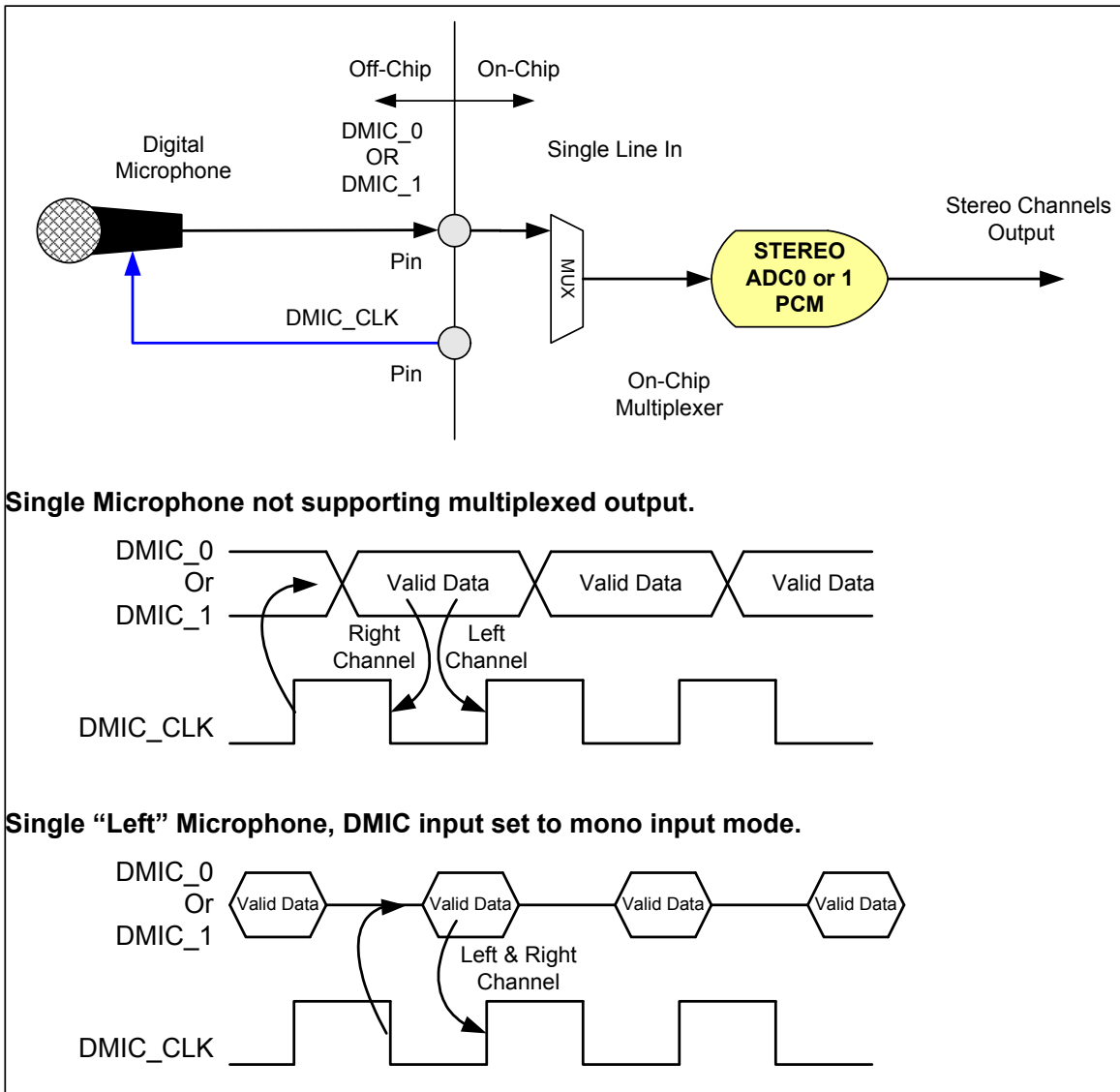
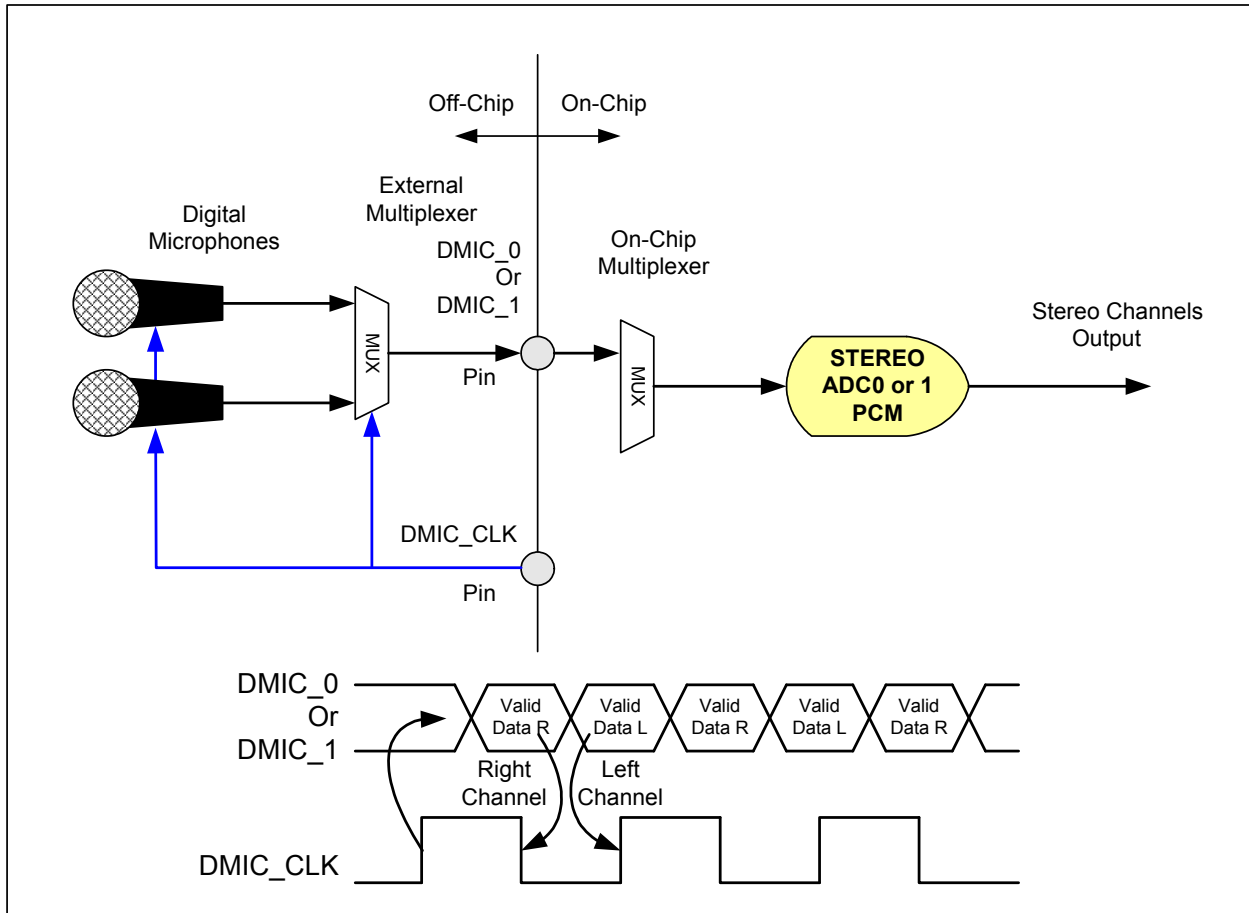


Figure 4. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

2.13. Analog PC-Beep

The codec does not support automatic routing of the PC_Beep pin to all outputs when the HD-Link is in reset. Analog PC-Beep may be supported during HD-Link Reset if analog PC_Beep is manually enabled before entering reset and the level shifters are locked. Analog PC_Beep is mixed at the port and only ports enabled as outputs will pass PC_Beep. Analog PC_Beep (or a digital equivalent) must not prevent passing WLP when analog PC_Beep is enabled. Analog PC_Beep, when enabled, must not prevent other audio sources from playing (we must mix not mux.) An activity monitor will allow the BTL amplifier (and cap-less headphone amplifiers if possible) to remain in shutdown when the function group is in D3 until the beep pin is active and then quickly change to an active state (within 10mS) to pass the beep tone. Beeps from ICH (from Beep.sys) can have a frequency of about 37Hz to about 32KHz. Beep duration is programmable from 1mS to about 32 seconds. A typical beep under Windows XP is 500Hz or 2KHz and lasts 75ms or 150mS. Due to external XOR gates used as mixers, the idle state may be logic 0 or logic 1.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced.

Analog PC_Beep is not supported in D3 Cold, or the vendor specific states D4/D5.

2.14. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz HD Audio Sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced. Digital PC_Beep requires a clock to operate and the CODEC will prevent the system from stopping the bus clock while in D3 by setting the Clock_Stop_OK bit to 0 to indicate that the part requires a clock.

2.15. Headphone Drivers

The codec implements capless headphone outputs. The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.)

The capless headphone drivers are supplied with +/-2.5V derived from AVDD. Therefore, it is possible to run the headphone supply from 5V and maintain ~60mW peak output power into 32 ohm headphones. Headphone performance will degrade if more than one port is driving a 32 ohm load.

2.16. EAPD

The EAPD pin (pin 47) is a dedicated, bi-directional control pin. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The default state of this pin is 0 (driving low.) The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and HDA015-B, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low. A port will request External Amp Power Up when its power state is active (FG and pin widget power state is D1 or D0) or (Analog PC_Beep is enabled and port is enabled as an output) and the port's EAPD bit is set to 1. The state of the EAPD pin (unless configured as an input or held low by an external circuit when configured as an open drain output) will be the logical OR of the external amp power up requests from all ports.

By default, the EAPD pin also functions as the Mute#/ShutDown# input for the internal BTL amplifier. In this mode, a low value at the pin (either due to internal EAPD being 0, or to an external entity forcing the pin low) will cause the internal BTL amplifier to mute or enter a low power state depending on the amplifier configuration. (See below)

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by a power on reset:

| MODE1 | MODE0 | EAPD Pin Function | Description |
|-------|-------|-------------------|--|
| 0 | 0 | Open Drain I/O | Value at pin is wired-AND of EAPD bit and external signal. (default) |
| 0 | 1 | CMOS Output | Value of EAPD bit in pin widget is forced at pin |
| 1 | 0 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |
| 1 | 1 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |

| Control Flag | Description |
|-------------------|---|
| EAPD PIN MODE 1:0 | Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain) |
| BTL/HP SD | 0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only |
| BTL/HP SD MODE | 0 = Amp will mute when disabled. / 1 = Amp will shut down (enter a low power state) when disabled (default) |
| BTL/HP SD INV | 0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high. |

| BTL SD | BTL SD MODE | BTL SD INV | EAPD Pin State | Amp State |
|--------|-------------|------------|----------------|---|
| 0 | 0 | 0 | 0 | Amplifier is mute |
| 0 | 0 | 0 | 1 | Amplifier is active |
| 0 | 0 | 1 | 0 | Amplifier is active |
| 0 | 0 | 1 | 1 | Amplifier is mute |
| 0 | 1 | 0 | 0 | Amplifier is in a low power state (default ¹) |
| 0 | 1 | 0 | 1 | Amplifier is active |
| 0 | 1 | 1 | 0 | Amplifier is active |
| 0 | 1 | 1 | 1 | Amplifier is in a low power state |
| 1 | 0 | NA | NA | Amplifier follows pin/function group power state and will mute when disabled |
| 1 | 1 | NA | NA | Amplifier follows pin/function group power state and will enter a low power state when disabled |

Table 6. BTL Amp Status

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

| HP SD | HP SD MODE | HP SD INV | EAPD Pin State | Headphone Amp State |
|-------|------------|-----------|----------------|---|
| 0 | 0 | 0 | 0 | Amplifier is mute |
| 0 | 0 | 0 | 1 | Amplifier is active |
| 0 | 0 | 1 | 0 | Amplifier is active |
| 0 | 0 | 1 | 1 | Amplifier is mute |
| 0 | 1 | 0 | 0 | Amplifier is in a low power state (default ¹) |
| 0 | 1 | 0 | 1 | Amplifier is active |
| 0 | 1 | 1 | 0 | Amplifier is active |
| 0 | 1 | 1 | 1 | Amplifier is in a low power state |
| 1 | 0 | NA | NA | Amplifier follows pin/function group power state and will mute when disabled |
| 1 | 1 | NA | NA | Amplifier follows pin/function group power state and will enter a low power state when disabled |

Table 7. Headphone Amp Enable Configuration

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

| BEEP Override | EAPD Pin value ¹ | Description |
|---------------|--------------------------------|--|
| 0 | Forced to low when in D2 or D3 | Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit. |
| 1 | Always follows EAPD bit | Power state is ignored and EAPD pin follows EAPD bit value only to allow PC_Beep support in D2 and D3 |

Table 8. EAPD Low Power Behavior

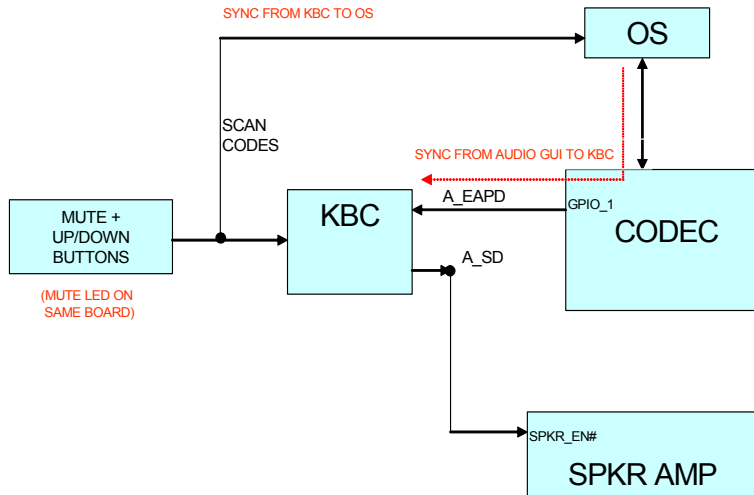
1. When pin is enabled as Open Drain or CMOS output.

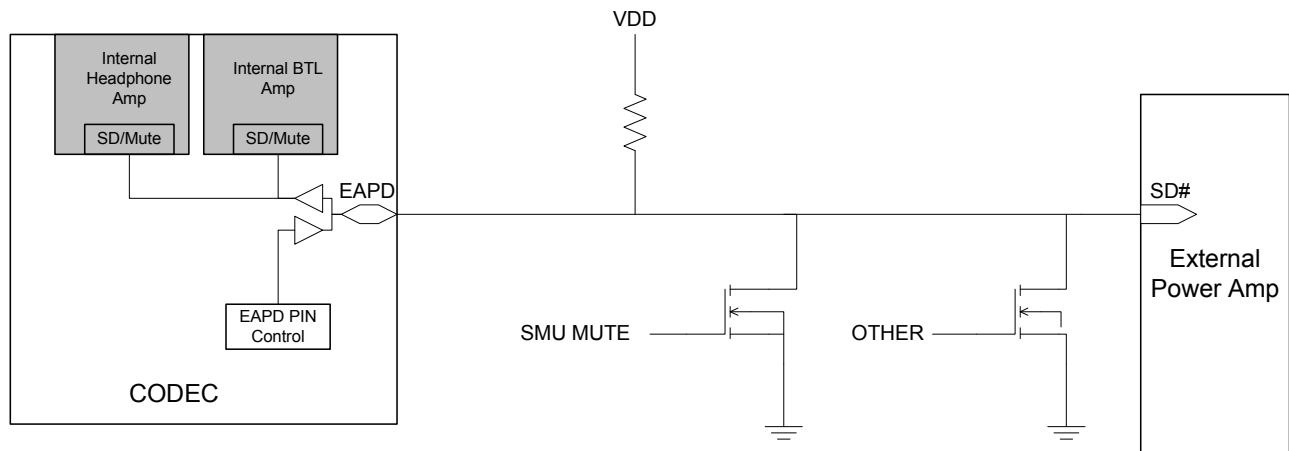
| AFG Power State | RESET# | BEEP Override | EAPD Power State | Pin Behavior |
|-----------------|--------------------|---------------|------------------|---|
| D0-D3 | Asserted (Low) | - | - | Active low immediately after power on, otherwise the previous state is retained across FG and link reset events |
| D0 | De-Asserted (High) | - | - | Active - Pin reflects EAPD bit unless held low by external source. |
| D1 | De-Asserted (High) | - | D0-D1 | Active - Pin reflects EAPD bit unless held low by external source. |
| D2 | De-Asserted (High) | Disabled | D0-D2 | Pin forced low to disable external amp |
| D2 | De-Asserted (High) | Enabled | D0-D2 | Active - Pin reflects EAPD bit unless held low by external source. |
| D3 | De-Asserted (High) | Disabled | D0-D3 | Pin forced low to disable external amp |
| D3 | De-Asserted (High) | Enabled | D0-D3 | Active - Pin reflects EAPD bit unless held low by external source. |
| D3cold | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D4 | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D5 | De-Asserted (High) | - | - | Pin Hi-Z (off) |

Table 9. EAPD Behavior

Figure 5. HP EAPD Example to be replaced by single pin for internal amp

HP AUDIO CONTROL BLOCK DIAGRAM





2.17. BTL Amplifier

An integrated class-AB stereo BTL amplifier is provided to directly drive 4 ohm speaker (2W @ 4.75V) or 8 ohm speaker (1W @ 4.75V). No external filter is needed for cable runs of 18" or less. An internal DC blocking filter prevents distortion when the audio source has DC content, and prevents unintentional power consumption when pausing audio playback. The amplifier may be controlled using the EAPD pin (see EAPD section.)

The BTL amplifier includes thermal management circuitry. When the CODEC reaches a temperature of about 135 degrees, the output amplitude of the BTL amp is gradually lowered until the temperature falls below 135.

Maximum gain for the BTL amplifier is programmable. The following 4 gain settings relative to a nominal line output are desired: +6.5dB, +9.5dB, +14.5dB and +16.5dB. Absolute gain may vary and the suggested accuracy is +/-1.5dB. The gain is exposed in a vendor specific widget and is intended to mimic the pin programmable gain implemented in discrete BTL amplifiers commonly used in notebook computers.

2.18. BTL Amplifier High-Pass Filter

Not available on TB revision.

For mobile applications, speakers are often incapable of reproducing low frequency audio and unable to handle the maximum output power of the BTL amplifier. A high-pass filter is implemented in the DAC output path to reduce the amount of low frequency energy reaching speakers attached to the BTL amplifier. This can prevent speaker failure.

2.18.1. Filter Description

The high-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off. The filter may be programmed for a -3dB response at: 100Hz, 200Hz, 300Hz, 400Hz, 500Hz, 750Hz, 1KHz, or 2KHz. The high pass filter is enabled by default with a cut-off frequency of 300Hz. The filter may be bypassed using the associated verb (processing state verb).

The filter is implemented in digital before the Digital to Analog converter. There are 2 major consequences to implementing the filter in the digital domain:

1. All ports connected to the DAC will be affected by the high-pass filter when it is enabled.
2. Analog paths (such as when the microphone input is routed through the mixer to the BTL amplifier) are not affected.

Like the other analog inputs, PC_Beep is not affected by the digital high-pass filter. To ensure that the speakers attached to the BTL amplifier are not harmed by low frequency audio entering the PC_Beep input, an external filter must be implemented. Fortunately, it is common practice to implement an attenuation circuit and DC blocking capacitor at the PC_Beep input. This attenuator/filter is easily adjusted to restrict low frequency audio. The easiest approach is to reduce the value of the DC blocking capacitor but other approaches are equally effective.

2.19. GPIO

2.19.1. GPIO Pin mapping and shared functions

| GPIO # | Pin | Supply | GPIO | GPI | GP O | VrefOut | DMIC | VOL | Pull Up | Pull Down |
|--------|-----|--------|------|-----|---------|---------|------|-----|------------|--------------|
| 1 | 2 | DVDD | YES | | | | CLK | | | 50K |
| 2 | 3 | DVDD | YES | | | | IN | | | 50K |

2.19.2. Digital Microphone/GPIO Selection

2 functions are available on the DMIC_CLK/GPIO1 (pin 2) and the DMIC_0/GPIO2 (pin 3) pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIOs are not enabled through the AFG, then at reset, pins 2 and 4 are pulled low by an internal pull-down resistor.
2. If the GPIO 1 is enabled, the 2 DMIC pins become mute (unless programmed for GPIO use) and pin 2 becomes an internal pull-down.
3. If GPIO2 is enabled through the AFG, pin 3 becomes a GPIO and is pulled low by an internal pull-down resistor.
4. If the port is enabled as an input, the digital microphones will be used.
5. If the port is not enabled as an input or if the pin is configured as a GPIO, the digital microphone path will be mute.

2.20. HD Audio HDA015-B support

Although HDA015-B is not yet complete (not a DCN), the 92HD87 will implement complete support for the specification building on the support already present in previous products. HDA015-B features supported are:

- Persistence of many configuration options through bus and function group reset.
- The ability to support port presence detect in D3 even when the HD Audio bus is in a low power state (no clock.)
- Fast resume times from low power states: 1ms D1 to D0, 2ms D2 to D0, 10mS D3 to D0.
- Notification if persistent register settings have been unexpectedly reset.

2.21. Digital Core Voltage Regulator

The digital core operates from 1.4 to 1.98V making it compatible with 1.5V (5%) and 1.8V (10%) supply voltages. Many systems require that the CODEC use a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 7, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

The digital core voltage regulator is only dependent on DVDD. The CODEC digital logic and I/O (unless referenced to AVDD) will operate in the absence of AVDD. DVDD and AVDD supply sequencing for the application of power and the removal of power is neither defined nor guaranteed. It is common for desktop systems to supply AVDD from the system standby supply and the CODEC will tolerate, indefinitely, the condition where AVDD is active but DVDD and DVDDIO are inactive.

To prevent pops, software is expected to mute paths as close to the port as is possible when changing power states or signal topology.

2.22. Aux Audio Support

The codec supports an auxiliary audio mode where analog audio is supported by default after power is supplied with the HD Audio bus disabled. In this mode, an analog input is routed to one of several output ports depending on jack presence detection.

In addition to shutting off the CODEC BTL and headphone amplifiers when the docked device output jack is used, the BTL amplifier will be disabled when the headphone jacks are used, and the headphone amplifiers will be disabled when not in use.

2.22.1. General conditions in Aux Audio Mode:

- HD Audio Link is off (RST# is 0, active, and BitClk is 0, inactive. CODEC does not need to monitor BitClk to enter/exit this mode but must not depend on BitClk to operate.)
- HD Audio CODEC analog and digital supplies are active.
- Port A may be an optional headphone jack (Normal and Aux Audio Mode) or an internal microphone port (Normal Mode only)
- Port B connect to the system headphone jack.
- Port C connects to the system microphone Jack
- Port D connects to the internal speakers.
- Port E is not present on the CODEC but the port presence detect is available and used to control internal resources.
- Port F is connected to the dock AUX Audio In (it is an input port)
- EAPD is used to control the power state of the mixer, BTL amplifier, and headphone amplifiers. The amplifiers are off if EAPD is held low.
- Internal circuitry will delay enabling (change power state, un-mute, etc.) the output amplifiers after the application of power or EAPD=1 to prevent pops.
- Internal circuitry will orchestrate power down (EAPD = 0) to prevent pops.
- EAPD must be forced low before removing power.
- No special Dock Present signal needed. Only port presence detect for port E is used to disable the speaker amplifier if the docked device has something plugged into its headphone jack.
- DCN HDA015-B "clock-less D3" operation presents a problem. Clock Stop OK or similar communication will be used to prevent problems when an OS driver attempts to put the HD Audio bus controller into D3 to save power. The bus must not be place into reset with the clock stopped or

unless EAPD is forced low or D3cold has been set. The Enable bit in the Aux Audio vendor specific verb is provided so firmware or other software can disable Aux Audio support and allow stopping the HD Audio bus when an OS is in an active state. The default value of this bit is determined by a bond option and may be determined by reading the device ID. This bit only returns to its default value when a power on reset event is generated.

2.22.2. **“Playback Path” Port Behavior**

Port F (Aux Audio In) input is routed to Port D (“internal speakers”) and Ports A&B (system headphone jacks) through the analog mixer.

2.22.3. **When Port E presence detect = 0**

- Presence detect for Port E = 0 (nothing plugged in)
- Port F, the “Aux Audio In”, input is routed to Port A, B, or D when that port is active.
- If either Port A or Port B is in use (port presence detect = 1), Port D, internal speakers, will be inactive (off)
- To save power, the power supply for Port B will be active only if Port B is in use (Port B presence detect = 1).
- If neither Port A nor Port B is in use (port presence detect = 0), Port D, internal speakers, will be active and ports A and B will be inactive.
- EAPD must not be forced low due to the dock being absent or high when a dock is present. EAPD is used to indicate if AUX Audio Mode is in use.

2.22.4. **When Port E presence detect = 1**

- Presence detect for Port E = 1 (something plugged in)
- Port F, the “Aux Audio In”, input is routed to Ports A, B
- Port D is disabled
- If either Port A or Port B is in use (port presence detect = 1), that port will be enabled and output the audio entering Port F.
- To save power, the power supply for Port B will be active only if Port B is in use (Port B presence detect = 1).
- If neither Port A nor Port B is in use (port presence detect = 0), ports A and B will be inactive and the audio on Port F will play through the docked device (assuming that the docked device signals that headphones are plugged into the device by using the Port E presence detect.)
- EAPD must not be forced low due to the dock being absent or high when a dock is present. EAPD is used to indicate if AUX Audio Mode is in use.

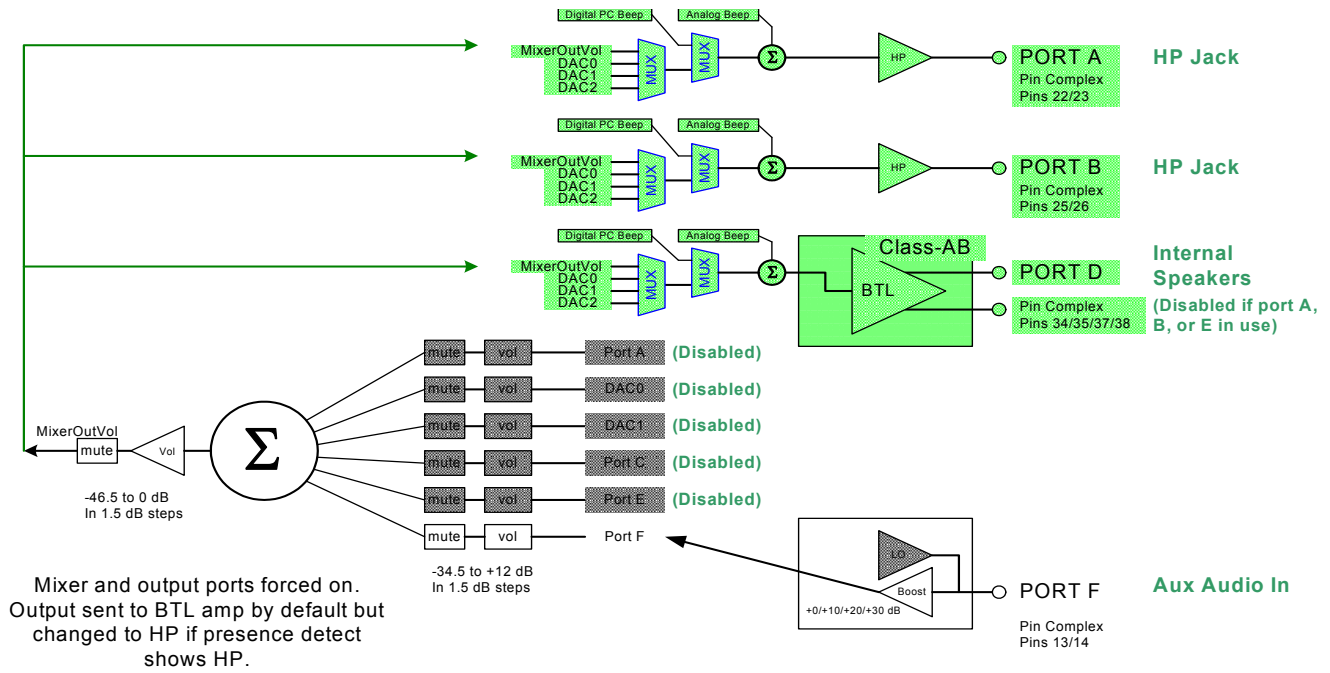


Figure 6. Aux Mode Block Diagram

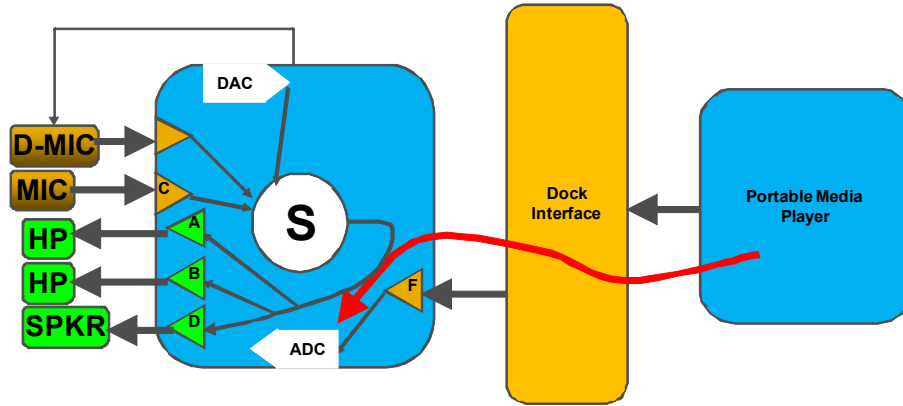
| EAPD (pin) | Aux Support Enable ¹ | Port E detect | Port B detect | Port A detect | Port C, D, F, DMIC detect | Port D behavior | Port B behavior | Port A behavior |
|------------|---------------------------------|---------------|---------------|---------------|---------------------------|-------------------------|-------------------------|-------------------------|
| 0 | NA | NA | NA | NA | NA | disabled | disabled | disabled |
| 1 | 0 | NA | NA | NA | NA | Widget controlled | Widget controlled | Widget controlled |
| 1 | 1 | 0 | 0 | 0 | NA | enabled (F to mix to D) | disabled | disabled |
| 1 | 1 | 0 | 0 | 1 | NA | disabled | disabled | enabled (F to mix to A) |
| 1 | 1 | 0 | 1 | 0 | NA | disabled | enabled (F to mix to B) | disabled |
| 1 | 1 | 0 | 1 | 1 | NA | disabled | enabled (F to mix to B) | enabled (F to mix to A) |
| 1 | 1 | 1 | 0 | 0 | NA | disabled | disabled | disabled |
| 1 | 1 | 1 | 0 | 1 | NA | disabled | disabled | enabled (F to mix to A) |
| 1 | 1 | 1 | 1 | 0 | NA | disabled | enabled (F to mix to B) | disabled |
| 1 | 1 | 1 | 1 | 1 | NA | disabled | enabled (F to mix to B) | enabled (F to mix to A) |

Table 10. Aux Mode Table

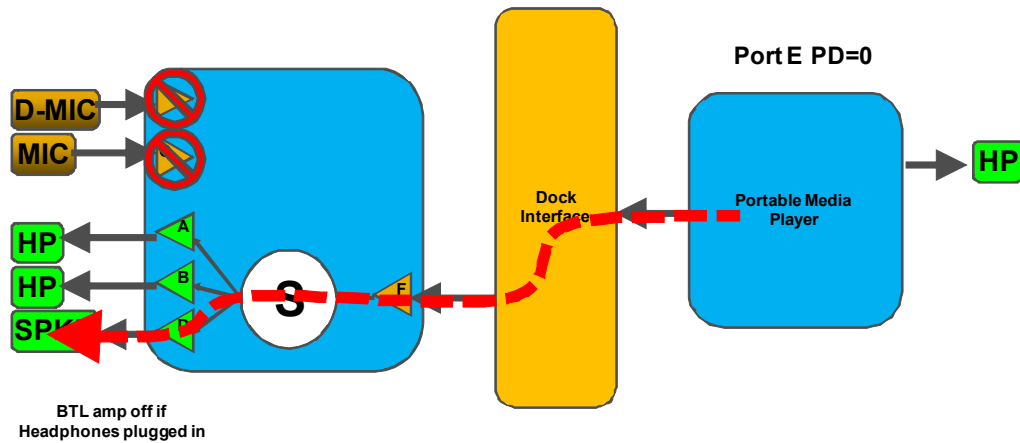
1.default value for Aux Audio Enable is determined by bond option.

2.22.5. SYSTEM DIAGRAMS

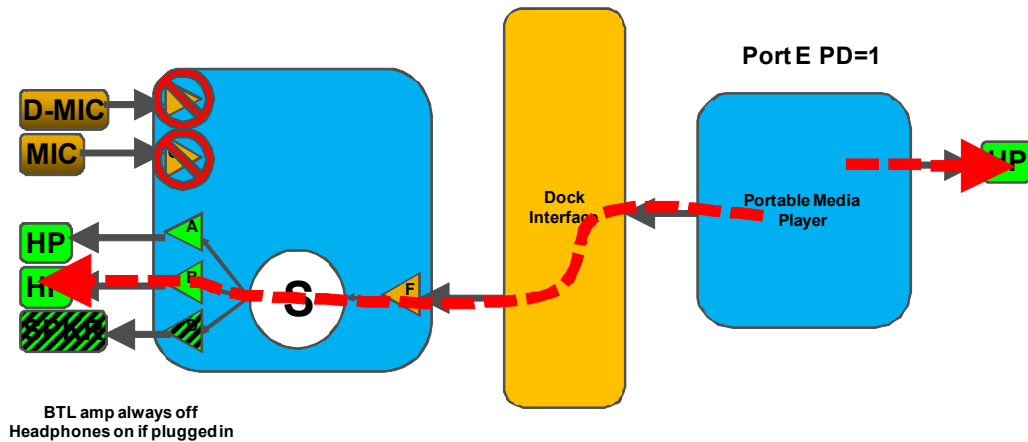
Docked – Normal Mode



Docked – Nothing plugged into docked player



Docked – Headphones plugged into docked player



2.22.6. EAPD

Since the Aux Audio mode overrides the default behavior but not the actual port settings when in reset, the logical state of the EAPD pin must be overridden as well. When Aux Audio mode is enabled and the part is in reset as described above, the logical state of EAPD will be 1 (External Amplifier Powered Up) unless held low by an external circuit. This ensures that audio pass-thru and analog PC_Beep will be supported.

2.22.7. Analog PC_Beep

Analog PC_Beep may be supported in Aux Audio mode. By default, analog PC_Beep is disabled. If the CODEC is programmed to enable analog PC_Beep and Aux Audio mode is enabled, the next time reset is asserted, the analog PC_Beep pin will be mixed at each of the active outputs.

2.22.8. Firmware/Software Requirements:

The reconfiguration outlined in this chapter is enabled by default (without the help of firmware or OS driver.)

This autonomous mode does not interfere with normal operation.

If it is desirable to stop the HD Audio bus while the CODEC is in D3 under OS control per DCN HDA015-B, Firmware must disable the AUX Audio Mode support in the CODEC prior to loading the OS. If Aux Audio Mode is not disabled in the CODEC, the CODEC will report to the OS driver that stopping the bus clock while the CODEC is in D3 is not supported or not available.

3. CHARACTERISTICS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD87. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Pin | Maximum Rating |
|---------------------------------------|------|---|
| Analog maximum supply voltage | AVdd | 6 Volts |
| Digital maximum supply voltage | DVdd | 5.5 Volts |
| VREFOUT output current | | 5 mA |
| Voltage on any pin relative to ground | | Vss - 0.3 V to Vdd + 0.3 V |
| Operating temperature | | 0 °C to +70 °C |
| Storage temperature | | -55 °C to +125 °C |
| Soldering temperature | | Soldering temperature information for all available in the package section of this datasheet. |

Table 11. Electrical Specification: Maximum Ratings

3.1.2. Recommended Operating Conditions

| Parameter | | Min. | Typ. | Max. | Units |
|-------------------------------|---|-------|------|-------|-------|
| Power Supplies | DVDD_Core | 1.4 | | 1.98 | V |
| | DVDD_IO (3.3V signaling) | 3.135 | 3.3 | 3.465 | V |
| | DVDD_IO (1.5V signaling) | 1.418 | 1.5 | 1.583 | V |
| Power Supply Voltage | Digital - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | (Note: With Supply Override Enable Bit set to force 5V operation.) Analog - 4 V | 3.8 | 4 | 4.2 | V |
| | Analog - 4.5 V | 4.51 | 4.75 | 4.99 | V |
| | Analog - 5 V | 4.75 | 5 | 5.25 | V |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Case Temperature | T _{case} (48-QFN) | | | +95 | °C |

Table 12. Recommended Operating Conditions

ESD: The 92HD87 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD87 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

3.2. 92HD87 Analog Performance Characteristics

(Tambient = 25 °C, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|--|---|-------------|----------|------------|--------|--------|
| Digital to Analog Converters | | | | | | |
| Resolution | | All | | 24 | | Bits |
| Dynamic Range ¹ : PCM to All Analog Outputs | -60dB FS signal level | 5V 4.75V | 93 93 | 100 100 | - | dB |
| SNR ² - DAC to All Mono/Line-Out Ports | Analog Mixer Disabled, PCM data | 5V 4.75V | 95 95 | | | dB |
| THD+N ³ - DAC to All Mono/Line-Out Ports | Analog Mixer Disabled, 0/-1/-3dB FS Signal, PCM data | 5V 4.75V | 83 83 | | | dBr |
| SNR ² - DAC to All Headphone Ports | Analog Mixer Disabled, 10KΩ load, PCM data | 5V 4.75V | 95 95 | | | dB |
| THD+N ³ - DAC to All Headphone Ports | Analog Mixer Disabled, 0/-1/-3dB FS Signal, 10KΩ load, PCM data | 5V 4.75V | 83 83 | | | dBr |
| SNR ² - DAC to All Headphone Ports | Analog Mixer Disabled, 32Ω load, PCM data | 5V 4.75V | 95 95 | | | dB |
| THD+N ³ - DAC to All Headphone Ports | Analog Mixer Disabled, 0dB FS Signal, 32Ω load, PCM data | 5V 4.75V | 68 68 | | | dBr |
| Any Analog Input (ADC) to DAC Crosstalk | 10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output. | All | -65 | - | - | dB |
| Any Analog Input (ADC) to DAC Crosstalk | 1KHz Signal Frequency see above | All | -65 | - | - | dB |
| DAC L/R crosstalk | DAC to LO or HP 20-15KHz into 10KΩ load | All | 65 | | | dB |
| DAC L/R crosstalk | DAC to HP 20-15KHz into 32Ω load | All | 65 | | | dB |
| Gain Error | Analog Mixer Disabled | All | | | 0.5 | dB |
| Interchannel Gain Mismatch | Analog Mixer Disabled | All | | | 0.5 | dB |
| D/A Digital Filter Pass Band ⁴ | | All | 20 | - | 21,000 | Hz |
| D/A Digital Filter Pass Band Ripple ⁵ | | | | | 0.1 | +/- dB |
| D/A Digital Filter Transition Band | | All | 21,000 | - | 31,000 | Hz |
| D/A Digital Filter Stop Band | | All | 31,000 | - | - | Hz |
| D/A Digital Filter Stop Band Rejection ⁶ | | All | -100 | - | - | dB |
| D/A Out-of-Band Rejection ⁷ | | All | -55 | - | - | dB |
| Group Delay (48KHz sample rate) | | All | - | - | 1 | ms |
| Attenuation, Gain Step Size DIGITAL | | All | - | 0.75 | - | dB |
| DAC Offset Voltage | | All | - | 10 | 20 | mV |
| Deviation from Linear Phase | | All | - | 1 | 10 | deg. |
| Analog Outputs | | | | | | |

Table 13. 92HD87 Analog Performance Characteristics

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|--|---|-------------|--------------|------------|-----|--------------|
| Full Scale All Mono/Line-Outs | DAC PCM Data | 5V 4.75V | 1.00 1.00 | - | - | Vrms |
| Full Scale All Mono/Line-Outs | DAC PCM Data | 5V 4.75V | 2.83 2.83 | - | - | Vp-p |
| All Headphone Capable Outputs | 32Ω load | 5V 4.75V | 40 40 | 60 60 | - | mW (peak) |
| Amplifier output impedance | Mono/Line Outputs Headphone Outputs | All | | 150 0.1 | | Ohms |
| External load Capacitance | Mono/Line Outputs Headphone Outputs | | | 220 | | pF |
| Analog inputs | | | | | | |
| Full Scale Input Voltage | 0dB Boost @4.75V (input voltage required for 0dB FS output) | 5V 4.75V | 1.05 | - | - | Vrms |
| All Analog Inputs with boost | 10dB Boost | 5V 4.75V | 0.320 | - | - | Vrms |
| All Analog Inputs with boost | 20dB Boost | 5V 4.75V | 0.105 | - | - | Vrms |
| All Analog Inputs with boost | 30dB Boost | 5V 4.75V | 0.032 | - | - | Vrms |
| Boost Gain Accuracy | | All | -1 | | | dB |
| Input Impedance | | All | - | 50 | - | KΩ |
| Input Capacitance | | All | - | 15 | - | pF |
| Analog Mixer | | | | | | |
| Dynamic Range: PCM to All Analog Outputs | -60dB FS signal level Analog Beep enabled all other mixer inputs mute | 5V 4.75V | 93 93 | | | |
| SNR ² - All Line-Inputs to all Line Outputs | All inputs unmuted, single line input driven by ATE. | 5V 4.75V | 85 85 | - | | dB |
| THD+N ³ - All Line-Inputs to all Line Outputs | 0dB Full Scale Input on one input, all others silent. | 5V 4.75V | 65 65 | - | | dBr |
| SNR ² - DAC to All Line Outputs | Analog Mixer Enabled, PCM data, all others inputes mute. | 5V 4.75V | 93 93 | - | | dB |
| THD+N ³ - DAC to All Line-Out Ports | Analog Mixer Enabled, 0/-1/-3dB FS signal, PCM data, all others inputes unmute/silent | 5V 4.75V | 83 83 | | | dBr |
| SNR ² - DAC to All Ports | Analog Mixer Enabled, PCM data, all others inputes unmute/silent. | 5V 4.75V | 85 85 | - | | dB |
| THD+N ³ - DAC to All Ports | Analog Mixer Enabled, 0dB FS Signal, PCM data, all others inputes unmute/silent | 5V 4.75V | 75 75 | - | | dBr |
| Attenuation, Gain Step Size ANALOG | | All | - | 1.5 | - | dB |
| Analog to Digital Converter | | | | | | |
| Resolution | | All | | 24 | | Bits |

Table 13. 92HD87 Analog Performance Characteristics

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|--|-------------|----------------|----------|--------|--------|
| Full Scale Input Voltage | 0dB Boost (input voltage required to generate 0dBFS per AES 17) | 5V 4.75V | 1.05 1.05 | | | |
| Dynamic Range ¹ , All Analog Inputs to A/D | High Pass Filter Enabled, -60dB FS, No boost | 5V 4.75V | 86 86 | 92 92 | | dB |
| SNR ² - All Analog Inputs to A/D | High Pass Filter enabled | 5V 4.75V | 86 86 | - | | dB |
| Full Scale Input Voltage | 20dB Boost (input voltage required to generate 0dBFS per AES 17) | 5V 4.75V | 0.105 0.105 | | | |
| Dynamic Range ¹ , All Analog Inputs to A/D | 20dB Boost High Pass Filter Enabled, -60dB FS | 5V 4.75V | 81 81 | | | |
| THD+N ³ All Analog Inputs to A/D | High Pass Filter enabled, -1/-3dB FS signal level | 5V 4.75V | 78 78 | | | dB |
| THD+N ³ All Analog Inputs to A/D | 20dB Boost, High Pass Filter enabled, -1/-3dB FS signal level | 5V 4.75V | 72 72 | | | dB |
| Analog Frequency Response ⁸ | | All | 10 | - | 30,000 | Hz |
| A/D Digital Filter Pass Band ⁴ | | All | 20 | - | 21,000 | Hz |
| A/D Digital Filter Pass Band Ripple ⁵ | | All | | | 0.1 | +/- dB |
| A/D Digital Filter Transition Band | | All | 21,000 | - | 31,000 | Hz |
| A/D Digital Filter Stop Band | | All | 31,000 | - | - | Hz |
| A/D Digital Filter Stop Band Rejection ⁶ | | All | -100 | - | - | dB |
| Group Delay | 48 KHz sample rate | All | - | - | 1 | ms |
| Any unselected analog Input to ADC Crosstalk | 10KHz Signal Frequency | All | -65 | - | - | dB |
| Any unselected analog Input to ADC Crosstalk | 1KHz Signal Frequency | All | -65 | - | - | dB |
| ADC L/R crosstalk | Any selected input to ADC 20-15Khz | All | -65 | | | dB |
| DAC to ADC crosstalk | DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz | All | -65 | | | dB |
| Spurious Tone Rejection ⁹ | | All | - | -100 | - | dB |
| Attenuation, Gain Step Size (analog) | | All | - | 1.5 | - | dB |
| Interchannel Gain Mismatch ADC | | All | - | - | 0.5 | dB |
| Power Supply | | | | | | |
| Power Supply Rejection Ratio | 10kHz | All | - | -60 | - | dB |
| Power Supply Rejection Ratio | 1kHz | All | - | -70 | - | dB |
| D0 Didd ¹⁰ | 3.3V, 1.8V, 1.5V | | | 25 | | mA |
| D0 Aidd ¹⁰ | 4.75V | | | 60 | | mA |
| D0 Didd ¹¹ | 3.3V, 1.8V, 1.5V | | | 20 | | mA |
| D0 Aidd ¹¹ | 4.75V | | | 34 | | mA |
| D1 Didd ¹² | 3.3V, 1.8V, 1.5V | | | 7 | | mA |

Table 13. 92HD87 Analog Performance Characteristics

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|--|----------------------------------|------|-----|-------------|-----|------|
| D1 Aidd ¹² | 4.75V | | | 30 | | mA |
| D2 Didd | 3.3V, 1.8V, 1.5V | | | 7 | | mA |
| D2 Aidd | 4.75V | | | 15 | | mA |
| D3 (Beep enabled) Didd ¹³ | 3.3V, 1.8V, 1.5V | | | 2 | | mA |
| D3 (Beep enabled) Aidd ¹³ | 4.75V | | | 10 | | mA |
| D3 Didd ¹³ | 3.3V, 1.8V, 1.5V | | | 2 | | mA |
| D3 Aidd ¹³ | 4.75V | | | 5 | | mA |
| D3cold Didd ¹³ | 3.3V, 1.8V, 1.5V | | | 1 | | mA |
| D3cold Aidd ¹³ | 4.75V | | | 5 | | mA |
| Vendor D4 Didd | 3.3V, 1.8V, 1.5V | | | 0.4 | | mA |
| Vendor D4 Aidd | 4.75V | | | 5 | | mA |
| Vendor D5 Didd | 3.3V, 1.8V, 1.5V | | | 0.4 | | mA |
| Vendor D5 Aidd | 4.75V | | | 0.6 | | mA |
| One Stereo ADC Didd | 3.3V, 1.8V, 1.5V | | | 4 | | mA |
| One Stereo ADC Aidd | 4.75 | | | 8 | | mA |
| One Stereo DAC Didd | 3.3V, 1.8V, 1.5V | | | 4 | | mA |
| One Stereo DAC Aidd | 4.75V | | | 6 | | mA |
| Voltage Reference Outputs | | | | | | |
| VREFOut ¹⁴ | | All | - | 0.5 X AVdd | - | V |
| VREFOut Drive | | All | | 1.6 | | mA |
| VREFILT (VAG) | | All | | 0.45 X AVdd | | V |
| Phased Locked Loop | | | | | | |
| PLL lock time | | All | | 96 | 200 | usec |
| PLL (or HD Audio Bit CLK) 24MHz clock jitter | | All | | 150 | 500 | psec |
| ESD / Latchup | | | | | | |
| Latch-up | As described in JESD78A Class II | All | | 70 | | degC |
| ESD - Human Body Model | As described in JESD22-A114-B | All | 2K | 3K | | V |
| Charged Device Model | As described in JESD22-C101 | All | 500 | 1K | | V |

Table 13. 92HD87 Analog Performance Characteristics

1. Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured "A weighted" over 20 Hz to 20 kHz bandwidth
2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. THD+N ratio as defined in AES17 and outlined in AES6id, non-weighted, over 20 Hz to 20 kHz bandwidth. Results at the jack are dependent on external components and will likely be 1 - 2dB worse.
4. Peak-to-Peak Ripple over Passband meets ± 0.125 dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
5. Peak-to-Peak Ripple over Passband meets ± 0.125 dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8. ± 1 dB limits for Line Output & 0 dB gain, at -20dBV

- 9. Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.
- 10. All functions/converters active, pin complexes enabled, two FDX streams, line (10Kohm) loads. Add 24mA analog current per stereo 32 ohm headphone.
- 11. One stereo DAC and corresponding pin widgets enabled (playback mode)
- 12. Mixer enabled
- 13. Idle measurement D3 set for minimum clicks/pops (biases and min. amps. on)
- 14. Can be set to 0.5 or 0.8 AVdd.

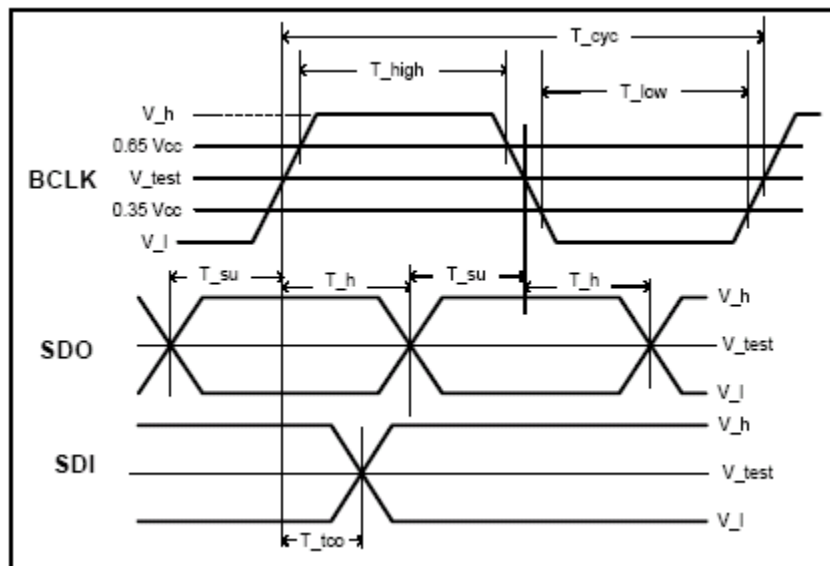
3.3. AC Timing Specs

3.3.1. HD Audio Bus Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|-----------------|--|-------------------|-------------|-------|-------------|-------|
| BCLK Frequency | Average BCLK frequency | | 23.997 6 | 24.0 | 24.002 4 | Mhz |
| BCLK Period | Period of BCLK including jitter | T _{cyc} | 41.163 | 41.67 | 42.171 | ns |
| BCLK High Phase | High phase of BCLK | T _{high} | 17.5 | | 24.16 | ns |
| BCLK Low Phase | Low phase of BCLK | T _{low} | 17.5 | | 24.16 | ns |
| BCLK jitter | BCLK jitter | | | 150 | 500 | ps |
| SDI delay | Time after rising edge of BCLK that SDI becomes valid | T _{tco} | 3 | | 11 | ns |
| SDO setup | Setup for SDO at both rising and falling edges of BCLK | T _{su} | 5 | | | ns |
| SDO hold | Hold for SDO at both rising and falling edges of BCLK | T _h | 5 | | | ns |

Table 14. HD Audio Bus Timing

Figure 7. HD Audio Bus Timing



3.3.2. Digital Microphone Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|--------------------|--|-----------|--------|--------|--------|-------|
| DMIC_CLK Frequency | Average DMIC_CLK frequency | | 1.176 | 2.352 | 4.704 | MHz |
| DMIC_CLK Period | Period of DMIC_CLK | Tdmic_cyc | 850.34 | 425.17 | 212.59 | ns |
| DMIC_CLK jitter | DMIC_CLK jitter | | | | 5000 | ps |
| DMIC Data setup | Setup for the microphone data at both rising and falling edges of DMIC_CLK | Tdmic_su | 5 | | | ns |
| DMIC Data hold | Hold for the microphone data at both rising and falling edges of DMIC_CLK | Tdmic_h | 5 | | | ns |

Table 15. Digital Mic timing

3.3.3. Class-AB BTL Amplifier Performance

| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| Output Power (BTL 4 ohm, 5V - Continuous Average Power)) | 2 | | | W |
| Output Power (BTL 8 ohm, 5V - Continuous Average Power)) | 1 | | | W |
| Amplifier Efficiency η (4 Ω , 5V, 2W) ¹ | | | 60 | % |
| THD+N (BTL 4 or 8 ohm, 5V, FS) | | | 1 | % |
| Frequency Response | 20 | - | 20K | Hz |
| Output voltage noise | | 50 | | uV |
| shutdown current | | 0.6 | | mA |

Table 16. Class-AB BTL Amplifier Performance

1. Amplifier efficiency includes circuits specific to the BTL amplifier audio path such as temperature limit, short circuit, and other support circuits.

3.3.4. Capless Headphone Supply Characteristics

| Parameter | Min | Typ | Max | Unit |
|-------------------------------------|-----|-----|-----|------|
| LDO idle current | | 1 | 2 | mA |
| Cap-less Headphone Amp idle current | | 2 | 3 | |
| Charge Pump idle current | | 4 | 6 | mA |
| Charge Pump shutdown time | | 1 | | mS |
| Charge Pump start-up time | | 10 | | mS |
| Frequency | | 384 | | KHz |
| C1/C2 cap value | | 2.2 | | uF |

Table 17. Capless Headphone Supply

4. FUNCTIONAL BLOCK DIAGRAMS

Port C is input only on the TB revision. RA revision is output capable.

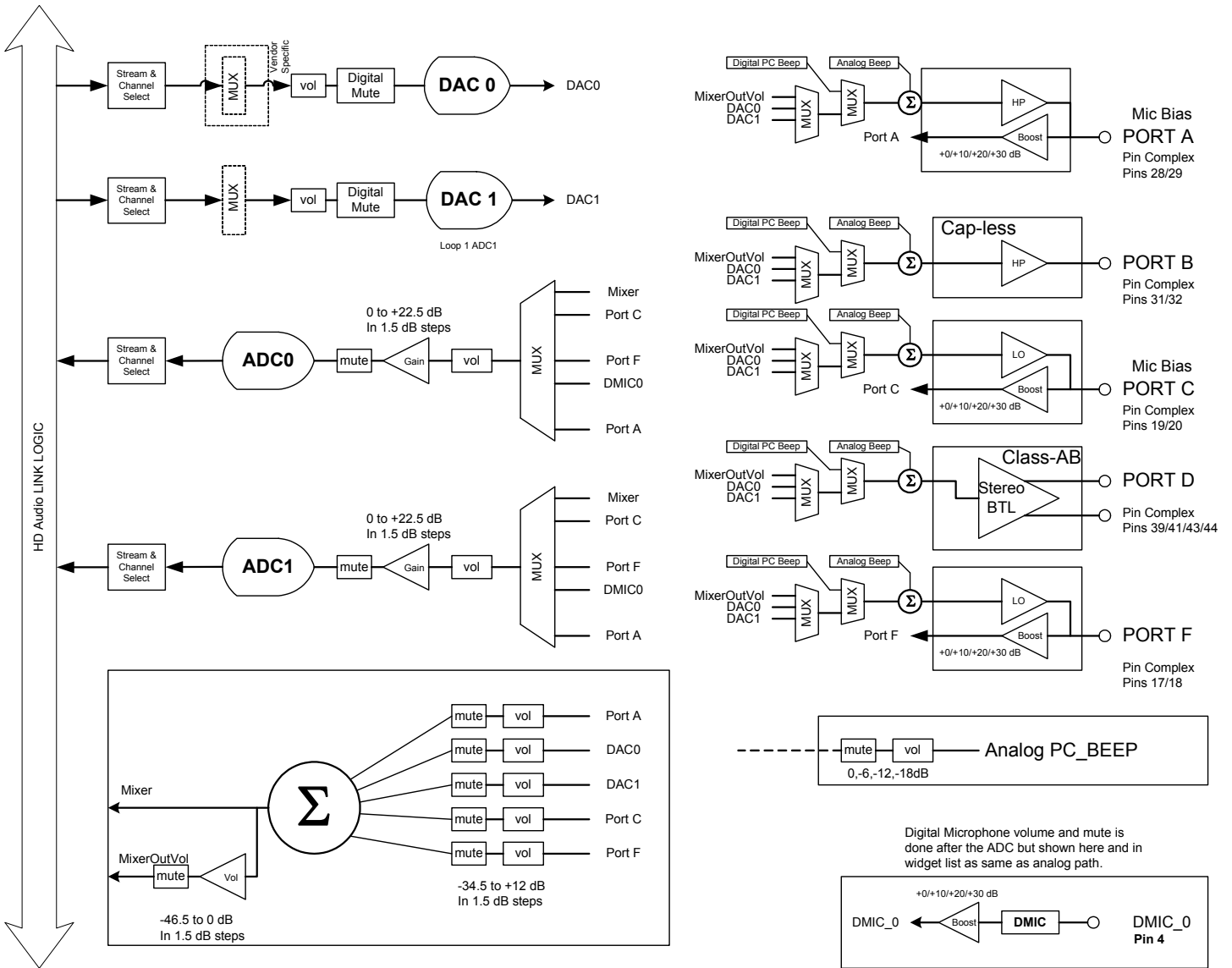


Figure 8. Functional Block Diagram

5. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS

Port C is input only on the TB revision. RA revision is output capable

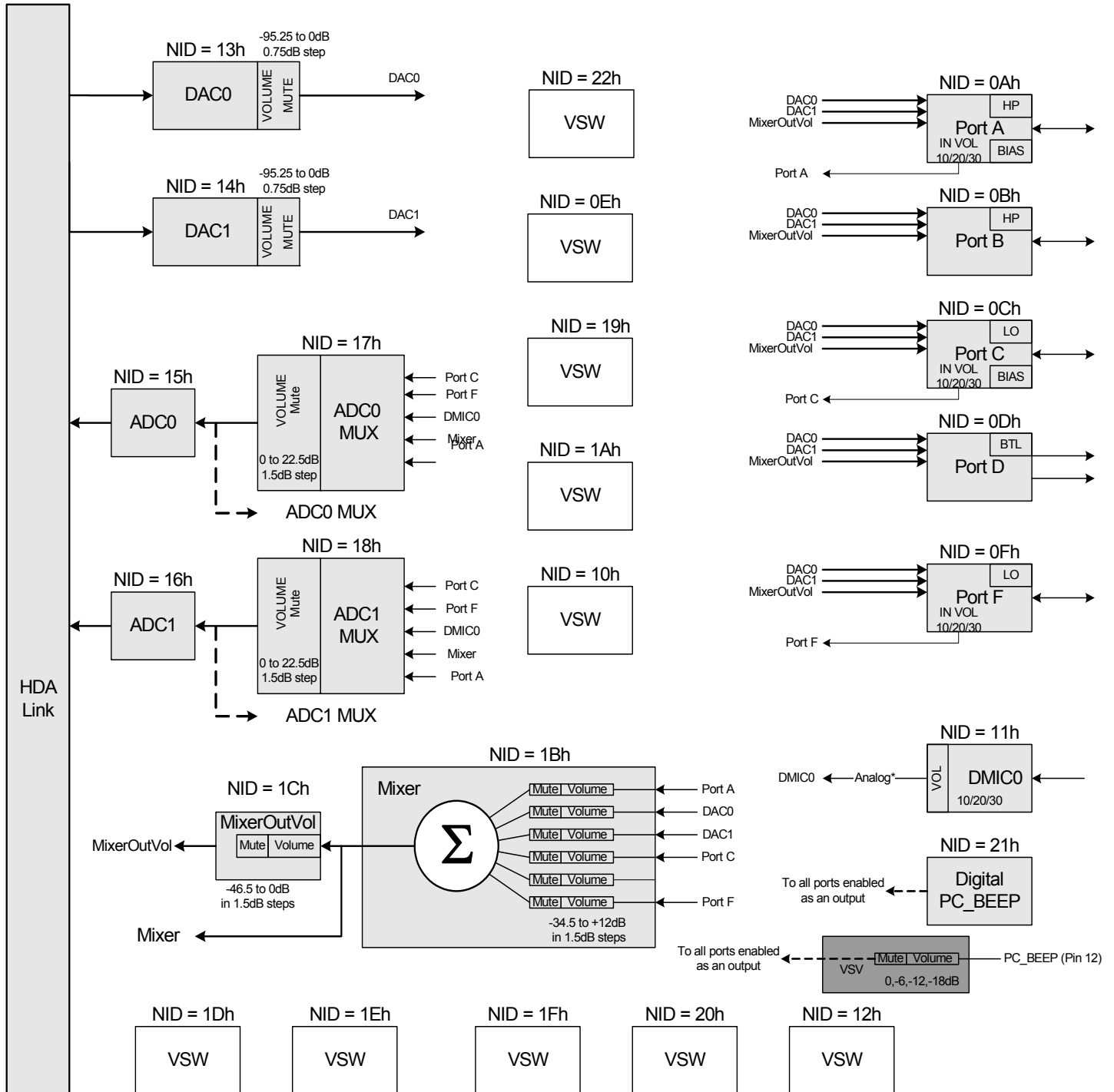


Figure 9. Widget Diagram

6. PORT CONFIGURATIONS

Port C is input only on the TB revision. RA revision is output capable

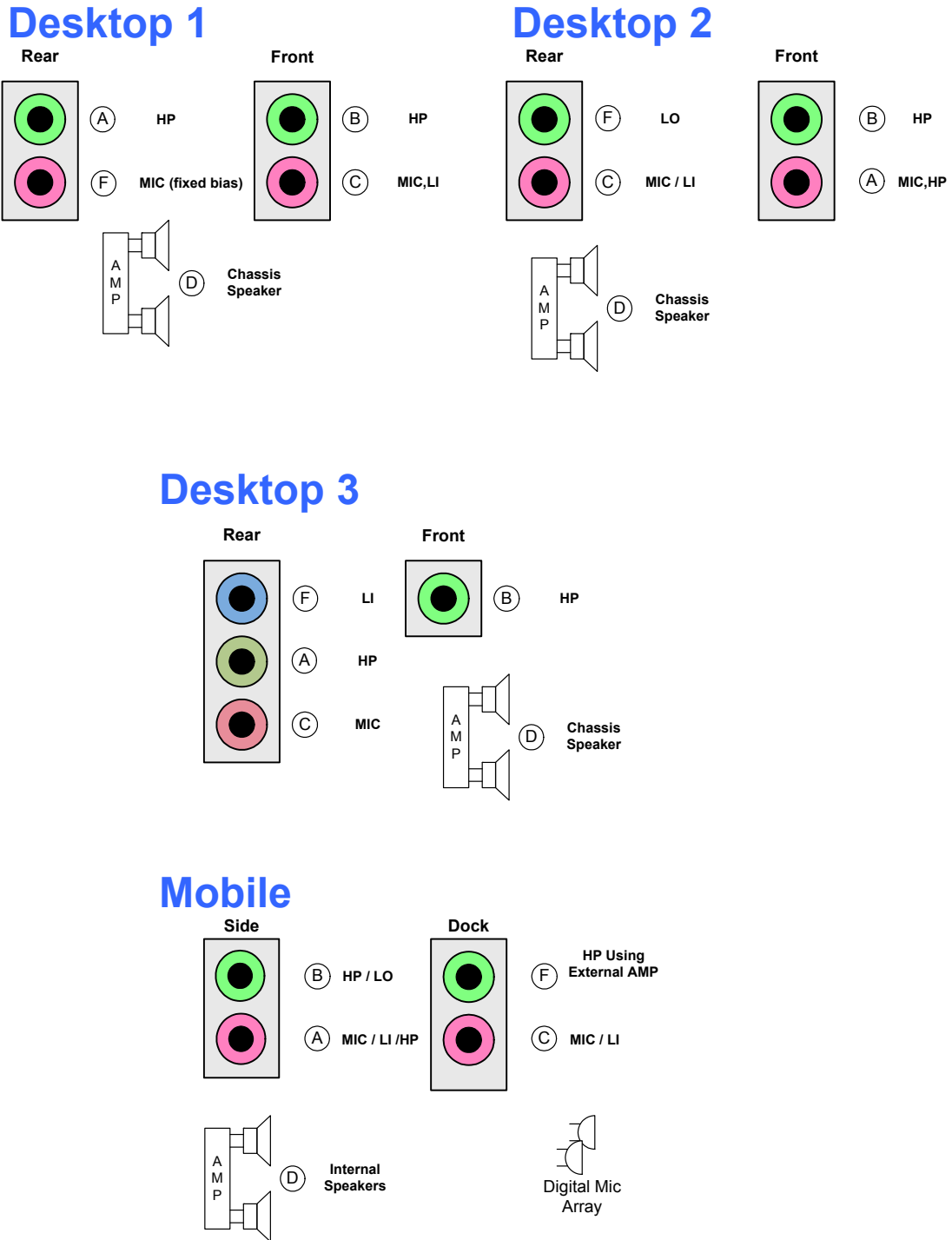


Figure 10. Port Configurations

6.1. Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Mobile 3-jack implementation with 3 HP jacks in front and 2 jacks in rear. The internal speaker is redirected from the front (green) headphone jack, while the other (black) headphone jack and microphone jack may be used for RTC.

| Pin Name | Port | Location | Device | Connection | Color | Misc | Pin Name | Port |
|------------|---------------------|--------------------|------------|------------------|------------|------------------------|----------|------|
| PortAPin | Connect to Jack 00b | Mainboard Front 2h | HP Out 2h | 1/8 inch Jack 1h | Green 4h | Jack Detect Override=0 | 3h | Fh |
| PortBPin | Connect to Jack 00b | Mainboard Front 2h | HP Out 2h | 1/8 inch Jack 1h | Black 1h | Jack Detect Override=0 | 1h | 0h |
| PortCPin | Connect to Jack 00b | Mainboard Front 2h | Mic In Ah | 1/8 inch Jack 1h | Pink 9h | Jack Detect Override=0 | 2h | 0h |
| PortDPin | Internal 10b | NA 010000b | Speaker 1h | Other Analog 7h | Unknown 0h | Jack Detect Override=0 | 3h | 0h |
| PortFPin | Connect to Jack 00b | Mainboard Rear 1h | Line In 8h | 1/8 inch Jack 1h | Pink 9h | Jack Detect Override=0 | 4h | 0h |
| DigMic0Pin | Internal 10b | Internal 010000b | Mic In Ah | ATAPI 3h | Unknown 0h | Jack Detect Override=0 | 4h | 1h |

Table 18. Pin Configuration Default Settings

Port C is input only on the TB revision. RA revision is output capable

7. WIDGET INFORMATION

| Bits [39:32] | Bits [31:28] | BITS [27:20] | BITS[19:16] | BITS [15:0] |
|--------------|---------------|--------------|-----------------|-----------------------|
| Reserved | CODEC Address | NID | Verb ID (4-bit) | Payload Data (16-bit) |

Table 19. Command Format for Verb with 4-bit Identifier

| Bits [39:32] | Bits [31:28] | BITS [27:20] | BITS[19:8] | BITS [7:0] |
|--------------|---------------|--------------|------------------|----------------------|
| Reserved | CODEC Address | NID | Verb ID (12-bit) | Payload Data (8-bit) |

Table 20. Command Format for Verb with 12-bit Identifier

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in the tables below. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

| Bit [35] | Bit [34] | BITS [33:32] | BITS[31:0] |
|-------------------|-----------|--------------|------------|
| Valid (Valid = 1) | UnSol = 0 | Reserved | Response |

Table 21. Solicited Response Format

| Bit [35] | Bit [34] | BITS [33:32] | BITS[31:28] | BITS [27:0] |
|-------------------|-----------|--------------|-------------|-------------|
| Valid (Valid = 1) | UnSol = 1 | Reserved | Tag | Response |

Table 22. Unsolicited Response Format

7.1. Widget List

| ID | Widget Name | Description |
|-----|-----------------|---|
| 00h | Root | Root Node |
| 01h | AFG | Audio Function Group |
| 0Ah | Port A | Port A Pin Widget (Capless Headphone) |
| 0Bh | Port B | Port B Pin Widget (Capless Headphone) |
| 0Ch | Port C | Port C Pin Widget (Line IN/OUT, MIC) (Line IN, MIC on TB revision) |
| 0Dh | Port D | Port D Pin Widget (BTL output - EAPD control) |
| 0Eh | Vendor Reserved | Vendor Reserved |
| 0Fh | Port F | Port F Pin Widget (Line IN/OUT, MIC) |
| 10h | Vendor Reserved | Vendor Reserved |
| 11h | DigMic0 | Digital Microphone 0 Pin Widget |

Table 23. High Definition Audio Widget

| ID | Widget Name | Description |
|-----|-----------------|---|
| 12h | Vendor Reserved | Vendor Reserved |
| 13h | DAC0 | Stereo Output Converter to DAC |
| 14h | DAC1 | Stereo Output Converter to DAC |
| 15h | ADC0 | Stereo Input Converter to ADC |
| 16h | ADC1 | Stereo Input Converter to ADC |
| 17h | ADC0Mux | ADC0 Mux with volume and mute |
| 18h | ADC1Mux | ADC1 Mux with volume and mute |
| 19h | Vendor Reserved | Vendor Reserved |
| 1Ah | Vendor Reserved | Vendor Reserved |
| 1Bh | Mixer | Input Mixer (Input Ports, DACs, Analog PC_Beep) |
| 1Ch | MixerOutVol | Volume control for analog mixer |
| 1Dh | Vendor Reserved | Vendor Reserved |
| 1Eh | Vendor Reserved | Vendor Reserved |
| 1Fh | Vendor Reserved | Vendor Reserved |
| 20h | Vendor Reserved | Vendor Reserved |
| 21h | DigBeep | Digital PC Beep |
| 22h | Vendor Reserved | Vendor Reserved |

Table 23. High Definition Audio Widget

8. WIDGETS

8.1. Reset Key

| Abbreviation | Description |
|--------------|--|
| POR | Power On Reset. |
| SAFG | Single AFG Reset - One single write to the Reset Verb in the AFG Node. |
| DAFG | Double AFG Reset - Two consecutive Single AFG Resets with only idle frames (if any) and no Link Resets between. |
| S&DAFG | Single And Double AFG Reset - Either one will cause reset. |
| LR | Link Reset - Level sensitive reset anytime the HDA Reset is set low. |
| ELR | Exiting Link Reset - Edge sensitive reset any time the HDA Reset transitions from low to high. |
| ULR | Unexpected Link Reset - Level sensitive reset anytime the HDA Reset is set low when the ClkStopOK indicator is currently set to 0. |
| PS | Power State Change - Reset anytime the Actual Power State changes for the Widget in question. |

8.2. Root (NID = 00h): VendorID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------|-----|-----------|-------|
| Vendor | 31:16 | R | 111Dh | N/A |
| | Vendor ID. | | | |
| DeviceFix | 15:8 | R | see below | N/A |
| | Device ID. | | | |
| DeviceProg | 7:0 | R | see below | N/A |
| | Device ID. | | | |

| Device | 92HD87B1 | 92HD87B2 | 92HD87B3 | 92HD87B4 |
|-----------|----------|----------|----------|----------|
| Device ID | 76D1h | 76D9 | 76D1h | 76D9h |

8.2.1. Root (NID = 00h): RevID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Major | 23:20 | R | 1h | N/A (Hard-coded) |
| | Major rev number of compliant HD Audio spec. | | | |
| Minor | 19:16 | R | 0h | N/A (Hard-coded) |
| | Minor rev number of compliant HD Audio spec. | | | |
| RevisionFix | 15:12 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| RevisionProg | 11:8 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| SteppingFix | 7:4 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |
| SteppingProg | 3:0 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |

8.2.2. Root (NID = 00h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| StartNID | 23:16 | R | 01h | N/A (Hard-coded) |
| | Starting node number (NID) of first function group | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 01h | N/A (Hard-coded) |
| | Total number of nodes | | | |

8.3. AFG (NID = 01h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StartNID | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Starting node number for function group subordinate nodes. | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 19h | N/A (Hard-coded) |
| | Total number of nodes. | | | |

8.3.1. AFG (NID = 01h): FGType

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:9 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| UnSol | 8 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response supported: 1 = yes, 0 = no. | | | |
| NodeType | 7:0 | R | 1h | N/A (Hard-coded) |
| | Function group type: 00h = Reserved 01h = Audio Function Group 02h = Vendor Defined Modem Function Group 03h-7Fh = Reserved 80h-FFh = Vendor Defined Function Group | | | |

8.3.2. AFG (NID = 01h): AFGCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0008h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd3 | 31:17 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| BeepGen | 16 | R | 1h | N/A (Hard-coded) |
| | Beep generator present: 1 = yes, 0 = no. | | | |
| Rsvd2 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| InputDelay | 11:8 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link. | | | |
| Rsvd1 | 7:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| OutputDelay | 3:0 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin. | | | |

8.3.3. AFG (NID = 01h): PCMCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

8.3.4. AFG (NID = 01h): StreamCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 0h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

8.3.5. AFG (NID = 01h): InAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 0h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 27h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.3.6. AFG (NID = 01h): PwrStateCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Fh | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| EPSS | 31 | R | 1h | N/A (Hard-coded) |
| | Extended power states support: 1 = yes, 0 = no. | | | |
| ClkStop | 30 | R | 1h | N/A (Hard-coded) |
| | D3 clock stop support: 1 = yes, 0 = no. | | | |
| S3D3ColdSup | 29 | R | 1h | N/A (Hard-coded) |
| | Codec state intended during system S3 state: 1 = D3Hot, 0 = D3Cold. On YB revs & prior, this was called LPD3Sup & default was 0h | | | |
| Rsvd | 28:5 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| D3ColdSup | 4 | R | 1h | N/A (Hard-coded) |
| | D3Cold power state support: 1 = yes, 0 = no. | | | |
| D3Sup | 3 | R | 1h | N/A (Hard-coded) |
| | D3 power state support: 1 = yes, 0 = no. | | | |
| D2Sup | 2 | R | 1h | N/A (Hard-coded) |
| | D2 power state support: 1 = yes, 0 = no. | | | |
| D1Sup | 1 | R | 1h | N/A (Hard-coded) |
| | D1 power state support: 1 = yes, 0 = no. | | | |
| D0Sup | 0 | R | 1h | N/A (Hard-coded) |
| | D0 power state support: 1 = yes, 0 = no. | | | |

8.3.7. AFG (NID = 01h): GPIOCnt

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0011h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| GPIWake | 31 | R | 1h | N/A (Hard-coded) |
| | Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin. | | | |
| GPIUnsol | 30 | R | 1h | N/A (Hard-coded) |
| | GPIO unsolicited response support: 1 = yes, 0 = no. | | | |
| Rsvd | 29:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumGPIs | 23:16 | R | 00h | N/A (Hard-coded) |
| | Number of GPI pins supported by function group. | | | |
| NumGPOs | 15:8 | R | 00h | N/A (Hard-coded) |
| | Number of GPO pins supported by function group. | | | |
| NumGPIOs | 7:0 | R | 03h | N/A (Hard-coded) |
| | Number of GPIO pins supported by function group. | | | |

8.3.8. AFG (NID = 01h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 02h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 7Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 7Fh | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.3.9. AFG (NID = 01h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd3 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Function Group have been reset. Cleared by PwrState 'Get' to this Widget. | | | |
| ClkStopOK | 9 | R | 1h | POR - DAFG - ULR |
| | Bit clock can currently be removed: 1 = yes, 0 = no. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 6:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 2:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.3.10. AFG (NID = 01h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.3.11. AFG (NID = 01h): GPIO

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 715h |
| Get | F1500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Data2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |

8.3.12. AFG (NID = 01h): GPIOEn

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 716h |
| Get | F1600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |

8.3.13. AFG (NID = 01h): GPIODir

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 717h |
| Get | F1700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Control2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |

8.3.14. AFG (NID = 01h): GPIOWakeEn

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 718h |
| Get | F1800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| W2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| W1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |

8.3.15. AFG (NID = 01h): GPIOUnsol

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 719h |
| Get | F1900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EnMask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state. | | | |
| EnMask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state. | | | |

8.3.16. AFG (NID = 01h): GPIOSticky

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 71Ah |

8.3.16. AFG (NID = 01h): GPIOSticky

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Get | F1A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |

8.3.17. AFG (NID = 01h): SubID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 723h | 722h | 721h | 720h |
| Get | F2300h / F2200h / F2100h / F2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|-------|
| Subsys3 | 31:24 | RW | 00h | POR |
| | Subsystem ID (byte 3) | | | |
| Subsys2 | 23:16 | RW | 00h | POR |
| | Subsystem ID (byte 2) | | | |
| Subsys1 | 15:8 | RW | 01h | POR |
| | Subsystem ID (byte 1) | | | |
| Assembly | 7:0 | RW | 00h | POR |
| | Assembly ID (Not applicable to codec vendors). | | | |

8.3.18. AFG (NID = 01h): GPIOIrty

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 770h |
| Get | F7000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| GP2 | 2 | RW | 1h | POR - DAFG - ULR |
| | GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |
| GP1 | 1 | RW | 1h | POR - DAFG - ULR |
| | GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |
| GP0 | 0 | RW | 1h | POR - DAFG - ULR |
| | GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |

8.3.19. AFG (NID = 01h): GPIODrive

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 771h |
| Get | F7100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OD2 | 2 | RW | 0h | POR - DAFG - ULR |
| | GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD1 | 1 | RW | 0h | POR - DAFG - ULR |
| | GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD0 | 0 | RW | 0h | POR - DAFG - ULR |
| | GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0, float for 1). | | | |

8.3.20. AFG (NID = 01h): DMic

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 778h |
| Get | F7800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|----------|------------------|
| Rsvd | 31:5 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mono0 | 4 | RW | 0h | POR |
| | DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel). | | | |
| PhAdj | 3:2 | RW | 0h | POR |
| | Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge 1h = left data center of high/right data center of low 2h = left data falling edge/right data rising edge 3h = left data center of low/right data center of high | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------|
| Rate | 1:0 | RW | 2h | POR |
| Selects the DMic clock rate: 0h = 4.704MHz 1h = 3.528MHz 2h = 2.352MHz 3h = 1.176MHz. | | | | |

8.3.21. AFG (NID = 01h): DACMode

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 780h |
| Get | F8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| SDMSettleDisable | 7 | RW | 0h | POR - S&DAFG - LR |
| SDM wait-to-settle disable: 1 = at mute, the SDM switches to the mute pattern immediately 0 = at mute, the SDM switches to the mute pattern after settling (can take up to ~45ms) | | | | |
| SDMCoeffSel | 6 | RW | 0h | POR - S&DAFG - LR |
| DAC SDM coefficient select (stages 1, 2, 3): 1 = 1/16, 1/2, 1/4 0 = 1/16, 1/4, 1/2 | | | | |
| SDMLFHalf | 5 | RW | 0h | POR - S&DAFG - LR |
| DAC SDM local feedback coefficient select: 1 = 1/4096, 0 = 1/2048. | | | | |
| SDMLFDisable | 4 | RW | 0h | POR - S&DAFG - LR |
| DAC SDM local feedback disable: 1 = local feedback disabled, 0 = local feedback enabled. | | | | |
| InvertValid | 3 | RW | 0h | POR - S&DAFG - LR |
| DAC Valid Invert: 1 = 7.056MHz valid strobe is inverted, 0 = 7.056MHz valid strobe is not inverted. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-----------------|--|-----|---------|-------------------|
| InvertData | 2 | RW | 0h | POR - S&DAFG - LR |
| | DAC Data Invert: 1 = 1-bit outputs are inverted, 0 = 1-bit outputs are not inverted. | | | |
| Atten6dBDisable | 1 | RW | 0h | POR - S&DAFG - LR |
| | Disable built-in -6dB digital attenuation: 1 = -6dB disabled, 0 = -6dB enabled. | | | |
| Fade | 0 | RW | 1h | POR - S&DAFG - LR |
| | DAC Gain Fade Enable: 1 = gain will be slowly faded from old value to new value (~10ms) 0 = gain will jump immediately to new value. | | | |

8.3.22. AFG (NID = 01h): ADCMode

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 784h |
| Get | F8400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|----------|-------------------|
| Rsvd2 | 31:4 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| InvertValid | 3 | RW | 0h | POR - S&DAFG - LR |
| | ADC Valid Invert: 1 = 14.112MHz valid strobe is inverted, 0 = 14.112MHz valid strobe is not inverted. | | | |
| InvertData | 2 | RW | 0h | POR - S&DAFG - LR |
| | ADC Data Invert: 1 = 1-bit inputs are inverted, 0 = 1-bit inputs are not inverted. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.3.23. AFG (NID = 01h): EAPD

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 788h |
| Get | F8800h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd4 | 31:15 | R | 00000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPBSDInv | 14 | RW | 0h | POR |
| | HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| HPBSDMode | 13 | RW | 1h | POR |
| | HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| HPBSD | 12 | RW | 0h | POR |
| | HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd3 | 11 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPASDInv | 10 | RW | 0h | POR |
| | HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| HPASDMode | 9 | RW | 1h | POR |
| | HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| HPASD | 8 | RW | 0h | POR |
| | HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BTLSDInv | 6 | RW | 0h | POR |
| | BTL Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| BTLSDMode | 5 | RW | 1h | POR |
| | BTL Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| BTLSD | 4 | RW | 0h | POR |
| | BTL Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| PinMode | 1:0 | RW | 0h | POR |
| | EAPD Pin Mode: 00b = Open Drain I/O (Value at pin is wired-AND of EAPD bit and external signal) 01b = CMOS Output (Value of EAPD bit is forced at pin) 1xb = CMOS Input (External signal controls internal amps, EAPD bit ignored) | | | |

8.3.24. AFG (NID = 01h): PortUse

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7C0h |
| Get | FC000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|----------|------------------|
| Rsvd | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mono | 6 | RW | 1h | POR |
| | Mono usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |
| PortF | 5 | RW | 1h | POR |
| | Port F usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|-------|
| PortE | 4 | RW | 1h | POR |
| | Port E usage: 0 = connected as an output, 1 = either not connected or connected as an input. Port E not supported. | | | |
| PortD | 3 | RW | 1h | POR |
| | Port D usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |
| PortC | 2 | RW | 1h | POR |
| | Port C usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |
| PortB | 1 | RW | 1h | POR |
| | Port B usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |
| PortA | 0 | RW | 1h | POR |
| | Port A usage: 0 = connected as an output, 1 = either not connected or connected as an input. | | | |

8.3.25. AFG (NID = 01h): VSPwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7D8h |
| Get | FD800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| D5 | 1 | RW | 0h | POR - ELR |
| | Vendor specific D5 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If set, this bit overrides the D4 bit (bit 0). Includes the power savings of D4, but additionally powers down GPIO pins, the VAG amp, and the HP amps. Exits this power state via POR or rising edge of Link Reset. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-----------|
| D4 | 0 | RW | 0h | POR - ELR |
| Vendor specific D4 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If the D5 bit (bit 1) is set, this bit is overridden. Includes the power savings of D3cold, but additionally powers down the HDA interface (no responses). Exit this power state via POR or rising edge of Link Reset. | | | | |

8.3.26. AFG (NID = 01h): AnaPort

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | 7EDh | 7ECh |
| Get | FEC00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|----------|--------------------|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| MonoPwd | 6 | RW | 0h | POR - S&DAFG - ULR |
| Power down Mono Output. | | | | |
| FPwd | 5 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port F. | | | | |
| EPwd | 4 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port E. Port E not supported. | | | | |
| DPwd | 3 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port D. | | | | |
| CPwd | 2 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port C. | | | | |
| BPwd | 1 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port B. | | | | |
| APwd | 0 | RW | 0h | POR - S&DAFG - ULR |
| Power down Port A. | | | | |

8.3.27. AFG (NID = 01h): AnaBeep

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7EEh |
| Get | FEE00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:3 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 2:1 | RW | 3h | POR - DAFG - ELR |
| | Analog PC Beep Gain: 0h = -24dB, 1h = -18dB, 2h = -12dB, 3h = -6dB. | | | |
| Enable | 0 | RW | 0h | POR - DAFG - ELR |
| | Analog PC Beep Enable: 1 = Analog PC beep enabled, 0 = Analog PC beep disabled. | | | |

8.3.28. AFG (NID = 01h): AnaBTL

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | 7F6h | 7F5h | 7F4h |
| Get | FF400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|--|-----|---------|------------------|
| Rsvd3 | 31 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| TSTripHighStatus | 30 | R | 0h | POR |
| | Temp sense high trip point status | | | |
| TSTripLowStatus | 29 | R | 0h | POR |
| | Temp sense low trip point status | | | |
| TSVolStatus | 28:24 | R | 00h | POR |
| | Temp sense volume status for the BTL amplifier: 00000b..11111b = Range specificity for MaxVol field. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|--------------------|------------------|
| TSMuteStatus | 23 | R | 0h | POR |
| | Temp sense forced mute status for the BTL amplifier. | | | |
| TSPwdStatus | 22 | R | 0h | POR |
| | Temp sense forced powerdown status for the BTL amplifier. | | | |
| Rsvd2 | 21 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| TSOverrideReset | 20 | RW | 0h | POR |
| | Override reset for the BTL amplifier temperature sensing circuit: set to 1 to recalculate, set back to 0 to latch the value. | | | |
| TSOverrideSel | 19 | RW | 0h | POR |
| | Override select for the BTL amplifier volume. Use MaxVol[4:0] and TSOverrideReset directly to drive analog | | | |
| TSTestMode | 18 | RW | 0h | POR |
| | Temp sense test mode select, 0=normal operation, 1=sensor will trip at ambient temperature. | | | |
| TSForcePwd | 17 | RW | 0h (UA) 1h (TA) | POR |
| | Temp sense force powerdown select 0=BTL will not be muted and powered down even if it is still overheating when the volume is 0h 1=BTL will be muted and powered down even if it is still overheating when the volume is 0h | | | |
| TSInstantCutMode | 16 | RW | 0h | POR |
| | Temp sense instant cut mode 0=Two trip points used to smoothly adjust the volume 1=One single trip point used to set volume to wither 0 or max value (TI mode) | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| TSWait | 15:12 | RW | 3h | POR |
| | Temperature sensing wait time between volume increments 0h = 2ms (polling at 2ms) 1h = 4ms (polling at 4ms) 2h = 8ms (polling at 8ms) 3h = 16ms (polling at 16ms) 4h = 32ms (polling at 16ms) 5h = 64ms (polling at 16ms) 6h = 128ms (polling at 16ms) 7h = 256ms (polling at 16ms) 8h = 512ms (polling at 16ms) 9h = 1.024s (polling at 16ms) Ah = 2.048s (polling at 16ms) Bh = 4.096s (polling at 16ms) Ch = 8.192s (polling at 16ms) Dh = 16.384s (polling at 16ms) Eh = 32.768s (polling at 16ms) Fh = 65.536s (polling at 16ms). | | | |
| TSTripSplit | 11:10 | RW | 0h | POR |
| | Temp sense split setting, determines how many degrees above the low point the high point is set: 0h = 15 Degrees C 1h = 30 Degrees C 2h = 45 Degrees C 3h = 60 Degrees C. | | | |
| TSTripShift | 9:8 | RW | 02h | POR |
| | Temp sense shift setting, determines where the low point is set: 0h = 110 Degrees C 1h = 125 Degrees C 2h = 140 Degrees C 3h = 155 Degrees C | | | |
| Rsvd1 | 7:6 | R | 0h | NA |
| | Reserved | | | |
| MonoSel | 5 | RW | 0h' | POR |
| | Mono select for the BTL amplifier, 1=mono, 0=stereo | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|-------|
| MaxVol | 4:0 | RW | 0Fh | POR |
| Gain setting for the BTL amplifier (temperature sensing logic will decrement from here): 00000 = -26.25dB: 00001 = -19.80dB 00010 = -15.80dB 00011 = -12.85dB 00100 = -10.40dB 00101 = -8.27dB 00110 = -6.35dB 00111 = -4.60dB 01000 = -2.90dB 01001 = -1.25dB 01010 = 0.35dB 01011 = 1.98dB 01100 = 3.63dB 01101 = 5.35dB 01110 = 7.19dB 01111 = 9.18dB 10000 = 9.95dB 10001 = 10.75dB 10010 = 11.58dB 10011 = 12.48dB 10100 = 13.43dB 10101 = 14.46dB 10110 = 15.57dB 10111 = 16.79dB 11000-11111 = Not valid | | | | |

8.3.29. AFG (NID = 01h): AnaCapless

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | 7FAh | 7F9h | 7F8h |
| Get | FF800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|------------------|
| Rsvd | 31:26 | R | 00h | N/A (Hard-coded) |
| Reserved. | | | | |
| VRegSCDet | 25 | R | 0h | POR |
| Capless regulator short circuit detect indicator. | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------------------|--|-----|----------------------------|-------------------|
| ChargePumpSCDet | 24 | R | 0h | POR |
| | Capless charge pump short circuit detect indicator. | | | |
| VRegSel | 23:20 | RW | 3h | POR - S&DAFG - LR |
| | Capless regulator output voltage multiply ratio. | | | |
| VRegSCRstB | 19 | RW | 0h | POR - S&DAFG - LR |
| | Capless regulator short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| VRegGndShort | 18 | RW | 0h | POR - S&DAFG - LR |
| | Ground the capless regulator output. | | | |
| VRegPwd | 17 | RW | 0h | POR - S&DAFG - LR |
| | Capless regulator powerdown. | | | |
| ChargePumpSCRstB | 16 | RW | 0h | POR - S&DAFG - LR |
| | Capless charge pump short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| ChargePumpHiZ | 15 | RW | 0h | POR - S&DAFG - LR |
| | Hi-Z the capless charge pump outputs. | | | |
| ChargePumpPwd | 14 | RW | 0h | POR - S&DAFG - LR |
| | Capless charge pump powerdown. | | | |
| ChargePumpSplyDetOverride | 13 | RW | 1h (YA rev) 0h | POR - S&DAFG - LR |
| | Capless charge pump supply detect override. | | | |
| ChargePumpFreqBypass | 12 | RW | 1h (YA, YC) 0h (YB rev) | POR - S&DAFG - LR |
| | Capless charge pump frequency reg bypass. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------------|---|-----|---------|-------------------|
| ChargePumpClkRate | 11:8 | RW | 8h | POR |
| | Capless charge pump clock rate: 0000b = 800.0kHz (24MHz/30) 0001b = 750.0kHz (24MHz/32) 0010b = 706.9kHz (24MHz/34) 0011b = 666.7kHz (24MHz/36) 0100b = 631.6kHz (24MHz/38) 0101b = 600.0kHz (24MHz/40) 0110b = 571.4kHz (24MHz/42) 0111b = 545.5kHz (24MHz/44) 1000b = 800.0kHz (24MHz/30) 1001b = 857.1kHz (24MHz/28) 1010b = 923.1kHz (24MHz/26) 1011b = 1.000MHz (24MHz/24) 1100b = 1.091MHz (24MHz/22) 1101b = 1.200MHz (24MHz/20) 1110b = 1.333MHz (24MHz/18) 1111b = 1.500MHz (24MHz/16) | | | |
| ChargePumpClkDiv | 7:5 | RW | 4h | POR |
| | Capless charge pump analog clock divider: 001b = No divide 010b = Divide by 2, 50% duty cycle 100b = Divide by 4, 50% duty cycle 110b = Divide by 2, 75% duty cycle 011b = Divide by 4, 75% duty cycle 111b = Divide by 4, 87.5% duty cycle Other values undefined | | | |
| ChargePumpClkSel | 4 | RW | 0h | POR |
| | Capless charge pump clock select: 0 = ring oscillator, 1 = charge pump clock defined by AFGCaplessChargePumpClkRate[3:0] field below. | | | |
| PadGnd | 3 | RW | 0h | POR - S&DAFG - LR |
| | Ground the output pad of the capless amplifiers. | | | |
| InputGnd | 2 | RW | 0h | POR - S&DAFG - LR |
| | Ground the input to the capless output amplifiers. | | | |
| Reserved | 1 | R | 0h | POR |
| | Reserved | | | |
| AntiPopBypass | 0 | RW | 0h | POR |
| | Anti-Pop bypass.. | | | |

8.3.30. AFG (NID = 01h): Reset

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7FFh |
| Get | FFF00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd1 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Execute | 7:0 | W | 00h | N/A (Hard-coded) |
| | Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The codec should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response. | | | |

8.3.31. AFG (NID = 01h): AuxAudio

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 774h |
| Get | F7400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| MixerPwD | 1 | RW | 0h | POR |
| | Aux Audio Moder mixer powerdown: 0 = Mixer enabled during Aux Audio Mode, 1 = Mixer forced powered down during Aux Audio Mode. | | | |
| Enable | 0 | RW | 1h | POR |
| | Aux Audio Mode select: 0 = Aux Audio disabled, 1 = Aux Audio enabled during HDA Link Reset. | | | |

8.4. PortA (NID = 0Ah): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.4.1. PortA (NID = 0Ah): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

8.4.2. PortA (NID = 0Ah): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.4.3. PortA (NID = 0Ah): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

8.4.4. PortA (NID = 0Ah): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.4.5. PortA (NID = 0Ah): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.4.6. PortA (NID = 0Ah): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.4.7. PortA (NID = 0Ah): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.4.8. PortA (NID = 0Ah): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved | | | |

8.4.9. PortA (NID = 0Ah): UnsoIResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.4.10. PortA (NID = 0Ah): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

8.4.11. PortA (NID = 0Ah): EAPDBTLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.4.12. PortA (NID = 0Ah): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 02h | POR |
| | Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 2h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 4h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 3h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Fh | POR |
| | Sequence. | | | |

8.5. PortB (NID = 0Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.5.1. PortB (NID = 0Bh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| EAPD support: 1 = yes, 0 = no. | | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| Balanced I/O support: 1 = yes, 0 = no. | | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| Input support: 1 = yes, 0 = no. | | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| Output support: 1 = yes, 0 = no. | | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| Headphone amp present: 1 = yes, 0 = no. | | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| Presence detection support: 1 = yes, 0 = no. | | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| Trigger required for impedance sense: 1 = yes, 0 = no. | | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| Impedance sense support: 1 = yes, 0 = no. | | | | |

8.5.2. PortB (NID = 0Bh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

8.5.3. PortB (NID = 0Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

8.5.4. PortB (NID = 0Bh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.5.5. PortB (NID = 0Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.5.6. PortB (NID = 0Bh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 5:0 | RW | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

8.5.7. PortB (NID = 0Bh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.5.8. PortB (NID = 0Bh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

8.5.9. PortB (NID = 0Bh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.5.10. PortB (NID = 0Bh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 02h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |
| Device | 23:20 | RW | 2h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|----------------|---|-----|---------|-------|
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | |
| Color | 15:12 | RW | 1h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 1h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

8.6. PortC (NID = 0Ch): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.6.1. PortC (NID = 0Ch): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

8.6.2. PortC (NID = 0Ch): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.6.3. PortC (NID = 0Ch): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

8.6.4. PortC (NID = 0Ch): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.6.5. PortC (NID = 0Ch): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.6.6. PortC (NID = 0Ch): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.6.7. PortC (NID = 0Ch): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.6.8. PortC (NID = 0Ch): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved | | | |

8.6.9. PortC (NID = 0Ch): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.6.10. PortC (NID = 0Ch): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

8.6.11. PortC (NID = 0Ch): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------|-----|---------|------------------|
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

8.6.12. PortC (NID = 0Ch): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 02h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

92HD87**SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO**

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | Ah | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 9h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 2h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

8.7. PortD (NID = 0Dh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.7.1. PortD (NID = 0Dh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| EAPD support: 1 = yes, 0 = no. | | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| BalancedIO | 6 | R | 1h | N/A (Hard-coded) |
| Balanced I/O support: 1 = yes, 0 = no. | | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| Input support: 1 = yes, 0 = no. | | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| Output support: 1 = yes, 0 = no. | | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| Headphone amp present: 1 = yes, 0 = no. | | | | |
| PresDtctCap | 2 | R | 0h | N/A (Hard-coded) |
| Presence detection support: 1 = yes, 0 = no. | | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| Trigger required for impedance sense: 1 = yes, 0 = no. | | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| Impedance sense support: 1 = yes, 0 = no. | | | | |

8.7.2. PortD (NID = 0Dh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

8.7.3. PortD (NID = 0Dh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

8.7.4. PortD (NID = 0Dh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.7.5. PortD (NID = 0Dh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.7.6. PortD (NID = 0Dh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd1 | 5:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.7.7. PortD (NID = 0Dh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.7.8. PortD (NID = 0Dh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 2h | POR |
| | Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|-------|
| Location | 29:24 | RW | 10h | POR |
| | Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | 1h | POR |
| | Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|----------------|---|-----|---------|-------|
| ConnectionType | 19:16 | RW | 7h | POR |
| | Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | |
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 3h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

8.8. Vendor Reserved (NID = 0Eh)

8.9. PortF (NID = 0Fh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.9.1. PortF (NID = 0Fh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

8.9.2. PortF (NID = 0Fh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.9.3. PortF (NID = 0Fh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

8.9.4. PortF (NID = 0Fh): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.9.5. PortF (NID = 0Fh): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.9.6. PortF (NID = 0Fh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.9.7. PortF (NID = 0Fh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.9.8. PortF (NID = 0Fh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved | | | |

8.9.9. PortF (NID = 0Fh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.9.10. PortF (NID = 0Fh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

8.9.11. PortF (NID = 0Fh): EAPDBTLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------|-----|---------|------------------|
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

8.9.12. PortF (NID = 0Fh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 01h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 8h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 9h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 4h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

8.10. Vendor Reserved (NID = 10h)

8.11. DMic0 (NID = 11h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnsolCap | 7 | R | 1h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.11.1. DMic0 (NID = 11h): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| EAPD support: 1 = yes, 0 = no. | | | | |
| VRefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| Balanced I/O support: 1 = yes, 0 = no. | | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| Input support: 1 = yes, 0 = no. | | | | |
| OutCap | 4 | R | 0h | N/A (Hard-coded) |
| Output support: 1 = yes, 0 = no. | | | | |
| HPhnDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| Headphone amp present: 1 = yes, 0 = no. | | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| Presence detection support: 1 = yes, 0 = no. | | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| Trigger required for impedance sense: 1 = yes, 0 = no. | | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| Impedance sense support: 1 = yes, 0 = no. | | | | |

8.11.2. DMic0 (NID = 11h): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | | |

8.11.3. DMic0 (NID = 11h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |

8.11.3. DMic0 (NID = 11h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.11.4. DMic0 (NID = 11h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.11.5. DMic0 (NID = 11h): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|----------|------------------|
| Rsvd2 | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

8.11.6. DMic0 (NID = 11h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

8.11.7. DMic0 (NID = 11h): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

8.11.8. DMic0 (NID = 11h): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 2h | POR |
| | Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|-------|
| Location | 29:24 | RW | 10h | POR |
| | Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | Ah | POR |
| | Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | |

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| Field Name | Bits | R/W | Default | Reset |
|----------------|---|-----|---------|-------|
| ConnectionType | 19:16 | RW | 3h | POR |
| | Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | |
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 4h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Eh | POR |
| | Sequence. | | | |

8.12. Reserved (NID = 12h)

8.13. DAC0 (NID = 13h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.13.1. DAC0 (NID = 13h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

8.13.2. DAC0 (NID = 13h): ProcState (RA revision only)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:2 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| DACHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the DAC HPF ("off"), 01b-11b= DAC HPF is enabled ("on" or "benign"). | | | |

8.13.3. DAC0 (NID = 13h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.13.4. DAC0 (NID = 13h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| Amp mute: 1 = muted, 0 = not muted. | | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | | |

8.13.5. DAC0 (NID = 13h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| Actual power state of this widget. | | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| Current power state setting for this widget. | | | | |

8.13.6. DAC0 (NID = 13h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

8.13.7. DAC0 (NID = 13h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.13.8. DAC0 (NID = 13h): ProclIndex (RA revision only)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 782h |
| Get | F8200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:3 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| CoeffIndex | 2:0 | RW | 2h | POR - DAFG - ULR |
| | Processing Coeff selection. 0 = -3db response at 100Hz 1 = -3db response at 200Hz 2 = -3db response at 300Hz 3 = -3db response at 400Hz 4 = -3db response at 500Hz 5 = -3db response at 750Hz 6 = -3db response at 1000Hz 7 = -3db response at 2000Hz | | | |

8.14. DAC1 (NID = 14h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.14.1. DAC1 (NID = 14h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| Stream type: 1 = Non-PCM, 0 = PCM. | | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| SmpIRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpI | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

8.14.2. DAC1 (NID = 14h): ProcState (RA revision only)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:2 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| DACHPFByP | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the DAC HPF ("off"), 01b-11b= DAC HPF is enabled ("on" or "benign"). | | | |

8.14.3. DAC1 (NID = 14h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.14.4. DAC1 (NID = 14h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.14.5. DAC1 (NID = 14h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |

8.14.5. DAC1 (NID = 14h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.14.6. DAC1 (NID = 14h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

8.14.7. DAC1 (NID = 14h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.14.8. DAC1 (NID = 14h): ProclIndex (RA revision only)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 782h |
| Get | F8200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:3 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| CoeffIndex | 2:0 | RW | 2h | POR - DAFG - ULR |
| | Processing Coeff selection. 0 = -3db response at 100Hz 1 = -3db response at 200Hz 2 = -3db response at 300Hz 3 = -3db response at 400Hz 4 = -3db response at 500Hz 5 = -3db response at 750Hz 6 = -3db response at 1000Hz 7 = -3db response at 2000Hz | | | |

8.15. DAC2 (NID = 22h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | Fh | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 0h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrD | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrD | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 0h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.15.1. DAC2 (NID = 22h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | R | 0h | N/A (Hard-coded) |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMltp | 13:11 | R | 0h | N/A (Hard-coded) |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | R | 0h | N/A (Hard-coded) |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| BitsPerSmpl | 6:4 | R | 0h | N/A (Hard-coded) |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | R | 0h | N/A (Hard-coded) |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

8.15.2. DAC2 (NID = 22h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | R | 0h | N/A (Hard-coded) |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | R | 00h | N/A (Hard-coded) |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.15.3. DAC2 (NID = 22h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | R | 0h | N/A (Hard-coded) |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | R | 00h | N/A (Hard-coded) |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.15.4. DAC2 (NID = 22h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 0h | N/A (Hard-coded) |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | N/A (Hard-coded) |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 0h | N/A (Hard-coded) |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| Set | 1:0 | R | 0h | N/A (Hard-coded) |
| Current power state setting for this widget. | | | | |

8.15.5. DAC2 (NID = 22h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Strm | 7:4 | R | 0h | N/A (Hard-coded) |
| Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | | |
| Ch | 3:0 | R | 0h | N/A (Hard-coded) |
| Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | | |

8.15.6. DAC2 (NID = 22h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapEn | 2 | R | 0h | N/A (Hard-coded) |
| Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

8.16. ADC0 (NID = 15h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.16.1. ADC0 (NID = 15h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.16.2. ADC0 (NID = 15h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 17h | N/A (Hard-coded) |
| | ADC0Mux Selector widget (0x18) | | | |

8.16.3. ADC0 (NID = 15h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

8.16.4. ADC0 (NID = 15h): ProcState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

8.16.5. ADC0 (NID = 15h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.16.6. ADC0 (NID = 15h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

8.17. ADC1 (NID = 16h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.17.1. ADC1 (NID = 16h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

8.17.2. ADC1 (NID = 16h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 18h | N/A (Hard-coded) |
| | ADC1Mux widget (0x18) | | | |

8.17.3. ADC1 (NID = 16h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| SmpIRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

8.17.4. ADC1 (NID = 16h): ProcState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

8.17.5. ADC1 (NID = 16h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.17.6. ADC1 (NID = 16h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

8.18. ADC0Mux (NID = 17h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.18.1. ADC0Mux (NID = 17h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 07h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.18.2. ADC0Mux (NID = 17h): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) in TB silicon Unused list entry in RA silicon. | | | |
| ConL5 | 15:8 | R | 12h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL4 | 7:0 | R | 11h | N/A (Hard-coded) |
| | DMic0 Pin widget (0x11) in TB silicon Port A Pin widget (0x0A) in RA silicon | | | |

8.18.3. ADC0Mux (NID = 17h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL3 | 31:24 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) in TB silicon DMic0 Pin widget (0x11) in RA silicon | | | |
| ConL2 | 23:16 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) in TB silicon Mixer Summing widget (0x1B) in RA silicon | | | |
| ConL1 | 15:8 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E) (Port E not available) in TB silicon Port F Pin widget (0x0F) in RA silicon | | | |
| ConL0 | 7:0 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C) in TB and RA silicon | | | |

8.18.4. ADC0Mux (NID = 17h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 0Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.18.5. ADC0Mux (NID = 17h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 3:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.18.6. ADC0Mux (NID = 17h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 3:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.18.7. ADC0Mux (NID = 17h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.18.8. ADC0Mux (NID = 17h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.18.9. ADC0Mux (NID = 17h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.19. ADC1Mux (NID = 18h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvr | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.19.1. ADC1Mux (NID = 18h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 07h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.19.2. ADC1Mux (NID = 18h): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) in TB silicon Unused list entry in RA silicon. | | | |
| ConL5 | 15:8 | R | 12h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL4 | 7:0 | R | 11h | N/A (Hard-coded) |
| | DMic0 Pin widget (0x11) in TB silicon Port A Pin widget (0x0A) in RA silicon | | | |

8.19.3. ADC1Mux (NID = 18h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL3 | 31:24 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) in TB silicon DMic0 Pin widget (0x11) in RA silicon | | | |
| ConL2 | 23:16 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) in TB silicon Mixer Summing widget (0x1B) in RA silicon | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL1 | 15:8 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E) (Port E not available) in TB silicon Port F Pin widget (0x0F) in RA silicon | | | |
| ConL0 | 7:0 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C) in TB and RA silicon | | | |

8.19.4. ADC1Mux (NID = 18h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 0Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.19.5. ADC1Mux (NID = 18h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 3:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.19.6. ADC1Mux (NID = 18h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 3:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.19.7. ADC1Mux (NID = 18h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

8.19.8. ADC1Mux (NID = 18h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.19.9. ADC1Mux (NID = 18h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

8.20. Reserved (NID = 19h)

8.21. Reserved (NID = 1Ah)

8.22. Mixer (NID = 1Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 2h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

8.22.1. Mixer (NID = 1Bh): InAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| Mute support: 1 = yes, 0 = no. | | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| Reserved. | | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| Number of gains steps (number of possible settings - 1). | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| Offset | 6:0 | R | 17h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.22.2. Mixer (NID = 1Bh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 06h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.22.3. Mixer (NID = 1Bh): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL5 | 15:8 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A). Uses InAmpLeft5/InAmpRight5 controls TB silicon Unused list entry in RA silicon | | | |
| ConL4 | 7:0 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14). Uses InAmpLeft4/InAmpRight4 controls in TB silicon Port A Pin widget (0x0A). Uses InAmpLeft4/InAmpRight4 controls RA silicon | | | |

8.22.4. Mixer (NID = 1Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| ConL3 | 31:24 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13). Uses InAmpLeft3/InAmpRight3 controls in TB silicon DAC1 Converter widget (0x14). Uses InAmpLeft3/InAmpRight3 controls in RA silicon | | | |
| ConL2 | 23:16 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F). Uses InAmpLeft2/InAmpRight2 controls in TB silicon DAC0 Converter widget (0x13). Uses InAmpLeft2/InAmpRight2 controls in RA silicon | | | |
| ConL1 | 15:8 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E). Uses InAmpLeft1/InAmpRight1 controls. (Port E not supported). TB silicon Port F Pin widget (0x0F). Uses InAmpLeft1/InAmpRight1 controls in RA silicon | | | |
| ConL0 | 7:0 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C). Uses InAmpLeft0/InAmpRight0 controls in TB and RA silicon | | | |

8.22.5. Mixer (NID = 1Bh): InAmpLeft0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |

8.22.5. Mixer (NID = 1Bh): InAmpLeft0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.6. Mixer (NID = 1Bh): InAmpRight0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.7. Mixer (NID = 1Bh): InAmpLeft1

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 361h |
| Get | B2001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.8. Mixer (NID = 1Bh): InAmpRight1

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 351h |
| Get | B0001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.9. Mixer (NID = 1Bh): InAmpLeft2

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 362h |
| Get | B2002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.10. Mixer (NID = 1Bh): InAmpRight2

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 352h |
| Get | B0002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.11. Mixer (NID = 1Bh): InAmpLeft3

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 363h |
| Get | B2003h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.12. Mixer (NID = 1Bh): InAmpRight3

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 353h |
| Get | B0003h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.13. Mixer (NID = 1Bh): InAmpLeft4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 364h |
| Get | B2004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.14. Mixer (NID = 1Bh): InAmpRight4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 354h |
| Get | B0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.15. Mixer (NID = 1Bh): InAmpLeft5

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 365h |
| Get | B2005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.16. Mixer (NID = 1Bh): InAmpRight5

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 355h |
| Get | B0005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

8.22.17. Mixer (NID = 1Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.23. MixerOutVol (NID = 1Ch): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

92HD87

SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

8.23.1. MixerOutVol (NID = 1Ch): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

8.23.2. MixerOutVol (NID = 1Ch): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

8.23.3. MixerOutVol (NID = 1Ch): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| Offset | 6:0 | R | 1Fh | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.23.4. MixerOutVol (NID = 1Ch): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.23.5. MixerOutVol (NID = 1Ch): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.23.6. MixerOutVol (NID = 1Ch): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.24. Reserved (NID = 1Dh)

8.25. Reserved (NID = 1Eh)

8.26. Reserved (NID = 1Fh)

8.27. Reserved (NID = 19h)

8.28. Reserved (NID = 20h)

8.29. DigBeep (NID = 21h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 7h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Rsvd2 | 19:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

8.29.1. DigBeep (NID = 21h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 17h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 03h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

8.29.2. DigBeep (NID = 21h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

8.29.3. DigBeep (NID = 21h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

8.29.4. DigBeep (NID = 21h): Gen

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ah |
| Get | F0A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Divider | 7:0 | RW | 00h | POR - DAFG - LR |
| | Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). | | | |

9. PINOUT

9.1. Pin Assignment

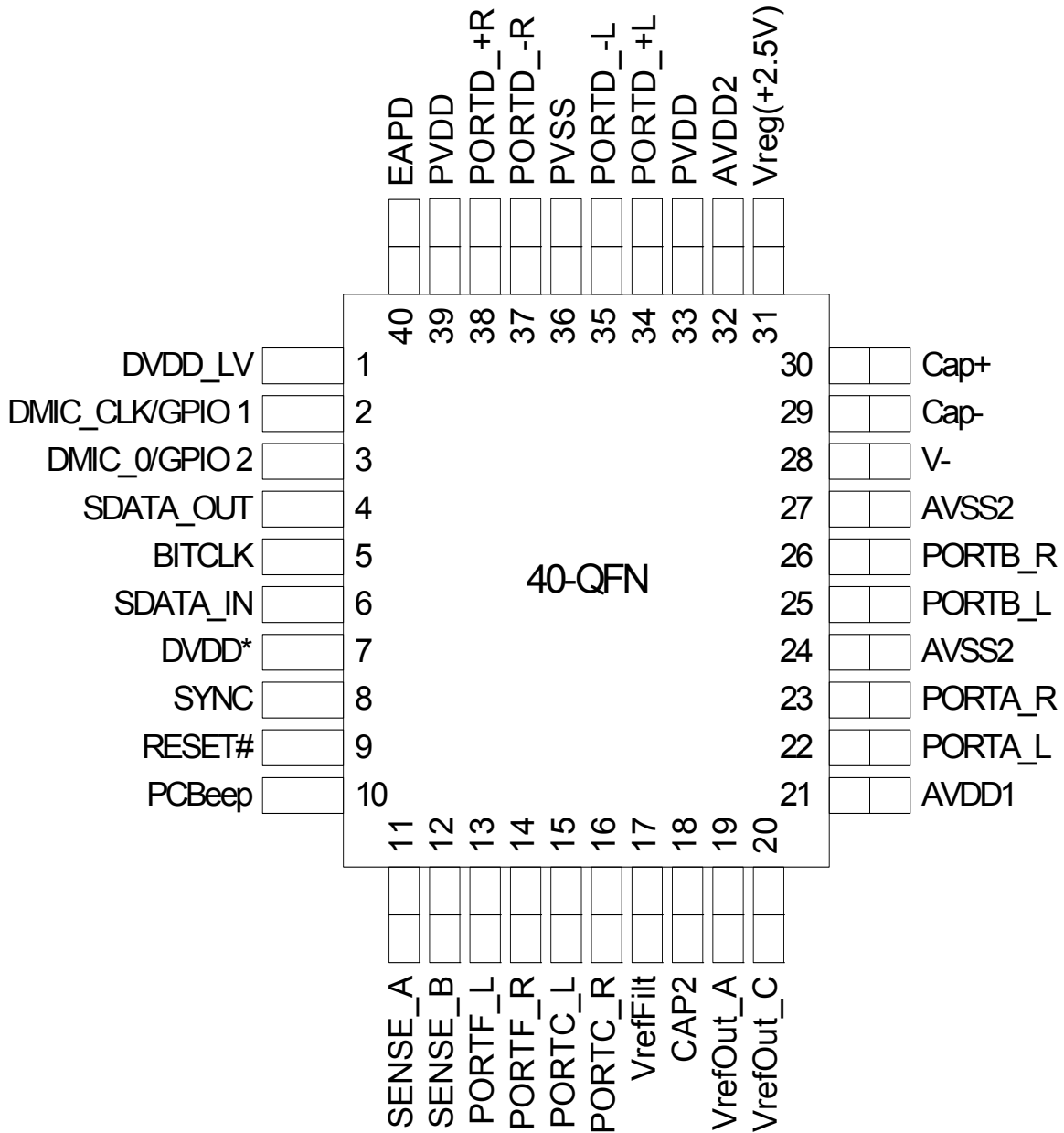


Figure 11. Pin Assignment

9.2. Pin Table

| Pin Name | Pin Function | I/O | Internal Pull-up/Pull-down | Pin location |
|----------------|---|--------------|----------------------------|--------------|
| DVDD_CORE | 1.5V Digital Core Regulator Filter Cap | O(Digital) | None | 1 |
| DMIC_CLK/GPIO1 | Digital Mic Clock Output/GPIO1 | I/O(Digital) | 60K Pull-down | 2 |
| DMIC0/GPIO2 | Digital Mic 0 Input/GPIO2 | I/O(Digital) | 60K Pull-down | 3 |
| SDATA_OUT | HD Audio Serial Data output from controller | I/O(Digital) | None | 4 |
| BITCLK | HD Audio Bit Clock | I(Digital) | None | 5 |
| SDATA_IN | HD Audio Serial Data Input to controller | O(Digital) | None | 6 |
| DVDD | Digital Vdd= 3.3V | I(Digital) | None | 7 |
| SYNC | HD Audio Frame Sync | I(Digital) | None | 8 |
| RESET# | HD Audio Reset | I(Digital) | None | 9 |
| PCBEEP | PC Beep | I(Analog) | None | 10 |
| SENSE_A | Jack insertion detection Ports A,B,C | I(Analog) | None | 11 |
| SENSE_B | Jack insertion detection Ports E,F | I(Analog) | None | 12 |
| PORTF_L | Port F Left | I/O(Analog) | None | 13 |
| PORTF_R | Port F Right | I/O(Analog) | None | 14 |
| PORTC_L | Port C Left | I/O(Analog) | None | 15 |
| PORTC_R | Port C Right | I/O(Analog) | None | 16 |
| VREFFILT | Analog Virtual Ground | O(Analog) | None | 17 |
| CAP2 | Reference filter Cap | O(Analog) | None | 18 |
| VREFOUT-A | Reference Voltage out drive (for mic bias) | O(Analog) | None | 19 |
| VREFOUT-C | Reference Voltage out drive (for mic bias) | O(Analog) | None | 20 |
| AVDD1 | Analog Vdd=5.0V or 3.3V | I(Analog) | None | 21 |
| PORTA_L (HP0) | Port A Output Left | I/O(Analog) | None | 22 |
| PORTA_R (HP0) | Port A Output Right | I/O(Analog) | None | 23 |
| AVSS | Analog Ground | I(Analog) | None | 24 |
| PORTB_L (HP1) | Port B Output Left | I/O(Analog) | None | 25 |
| PORTB_R (HP1) | Port B Output Right | I/O(Analog) | None | 26 |
| AVSS | Analog Ground | I(Analog) | None | 27 |
| V- | Negative analog supply | O(Analog) | None | 28 |
| CAP- | Charge pump cap - | O(Analog) | None | 29 |
| CAP+ | Charge pump cap + | O(Analog) | None | 30 |
| VREG | Linear Regulator Output (2.5V) filter cap | O(Analog) | None | 31 |
| AVDD2 | Analog Supply for VREG | I(Analog) | None | 32 |
| PVDD | Analog Supply for Class-D amp | I(Analog) | None | 33 |
| PORTD_+L | BTL amp Left + | O(Analog) | None | 34 |
| PORTD_-L | BTL amp Left - | O(Analog) | None | 35 |
| PVSS | Analog Ground | I(Analog) | None | 36 |

Table 24. Pinout List

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+STEREO SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Pin Name | Pin Function | I/O | Internal Pull-up/Pull-down | Pin location |
|----------|-------------------------------|--------------------------|----------------------------|--------------|
| PORTD_-R | BTL amp Right - | O(Analog) | None | 37 |
| PORTD_+R | BTL amp Right + | O(Analog) | None | 38 |
| PVDD | Analog Supply for Class-D amp | I(Analog) | None | 39 |
| EAPD | EAPD | I/O (Open Drain Digital) | 60K pull-up | 40 |

Table 24. Pinout List

9.3. Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95

POD IN BOTTOM VIEW

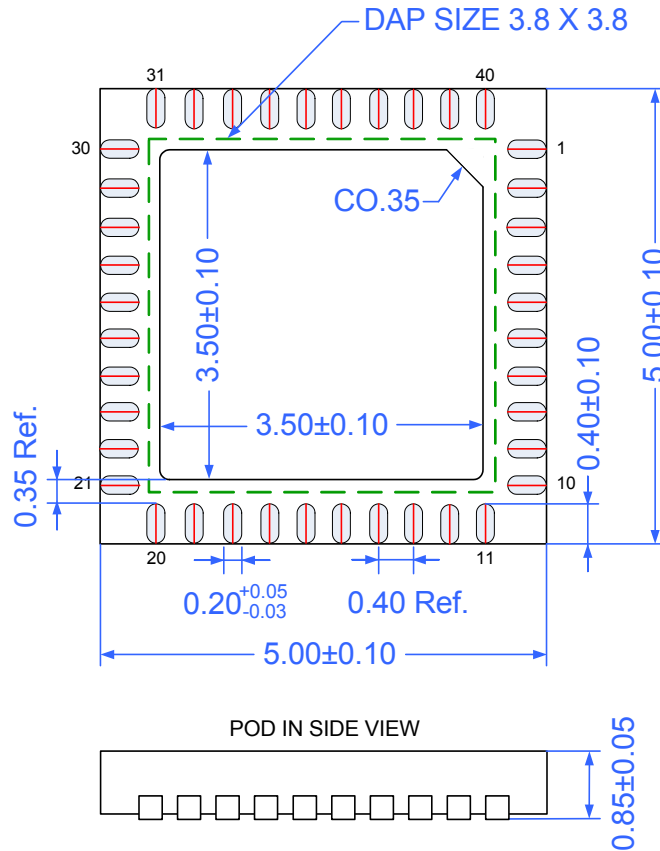


Figure 12. 40QFN Package Diagram

9.4. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices” (www.jedec.org/download).

| Profile Feature | Pb Free Assembly |
|---|--|
| Average Ramp-Up Rate ($T_{s_{max}} - T_p$) | 3 °C / second max |
| Preheat: Temperature Min ($T_{s_{min}}$) Temperature Max ($T_{s_{max}}$) Time ($t_{s_{min}} - t_{s_{max}}$) | 150 °C 200 °C 60 - 180 seconds |
| Time maintained above: Temperature (T_L) Time (t_L) | 217 °C 60 - 150 seconds |
| Peak / Classification Temperature (T_p) | See “Package Classification Reflow Temperatures” |
| Time within 5 °C of actual Peak Temperature (t_p) | 20 - 40 seconds |
| Ramp-Down rate | 6 °C / second max |
| Time 25 °C to Peak Temperature | 8 minutes max |

Note: All temperatures refer to topside of the package, measured on the package body surface.

Table 25. Standard Reflow Profile

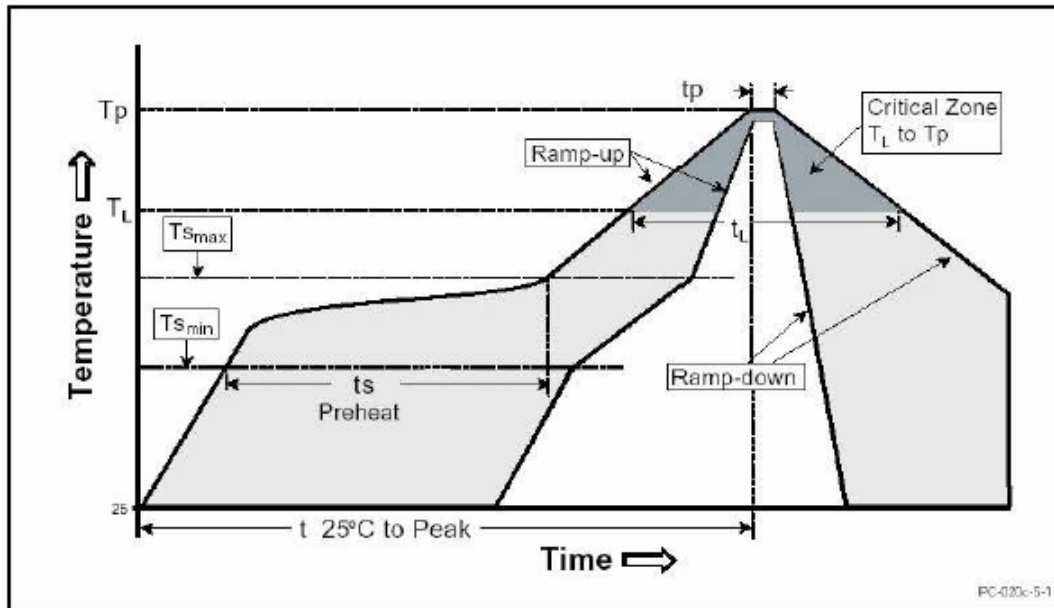


Figure 13. Solder Reflow Profile

10. DISCLAIMER

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11. DOCUMENT REVISION HISTORY

| Revision | Date | Description of Change |
|----------|---------------|---|
| 0.93 | April 2010 | initial release |
| 0.94 | July 2010 | Added Aux mode description section |
| 0.95 | October 2010 | PortC as input only for TB silicon revision |
| 0.99 | October 2010 | SA revision, Port C is input and output. BTL/SD_Mode default changed. High pass filter feature added (description and widgets to control DAC0/1 ProcState and ProIndex), updated datasheet formatting to new style. ECR15B references changed to HDA015-B. Removed Preliminary. |
| 0.99 | November 2010 | Additional SA revision changes. ADC0Mux, ADC1Mux and Mixer widgets connection lists differ from TB silicon. Values for both revisions listed for each con# item. |
| 0.995 | January 2011 | Updated SA revision comments for RA revisions. |