Wire bonding vertical SiCap WASC522.310 (100pF/0101/BV>150V)

Rev. 2.0

General description

The WAS Capacitor has been qualified according to AECQ-100 up to 68V, Grade 0 (-40°C/+150°C) 2000 cycles TMCL. Qualification report of the BV150 technology according to AECQ100 requirements is available on request.
Target applications are decoupling and filtering of active devices when miniaturization and low ESL are required. This product is a single 100pF capacitor in 0.25 x 0.25mm package size. Other capacitance values and other package size are available as a single die or capacitor array; please feel free to contact us.
The WAS Capacitor is based on PICS Integrated Passive technology.

Standard PCB FR4 can be used.

Assembly: WASC capacitors are directly mounted on the PCB application using die bonding and wire bonding.

WASC capacitors have the bottom electrode in Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm) and top electrode in gold, other top finishing are available on request such as Aluminum.

Key features

- AECQ-100 Qualification
- Full compatible Monolithic ceramic capacitors for replacement
- Ultra-high stability of capacitance value:
  - Temperature 60ppm/K (-55 °C to +150 °C)
  - Voltage <0.02%/Volts
  - Negligible capacitance loss through ageing
- Low profile 0.1mm
- Small size 0.25 x 0.25 mm (0101 format)
- Break down voltage > 150V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0101 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

Key applications

- Any demanding automotive applications, such as ADAS sensors (Lidars, Radars) as well as all Automotive SiP devices (Mems sensors, TPMS…)
- Supply decoupling / filtering of active device
- High reliability applications
- Devices with battery operations
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)

Functional diagram

The next figure provides implementation set-up diagram.

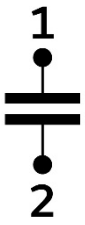

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	100	-	pF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	60	-	ppm/K
RV_{DC}	Rated voltage (3)		-		68(4) 61(5)	V_{DC}
BV	Break down voltage	@+25°C	150	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.02	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESL	Equivalent Serial Inductance (6)	@+25°C, SRF shunt mode	-	20	-	pH
ESR	Equivalent Serial Resistance (6)	@+25°C, shunt mode	-	150	-	mOhm
ESD	HBM stress (6)	JS-001-2017	500	-	-	V

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Pinning definition

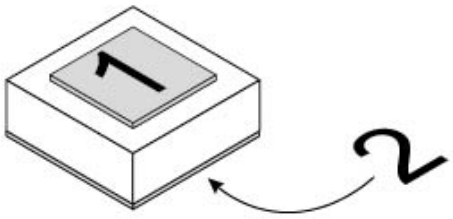

Figure 2 Pinning definition

pin #	Description
1	Top side Electrode finishing: Au
2	Back side Electrode finishing:Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm)

Table 2 - Pining description..

Ordering Information

Murata Integrated Passive Devices delivers products with AQL level II (0.65).

Type number (15NC)	Die name	Package		
		Packaging	Finishing	Description
935 148 522 310-F1T	WO0101310	6” FFC	Au(1)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm
935 148 522 310-W0T	WO0101310	Waffle pack 400units	Au(1)	100pF/0101 – 1 bondpad – 0.25 x 0.25mm x 0.10mm

(1) Au = TiW (0.3µm) / Au (3µm)

Table 3 - Packaging and ordering information

Pad Metallization

The standard pad finishing metallization is Au for the top pad and Ti (0.1 µm)/Ni (0.3µm)/Au (0.2µm) for the bottom pad.

Other Metallization, such as Thick Gold or Aluminum pads are possible on request.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative

Package outline

The product is delivered as a bare silicon die, with passivation opening for contacts.

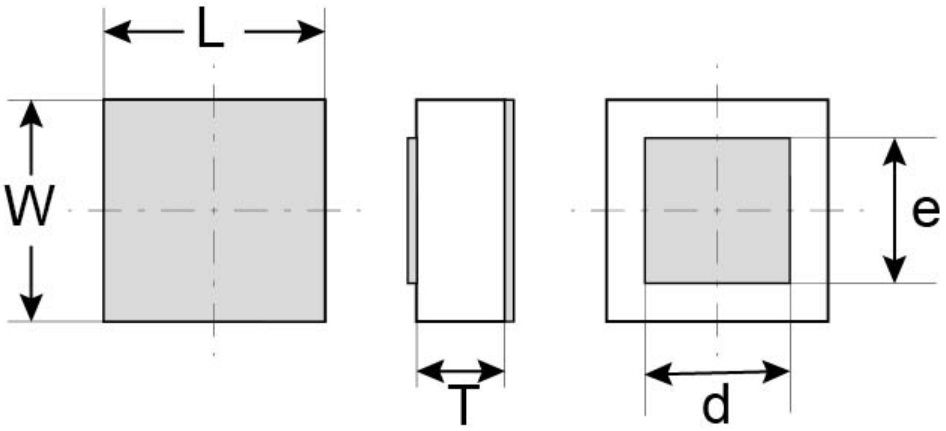

Figure 3 - Package outline drawing

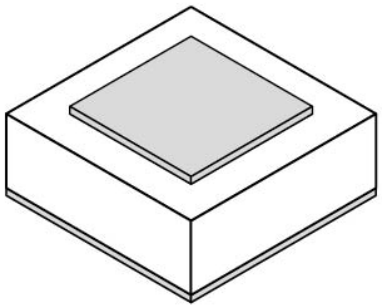

Figure 4 - Package isometric view

L (mm)	W (mm)	T (mm)	d (mm)	e (mm)
0.25 ±0.03	0.25 ±0.03	0.10 ±0.01	0.164	0.164

Table 4 - Dimensions and tolerances

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the appropriate e-mapping format. No ink is added on wafer to label other dies.

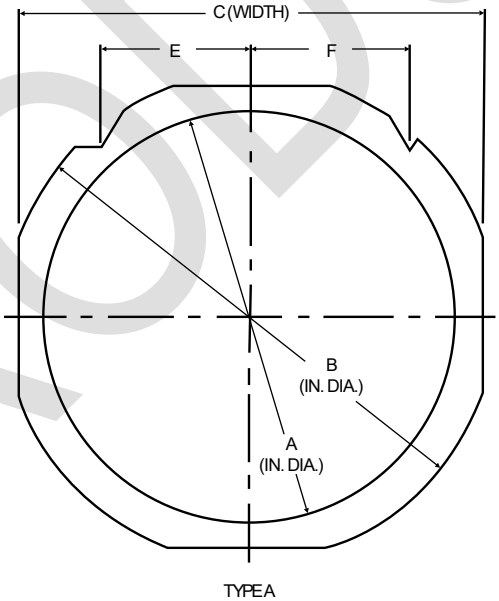

Figure 6 – Film frame drawing

Wafer diameter	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F	Frame style
6''	7.639"	8.976"	8.346"	0.048''	2.370"	2.5''	DTF-2-6-1

Table 5 - Frame dimensions (inches)

Waffle pack:

Please refer to application note ‘Waffle Pack Chip Carrier Handling & Opening Procedure’

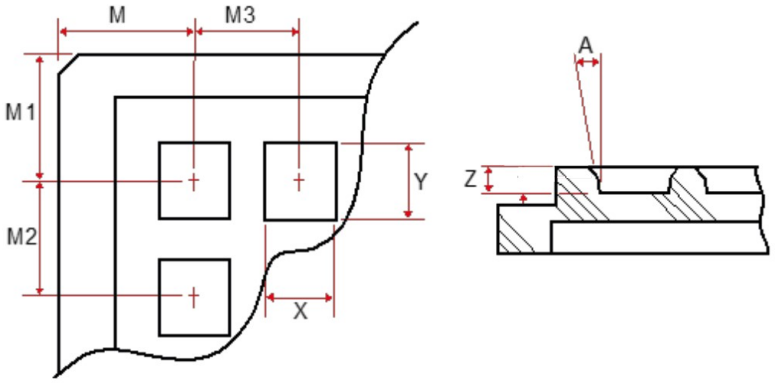

Figure 7 Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	0.36 ±0.05	0.36 ±0.05	0.13 ±0.05

Table 6 - Waffle pack dimensions (mm)

M	M1	M2	M3	A
4.55 ±0.08	4.55 ±0.08	2.18 ±0.05	2.18 ±0.05	7° ±1/2°

Table 7 - Waffle pack dimensions (mm)