

Description

The 9DB233 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB233 is driven by a differential SRC output pair from an IDT 932S421 or 932SQ420 or equivalent main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking. An SMBus interface allows control of the PLL bandwidth and bypass options, while 2 clock request (OE#) pins make the 9DB233 suitable for Express Card applications.

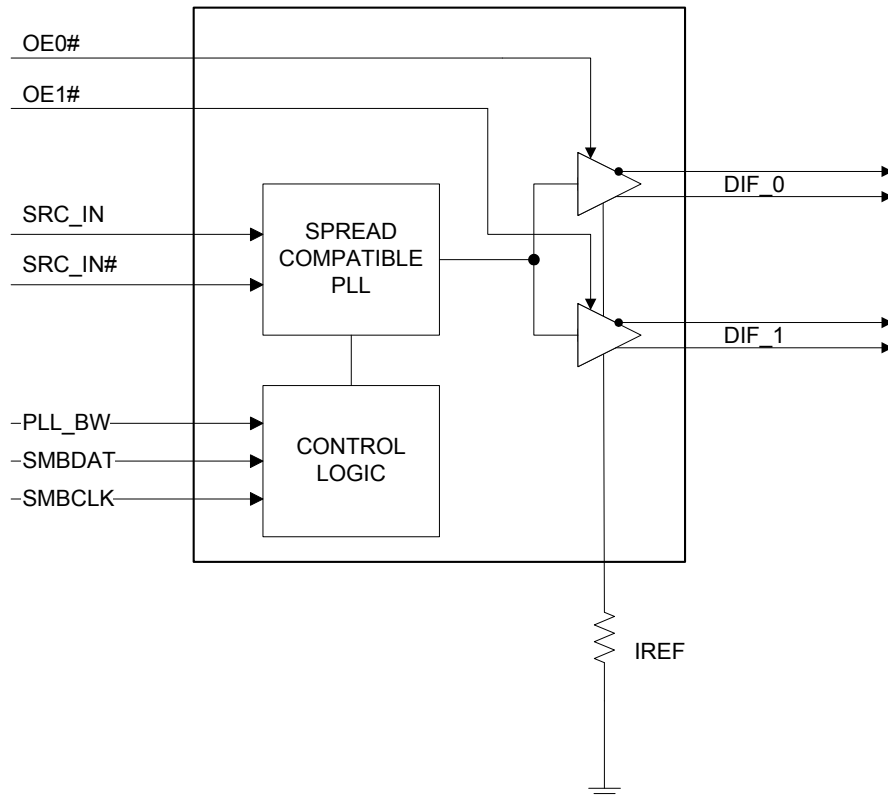
Recommended Application

2 output PCIe Gen3 zero-delay/fanout buffer

Output Features

- 2 - 0.7V current mode differential HCSL output pairs

Block Diagram



Features/Benefits

- OE# pins; suitable for Express Card applications
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI
- SMBus Interface; allows control of PLL BW and Mode

Key Specifications

- Cycle-to-cycle jitter < 50 ps
- Output-to-output skew < 50 ps
- PCIe Gen3 phase jitter < 1.0ps RMS

Pin Configuration

| | | | | |
|---------|----|---------------|----|--------|
| PLL_BW | 1 | 9DB233 | 20 | VDDA |
| SRC_IN | 2 | | 19 | GNDA |
| SRC_IN# | 3 | | 18 | IREF |
| vOE0# | 4 | | 17 | vOE1# |
| VDD | 5 | | 16 | VDD |
| GND | 6 | | 15 | GND |
| DIF_0 | 7 | | 14 | DIF_1 |
| DIF_0# | 8 | | 13 | DIF_1# |
| VDD | 9 | | 12 | VDD |
| SMBDAT | 10 | | 11 | SMBCLK |

Note: Pins preceded by ' v ' have internal 120K ohm pull down resistors

Power Distribution Table

| Pin Number | | Description |
|------------|------|-------------------------------|
| VDD | GND | |
| 5,9,12,16 | 6,15 | Differential Outputs |
| 9 | 6 | SMBUS |
| 20 | 19 | IREF |
| 20 | 19 | Analog VDD & GND for PLL core |

Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|---|
| 1 | PLL_BW | IN | 3.3V input for selecting PLL Band Width 0 = low, 1 = high |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 4 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 5 | VDD | PWR | Power supply, nominal 3.3V |
| 6 | GND | PWR | Ground pin. |
| 7 | DIF_0 | OUT | 0.7V differential true clock output |
| 8 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 9 | VDD | PWR | Power supply, nominal 3.3V |
| 10 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 11 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 12 | VDD | PWR | Power supply, nominal 3.3V |
| 13 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 14 | DIF_1 | OUT | 0.7V differential true clock output |
| 15 | GND | PWR | Ground pin. |
| 16 | VDD | PWR | Power supply, nominal 3.3V |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 19 | GND A | PWR | Ground pin for the PLL core. |
| 20 | VDD A | PWR | 3.3V power for the PLL core. |

Note:

Pins preceded by ' v ' have internal 120K ohm pull down resistors

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DB233. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDDA | | | | 4.6 | V | 1,2 |
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_{AMB}=T_{COM} or T_{IND} unless otherwise indicated, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|--------------------|---|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | V _{CROSS} | Cross Over Voltage | 150 | 375 | 900 | mV | 1 |
| Input Swing - DIF_IN | V _{SWING} | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 1 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | |
| Input Duty Cycle | d _{tin} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Current Consumption

T_A = T_{COM} or T_{IND}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|-----------------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD3.3OP} | All outputs active @100MHz, C _L = Full load; | | 70 | 80 | mA | 1 |
| Powerdown Current | I _{DD3.3PD} | All diff pairs driven | | | N/A | mA | 1 |
| | I _{DD3.3PDZ} | All differential pairs tri-stated | | | N/A | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| | T _{IND} | Industrial range | -40 | | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | µA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | µA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 10 | | 110 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 100MHz PLL mode | 33 | 100.00 | 110 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.800 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | cycles | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | | 300 | µs | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM}$ or T_{IND} ; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|-----------------------|---|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 0.6 | 2 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 4.2 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 791 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 13 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 801 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | 5 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1557 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 367 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | ΔVcross | Scope averaging off | | 46 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$.

$I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O=50\Omega$ (100 Ω differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

$T_A = T_{COM}$ or T_{IND} ; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 5\%$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|--|------|------|------|-------|-------|
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 2.2 | 4 | MHz | 1 |
| | | -3dB point in Low BW Mode | 0.4 | 0.5 | 1 | MHz | 1 |
| PLL Jitter Peaking | t_{JPEAK} | Peak Pass band Gain | | 0.6 | 1.5 | dB | 1 |
| Duty Cycle | t_{DC} | Measured differentially, PLL Mode | 45 | 48 | 55 | % | 1 |
| Duty Cycle Distortion | t_{DCD} | Measured differentially, Bypass Mode @100MHz | -2 | 0.4 | 2 | % | 1,4 |
| Skew, Input to Output | t_{pdBYP} | Bypass Mode, $V_T = 50\%$ | 2500 | 3660 | 4500 | ps | 1 |
| | t_{pdPLL} | Hi BW PLL Mode $V_T = 50\%$ | -50 | 136 | 350 | ps | 1 |
| Skew, Output to Output | t_{sk3} | $V_T = 50\%$ | | 16 | 50 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcy-cyc}$ | PLL mode | | 29 | 50 | ps | 1,3 |
| | | Additive Jitter in Bypass Mode | | 0.2 | 50 | ps | 1,3 |

¹Guaranteed by design and characterization, not 100% tested in production.

² $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O=50\Omega$.

³ Measured from differential waveform

⁴ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Electrical Characteristics–PCIe Phase Jitter Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|------------------------|--|-----|-----|-----|----------|-------|
| Phase Jitter, PLL Mode | t _{jphPCIeG1} | PCIe Gen 1 | | 34 | 86 | ps (p-p) | 1,2,3 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 1 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 2 | 3.1 | ps (rms) | 1,2 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 1 | 1 | ps (rms) | 1,2,4 |
| Additive Phase Jitter, Bypass Mode | t _{jphPCIeG1} | PCIe Gen 1 | | 2 | 5 | ps (p-p) | 1,2,3 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.2 | 0.3 | ps (rms) | 1,2 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.1 | 0.2 | ps (rms) | 1,2 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.1 | 0.2 | ps (rms) | 1,2,4 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

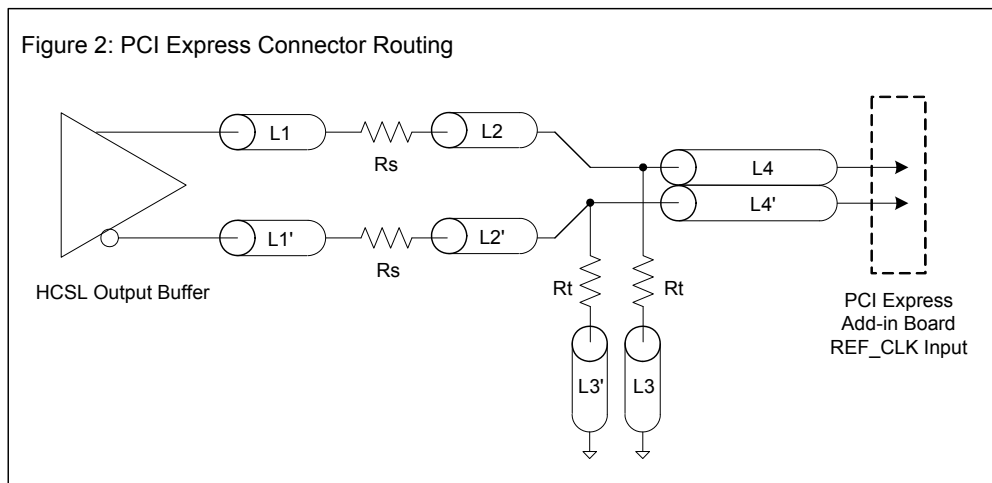
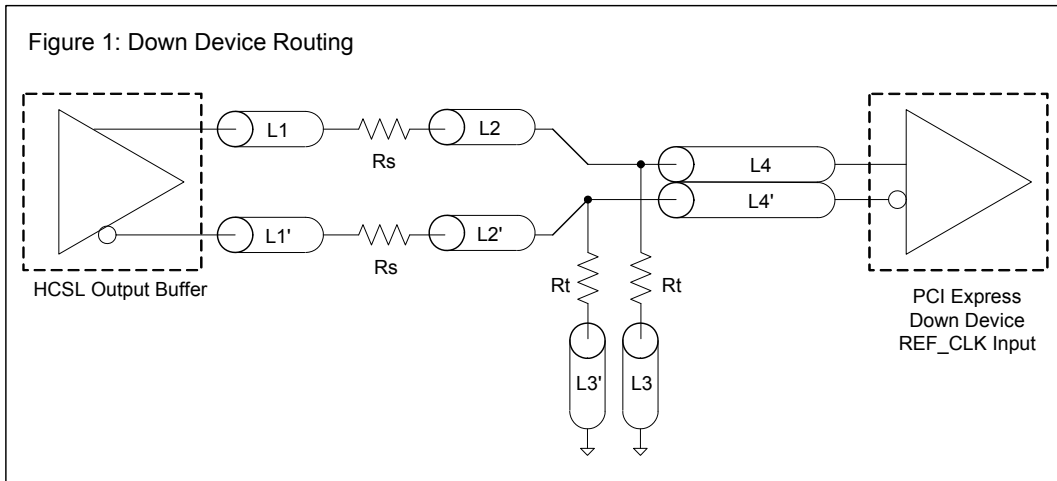
³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final ratification by PCI SIG.

| SRC Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

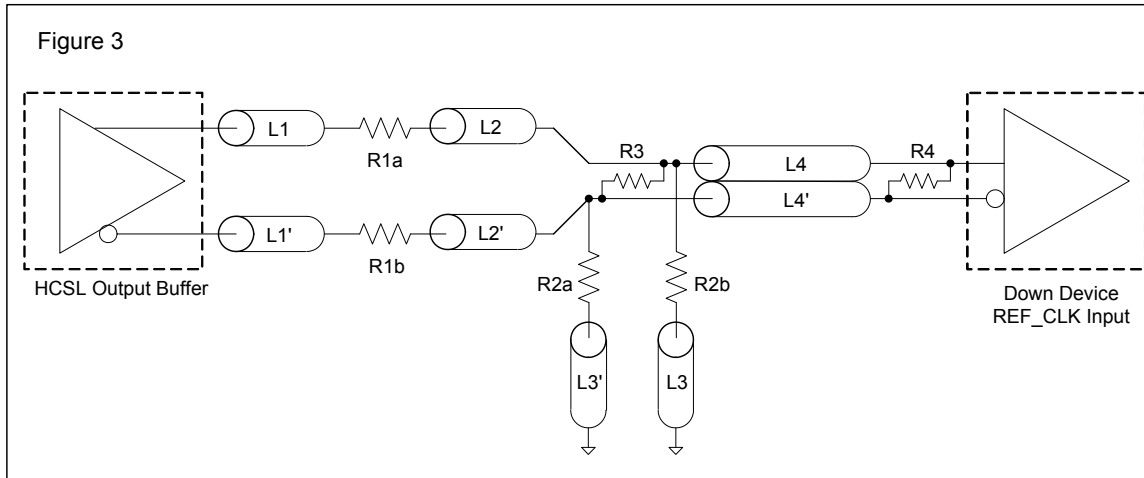
| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |



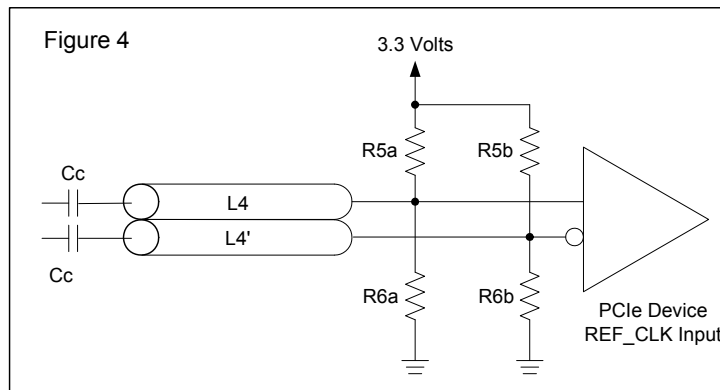
| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|------------------|-----------------|----|------|------|-----|--------------------------------|
| V _{diff} | V _{p-p} | V _{cm} | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μF | |
| V _{cm} | 0.350 volts | |



General SMBus Serial Interface Information for 9DB233

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|----------------------|-----|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| Beginning Byte = N | | | ACK |
| Data Byte Count = X | | | ACK |
| Beginning Byte N | | X Byte | ACK |
| O | | | O |
| O | | | O |
| O | | | O |
| Byte N + X - 1 | | | ACK |
| P | stoP bit | | |

| Read Address | Write Address |
|-------------------|-------------------|
| D5 _(H) | D4 _(H) |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|----------------------|------------------|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| Beginning Byte = N | | | ACK |
| Repeat starT | | | ACK |
| Slave Address | | | |
| RD | ReaD | | ACK |
| Data Byte Count=X | | | |
| ACK | | X Byte | Beginning Byte N |
| ACK | | | O |
| O | | | O |
| O | | | O |
| ACK | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Device Control Register, READ/WRITE ADDRESS (D5/D4)

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------------|---------------------------------------|------|---|---|---------|
| Bit 7 | - | SW_EN | Enables SMBus Control of bite 1 and 0 | RW | PLL Functions controlled by SMBus registers | PLL Functions controlled by device pins | 1 |
| Bit 6 | - | RESERVED | | RW | - | - | X |
| Bit 5 | - | RESERVED | | RW | - | - | X |
| Bit 4 | - | RESERVED | | RW | - | - | X |
| Bit 3 | - | RESERVED | | RW | - | - | X |
| Bit 2 | - | RESERVED | | RW | - | - | X |
| Bit 1 | - | PLL BW #adjust | Selects PLL Bandwidth | RW | Low BW | High BW | 1 |
| Bit 0 | - | PLL Enable | Bypasses PLL for board test | RW | PLL bypassed (fan out mode) | PLL enabled (ZDB mode) | 1 |

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7 | - | RESERVED | | RW | - | - | X |
| Bit 6 | - | RESERVED | | RW | - | - | X |
| Bit 5 | - | RESERVED | | RW | - | - | X |
| Bit 4 | - | RESERVED | | RW | - | - | X |
| Bit 3 | - | RESERVED | | RW | - | - | X |
| Bit 2 | - | RESERVED | | RW | - | - | X |
| Bit 1 | - | RESERVED | | RW | - | - | X |
| Bit 0 | - | RESERVED | | RW | - | - | X |

SMBus Table: Function Select Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---|---|---------|
| Bit 7 | - | RESERVED | | RW | - | - | X |
| Bit 6 | - | RESERVED | | RW | - | - | X |
| Bit 5 | - | RESERVED | | RW | - | - | X |
| Bit 4 | - | RESERVED | | RW | - | - | X |
| Bit 3 | - | RESERVED | | RW | - | - | X |
| Bit 2 | - | RESERVED | | RW | - | - | X |
| Bit 1 | - | RESERVED | | RW | - | - | X |
| Bit 0 | - | RESERVED | | RW | - | - | X |

SMBus Table: Vendor & Revision ID Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | 0 |
| Bit 6 | - | RID2 | | R | - | - | 0 |
| Bit 5 | - | RID1 | | R | - | - | 0 |
| Bit 4 | - | RID0 | | R | - | - | 1 |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBus Table: DEVICE ID

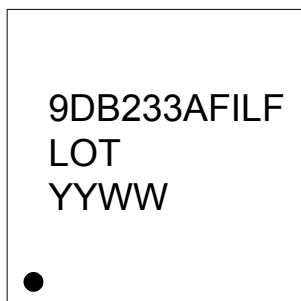
| Byte 4 | | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|---|-------|-----------------------|------------------|------|---|---|---------|
| Bit 7 | - | | Device ID = 06 Hex | | R | - | | 0 |
| Bit 6 | - | | | | R | - | | 0 |
| Bit 5 | - | | | | R | - | | 0 |
| Bit 4 | - | | | | R | - | | 0 |
| Bit 3 | - | | | | R | - | | 0 |
| Bit 2 | - | | | | R | - | | 1 |
| Bit 1 | - | | | | R | - | | 1 |
| Bit 0 | - | | | | R | - | | 0 |

SMBus Table: Byte Count Register

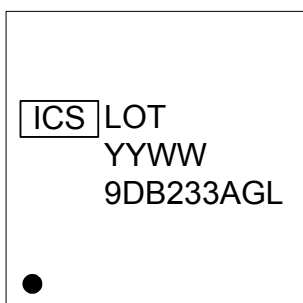
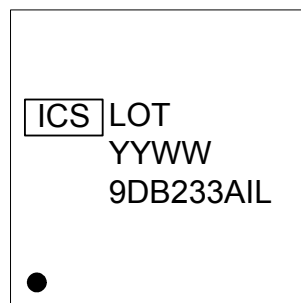
| Byte 5 | | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|---|-------|------|--|------|---|---|---------|
| Bit 7 | - | | BC7 | Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes. | RW | - | - | 0 |
| Bit 6 | - | | BC6 | | RW | - | - | 0 |
| Bit 5 | - | | BC5 | | RW | - | - | 0 |
| Bit 4 | - | | BC4 | | RW | - | - | 0 |
| Bit 3 | - | | BC3 | | RW | - | - | 0 |
| Bit 2 | - | | BC2 | | RW | - | - | 1 |
| Bit 1 | - | | BC1 | | RW | - | - | 1 |
| Bit 0 | - | | BC0 | | RW | - | - | 0 |

Marking Diagrams

20-pin SSOP



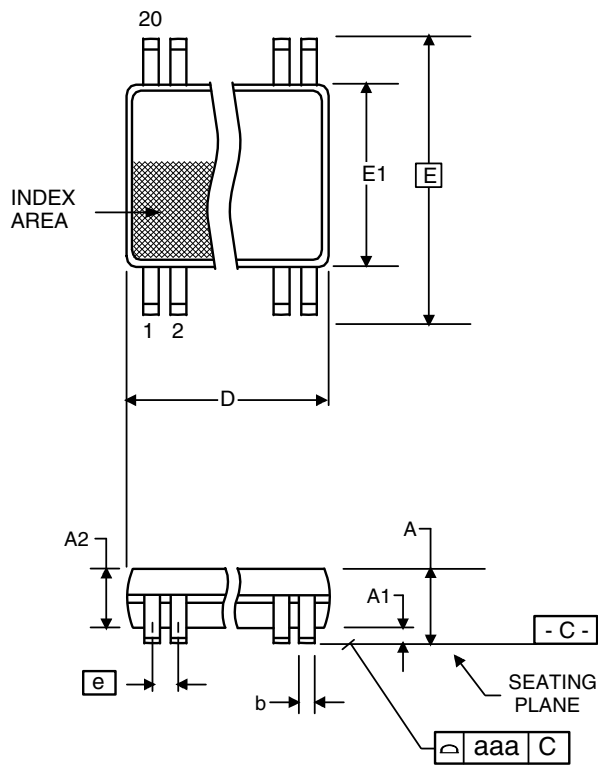
20-pin TSSOP



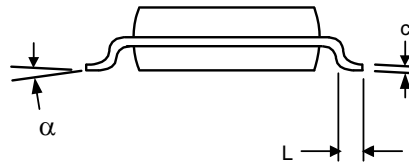
Notes:

1. "LOT" is the lot number.
2. "YYWW" is the last two digits of the year and week that the part was assembled.
3. "L" or "LF" denotes RoHS compliant package.
4. "I" denotes industrial temperature.
5. Bottom marking: country of origin if not USA.

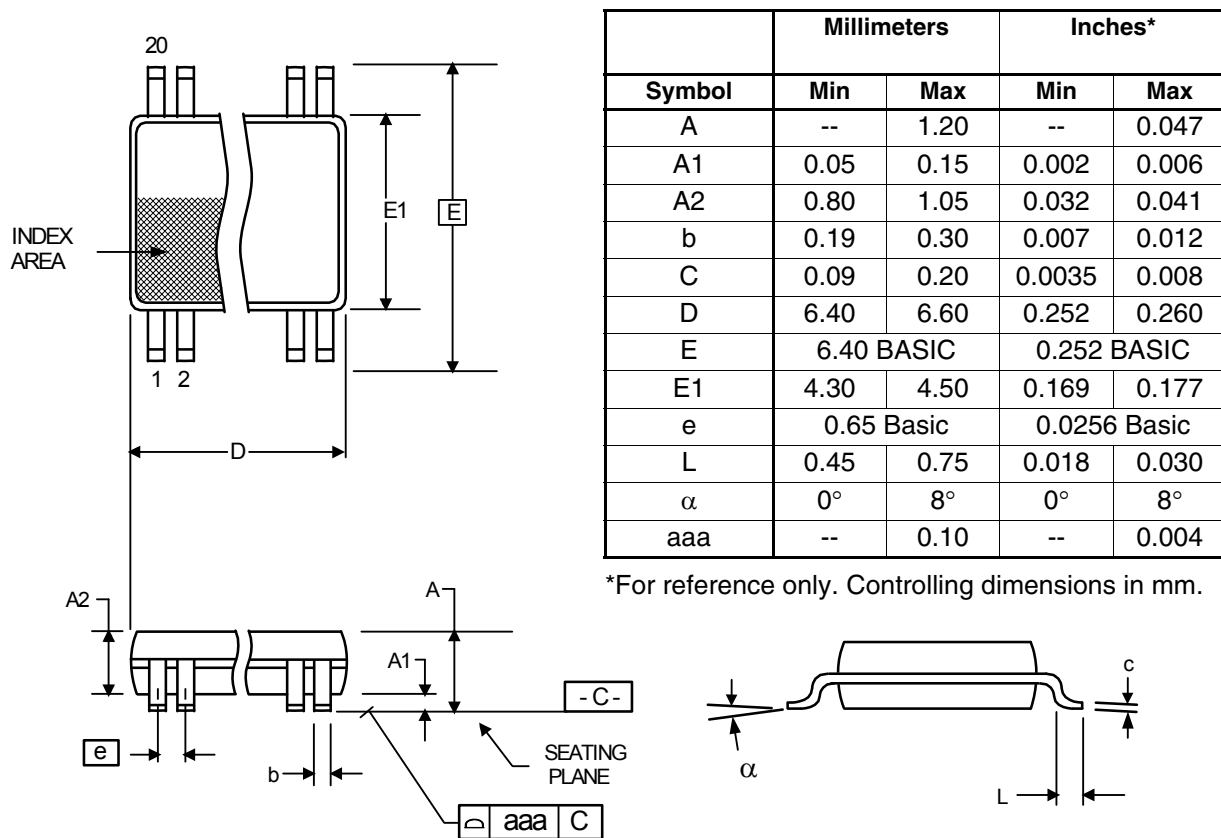
Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Wide Body)



| Symbol | Millimeters | | Inches | |
|----------|-------------|------|------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | -- | 1.50 | -- | 0.059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | .635 Basic | | .025 Basic | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |



Package Outline and Package Dimensions (20-pin TSSOP, 4.4mm Narrow Body)



Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|--------------|--------------|
| 9DB233AFLF | Tubes | 20-pin SSOP | 0 to +70°C |
| 9DB233AFLFT | Tape and Reel | 20-pin SSOP | 0 to +70°C |
| 9DB233AFILF | Tubes | 20-pin SSOP | -40 to +85°C |
| 9DB233AFILFT | Tape and Reel | 20-pin SSOP | -40 to +85°C |
| 9DB233AGLF | Tubes | 20-pin TSSOP | 0 to +70°C |
| 9DB233AGLFT | Tape and Reel | 20-pin TSSOP | 0 to +70°C |
| 9DB233AGILF | Tubes | 20-pin TSSOP | -40 to +85°C |
| 9DB233AGILFT | Tape and Reel | 20-pin TSSOP | -40 to +85°C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

| Rev. | Who | Issue Date | Description | Page # |
|------|-----|------------|---|---------|
| A | RDW | 6/30/2010 | Released to final | |
| B | RDW | 7/12/2010 | 1. Changed PWD to Default in SMBus tables. | 10,11 |
| C | RDW | 4/14/2011 | Changed pull down indicator from '**' to 'v'. | |
| D | RDW | 4/9/2012 | 1. Updated typical electrical characteristics to reflect improved performance | 3-6 |
| E | RDW | 2/19/2014 | 1. Corrected typo for Read/Write address from D4/D5 to D5/D4 respectively. 2. Added device marking diagrams. | Various |
| F | RDW | 10/20/2016 | Updated input clock electrical table to latest format. No change to form, fit or function of the device | 4 |

9DB233

TWO OUTPUT DIFFERENTIAL BUFFER FOR PCIE GEN3