DATASHEET

Description

The 9DBL07x1 devices are 3.3V members of IDT's Full-Featured PCIe clock family. The 9DBL07x1 devices support PCIe Gen1–4 Common Clocked (CC) and PCIe Separate Reference Independent Spread (SRIS) systems. They offer a choice of integrated output terminations providing direct connection to 85Ω or 100Ω transmission lines. The 9DBL07P1 can be factory programmed with a user-defined power up default SMBus configuration.

Recommended Application

PCIe Gen1–4 clock distribution for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

Output Features

- 7 – 1-200 MHz Low-Power (LP) HCSL DIF pairs
  - 9DBL0741 default Zout = 100Ω
  - 9DBL0751 default Zout = 85Ω
  - 9DBL07P1 factory programmable defaults
- Easy AC-coupling to other logic families, see IDT application note AN-891.

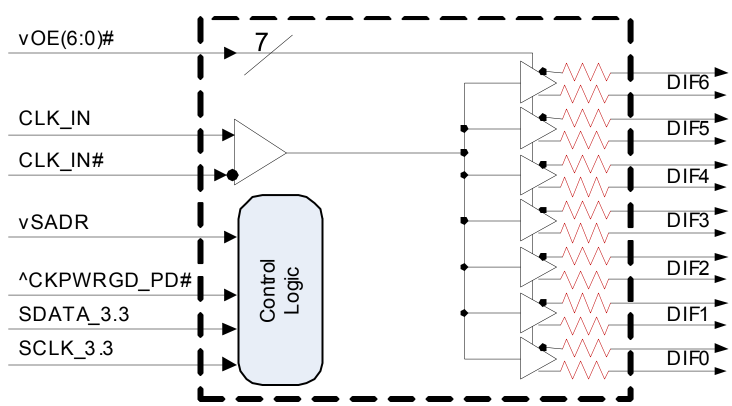
Key Specifications

- DIF *additive* cycle-to-cycle jitter < 5ps
- DIF output-to-output skew < 50ps
- *Additive* phase jitter is 0ps (typical rms) for PCIe Gen1–4 CC, SRIS
- *Additive* phase jitter 111fs rms typ. at 156.25M (1.5M to 10M)

Features/Benefits

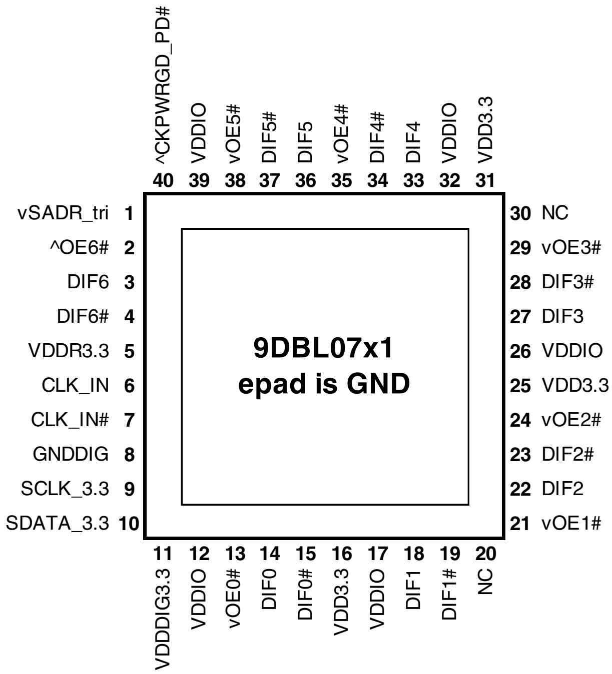
- Direct connection to 100Ω (xx41) or 85Ω (xx51) transmission lines; saves 28 resistors compared to standard PCIe devices
- 134mW typical power consumption; eliminate thermal concerns
- VDDIO allows 50% power savings at optional 1.05V; maximum power savings
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - differential output amplitude
  - output impedance for each output
- Customer defined SMBus power up default can be programmed into P1 device; allows exact optimization to customer requirements
- OE# pins; support DIF power management
- HCSL differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- Device contains default configuration; SMBus interface not required for device operation
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 40-pin 5 x 5mm VFQFPN; minimal board space

Block Diagram



Note: Resistors default to internal on 41/51 devices. P1 devices have programmable default impedances on an output-by-output basis.

Pin Configuration



40-VFQFPN, 5x5mm 0.4mm pin pitch

^v prefix indicates internal 120KOhm pull up *AND pull* down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx	
				True O/P	Comp. O/P
0	X	X	X	Low[1]	Low[1]
1	Running	0	X	Low[1]	Low[1]
1	Running	1	0	Running	Running
1	Running	1	1	Low[1]	Low[1]

1. The output state is set by B11[1:0] (Low/Low default)

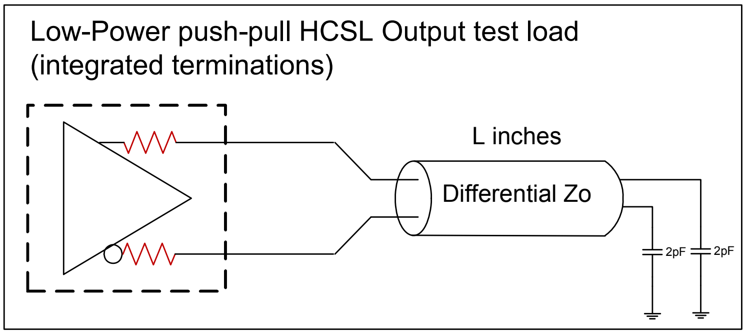
Power Connections

Pin Number			Description
VDD	VDDIO	GND	
5		41	Input receiver analog
11		8	Digital Power
16,25,31	12,17,26,32,39	41	DIF outputs

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	vSADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.
2	^OE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs
3	DIF6	OUT	Differential true clock output
4	DIF6#	OUT	Differential Complementary clock output
5	VDDR3.3	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
6	CLK_IN	IN	True Input for differential reference clock.
7	CLK_IN#	IN	Complementary Input for differential reference clock.
8	GNDDIG	GND	Ground pin for digital circuitry
9	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
10	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
11	VDDDIG3.3	PWR	3.3V digital power (dirty power)
12	VDDIO	PWR	Power supply for differential outputs
13	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
14	DIF0	OUT	Differential true clock output
15	DIF0#	OUT	Differential Complementary clock output
16	VDD3.3	PWR	Power supply, nominal 3.3V
17	VDDIO	PWR	Power supply for differential outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	NC	N/A	No Connection.
21	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
22	DIF2	OUT	Differential true clock output
23	DIF2#	OUT	Differential Complementary clock output
24	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	VDD3.3	PWR	Power supply, nominal 3.3V
26	VDDIO	PWR	Power supply for differential outputs
27	DIF3	OUT	Differential true clock output
28	DIF3#	OUT	Differential Complementary clock output
29	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
30	NC	N/A	No Connection.
31	VDD3.3	PWR	Power supply, nominal 3.3V
32	VDDIO	PWR	Power supply for differential outputs
33	DIF4	OUT	Differential true clock output
34	DIF4#	OUT	Differential Complementary clock output
35	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
36	DIF5	OUT	Differential true clock output
37	DIF5#	OUT	Differential Complementary clock output
38	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
39	VDDIO	PWR	Power supply for differential outputs
40	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
41	ePAD	GND	Connect paddle to ground.

Test Loads



L = 5 inches

Terminations

Device	Zo (Ω)	Rs (Ω)
9DBL0741	100	None needed
9DBL0751	100	7.5
9DBL07P1	100	Prog.
9DBL0741	85	N/A
9DBL0751	85	None needed
9DBL07P1	85	Prog.

Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBL07x1. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx				4.6	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2500			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency			500	kHz	2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2.] The device must be powered up for the SMBus to function.

[3.] The differential input clock must be running for the SMBus to be active

Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Output Supply Voltage	VDDIO	Supply voltage for Low Power HCSL Outputs	0.95	1.05-3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix)	0.75 V_{DDx}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 V_{DDx}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	F_{IN}		1		200	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	1.7	2.7	4	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	0.8	1.9	2.8	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching		6	20	%	1,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	783	850	mV	7
Voltage Low	V_{LOW}		-150	-17	150		7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		818	1150	mV	7
Min Voltage	Vmin		-300	-54			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	377	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		18	140	mV	1,6

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DD}	VDD + VDDR All outputs active @100MHz, 100Δ Loads		12	16	mA	
	I_{DDDIG}	VDDDIG All outputs active @100MHz, 100Δ Loads		0.4	0.8	mA	
	I_{DDIO}	VDDIO All outputs active @100MHz, 100Δ Loads		28	32	mA	
Powerdown Current	I_{DDPD}	VDD + VDDR, CKPWRGD_PD#=0		1.4	2	mA	2
	$I_{DDDIGPD}$	VDDDIG, CKPWRGD_PD#=0		0.4	0.8	mA	2
	I_{DDIOPD}	VDDIO, CKPWRGD_PD#=0		0.0	0.1	mA	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	t_{DCD}	Measured differentially, 100MHz	-1	-0.1	1	%	1,3
Skew, Input to Output	t_{pd}	V_T = 50%	2200	2982	4000	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%		43	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	*Additive* Jitter		0.1	1	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures[1,5]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1		0.4	2	n/a	ps (p-p)	2,3
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.0	0.1		ps (rms)	2,4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.24	0.5		ps (rms)	2,4
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.07	0.15		ps (rms)	2,4
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.07	0.15		ps (rms)	2,4

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

[5] Driven by 9FGL0841 or equivalent

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures[1]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter	$t_{jphPCIeG1\text{-}SRIS}$	PCIe Gen 1	TBD			Note 5	ps (pk-pk)	2,3
	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.3	0.4		ps (rms)	2
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.03	0.13		ps (rms)	2
	$t_{jphPCIeG4\text{-}SRIS}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	TBD				ps (rms)	2

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Based PCIe Base Specification Rev3.1a filters. These filters are different than Common Clock filters. See http://www.pcisig.com for latest specifications and are not defined for Gen1 or Gen4

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values, additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

[5] As of PCIe Base Specification Rev4.0 draft 0.7, SRIS limits are defined as implementation depdendent.

Electrical Characteristics–Unfiltered Phase Jitter Parameters[1]

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter	$t_{jph156M}$	156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		111		N/A	fs (rms)	2,3
	$t_{jph156M12k\text{-}20}$	156.25MHz, 12kHz to 20MHz, -20dB/decade rollover <12kHz, -40db/decade rolloff > 20MHz		272		N/A	fs (rms)	2,3

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Driven by Rohde & Schartz SMA100

[3] For RMS values, additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N			
			ACK
O			
O		X Byte	O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus Address is Latched on SADR pin.
Unless otherwise indicated, default values are for the x41 and xx51. P1 devices are fully factory programmable.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
			Beginning Byte N
ACK			
			O
O		X Byte	O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE5	Output Enable	RW	Low/Low	Enabled	1
Bit 6	DIF OE4	Output Enable	RW	Low/Low	Enabled	1
Bit 5	Reserved					1
Bit 4	DIF OE3	Output Enable	RW	Low/Low	Enabled	1
Bit 3	DIF OE2	Output Enable	RW	Low/Low	Enabled	1
Bit 2	DIF OE1	Output Enable	RW	Low/Low	Enabled	1
Bit 1	Reserved					1
Bit 0	DIF OE0	Output Enable	RW	Low/Low	Enabled	1

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: Output Enable and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					1
Bit 5	DIF OE6	Output Enable	RW	Low/Low	Enabled	1
Bit 4	Reserved					0
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01= 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF5	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF4	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1
Bit 5	Reserved					1
Bit 4	SLEWRATESEL DIF3	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF2	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF1	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1

SMBus Table: DIF Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL DIF6	Adjust Slew Rate	RW	Slow Setting	Fast Setting	1

Byte 4 is Reserved and reads back 'hFF

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	B rev = 0001		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			1
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx, 10 = DMx, 11= DBx w/oPLL		1
Bit 6	Device Type0		R			1
Bit 5	Device ID5	Device ID	R	000111 binary or 07 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			0
Bit 2	Device ID2		R			1
Bit 1	Device ID1		R			1
Bit 0	Device ID0		R			1

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved

SMBus Table: PLL MN Enable, PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Impedance Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	DIF6_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF6_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF2_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF2_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	DIF1_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 4	DIF1_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					
Bit 2	Reserved					
Bit 1	DIF0_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 0	DIF0_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	DIF5_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF5_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	DIF4_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 4	DIF4_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					
Bit 2	Reserved					
Bit 1	DIF3_imp[1]	Set Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 0	DIF3_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	

Note: xx41 = 10, xx51 = 01, P1 = factory programmable.

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE2_pu/pd[1]	Set Pull-up(PuP)/ Pull-down(Pdwn)	RW	00=None	10=Pup	0
Bit 6	OE2_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE1_pu/pd[1]	Set Pull-up(PuP)/ Pull-down(Pdwn)	RW	00=None	10=Pup	0
Bit 4	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	OE0_pu/pd[1]	Set Pull-up(PuP)/ Pull-down(Pdwn)	RW	00=None	10=Pup	0
Bit 0	OE0_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1

Note: These values are for xx41 and xx51. P1 is factory programmable.

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	OE5_pu/pd[1]	Set Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 6	OE5_pu/pd[0]	Pull-down(Pdwn)	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE4_pu/pd[1]	Set Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 4	OE4_pu/pd[0]	Pull-down(Pdwn)	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	OE3_pu/pd[1]	Set Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 0	OE3_pu/pd[0]	Pull-down(Pdwn)	RW	01=Pdwn	11 = Pup+Pdwn	1

Note: These values are for xx41 and xx51. P1 is factory programmable.

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					1
Bit 4	Reserved					0
Bit 3	OE6_pu/pd[1]	Set Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 2	OE6_pu/pd[0]	Pull-down(Pdwn)	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	0

Note: These values are for xx41 and xx51. P1 is factory programmable.

Bytes 17 is Reserved and reads back 0h00.

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	OE5_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 6	OE4_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	Reserved					0
Bit 4	OE3_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE2_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	OE1_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	Reserved					0
Bit 0	OE0_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0

SMBus Table: Polarity Control

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	OE6_polarity	Sets OE polarity	RW	Enabled when Low	Enabled when High	0
Bit 0	CKPWRGD_PD	Sets CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Marking Diagrams

ICS
BL0741BI
YYWW
COO
LOT

ICS
BL0751BI
YYWW
COO
LOT

ICS
7P1B000I
YYWW
COO
LOT

Notes:
1. "LOT" is the lot sequence number.
2. "COO" denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. "I" denotes industrial temperature range device.

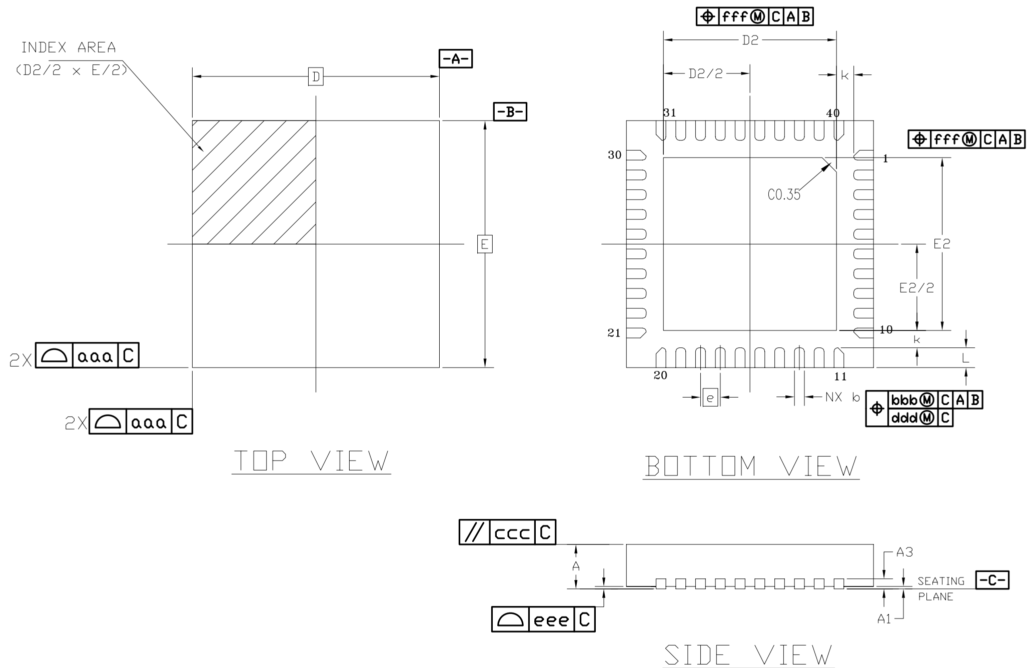
Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NDG40	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	$\theta_{JA0\theta}$	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1]ePad soldered to board

Package Outline and Dimensions (NDG40P2)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/17/16	JH



SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
L	0.30	0.40	0.50
e		0.40 BSC	
N		40	
ND		10 (note 3)	
NE		10 (note 3)	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k		0.35 REF	
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2 ALL DIMENSIONS ARE IN MILLIMETERS.
3. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

TOLERANCES UNLESS SPECIFIED
DECIMAL X±.1 XX±.05 XXX± .030
ANGULAR ±1°

IDT™ www.IDT.com

6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

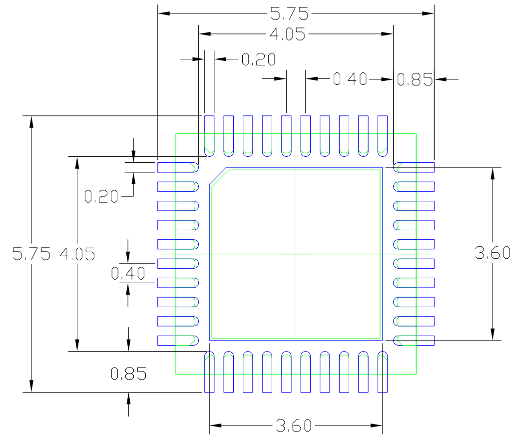
APPROVALS	DATE
DRAWN mæ	05/31/10
CHECKED	

TITLE ND/NDG40 PACKAGE OUTLINE
5.0 x 5.0 mm BODY,EPAD 3.50mm SQ.
0.40 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC–4292–02	00

DO NOT SCALE DRAWING SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/17/16	JH



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL X±.1 XX±.05 XXX± .030	ANGULAR ±1°	IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE ND/NDG40 PACKAGE OUTLINE 5.0 x 5.0 mm BODY,EPAD 3.50mm SQ. 0.40 mm PITCH QFN	
DRAWN mr	05/31/10		
CHECKED			
		SIZE C	DRAWING No. PSC-4292-02 / REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Ordering Information

Part / Order Number	Output Impedance	Shipping Packaging	Package	Temperature
9DBL0741BKILF	100Ω	Trays	40-pin VFQFPN	-40 to +85° C
9DBL0741BKILFT		Tape and Reel	40-pin VFQFPN	-40 to +85° C
9DBL0751BKILF	85Ω	Trays	40-pin VFQFPN	-40 to +85° C
9DBL0751BKILFT		Tape and Reel	40-pin VFQFPN	-40 to +85° C
9DBL07P1BxxxKILF	Factory configurable. Contact IDT for addtional information.	Trays	40-pin VFQFPN	-40 to +85° C
9DBL07P1BxxxKILFT		Tape and Reel	40-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).
"xxx" is a unique factory assigned number to identify a particular default configuration.

Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	9/19/2016	1. Updated front page text 2. Changed VDDA3.3 pin to VDD3.3, since this part has no PLL 3. Removed references to PLL mode, since this part has no PLL 4. Regrouped IDD values to simplify the table 5. Updated Electrical tables to latest version, including PCIe Gen4 6. Updated ordering information to B rev 7. Corrected readback of SMbus B1[1:0], B3[7], B5[4], B10[7], B16[5] - most of these are reserved bits 8. Updated footnote text under block diagram. 9. Updated block diagram for stylistic consistency. 10. Updated electrical tables with char data, move to final.	Various
B	RDW	9/28/2016	Fixed corrupted ohm symbols in Bytes 11, 12, and 13 register tables	13
C	RDW	8/1/2017	Removed reference to differential waveform in slew rate matching spec	7