# 8-Output 1.8V PCIe Zero-Delay/Fanout Clock Buffer with Zo = 100ohms

**9DBV0841**

**DATASHEET**

## Description

The 9DBV0841 is a 1.8V member of Renesas' full featured PCIe family. It has integrated output terminations providing Zo = 100Ω for direct connection for 100Ω transmission lines. The device has 8 output enables for clock management and 3 selectable SMBus addresses.

## Typical Applications

- SSD, microServers, WLAN Access points

## Output Features

- Eight 1–200MHz Low-Power (LP) HCSL DIF pairs

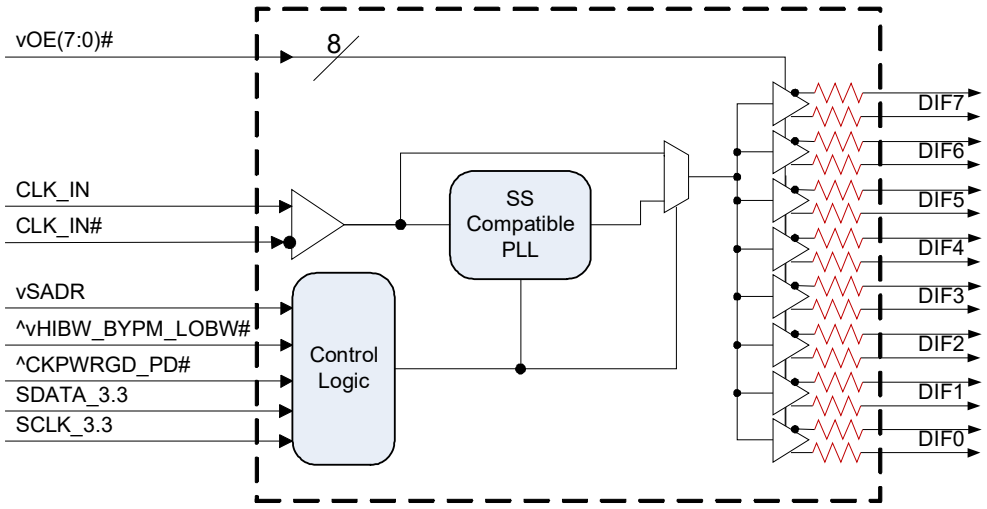
## Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- PCIe Gen5 CC additive phase jitter < 40fs RMS
- 12kHz–20MHz additive phase jitter = 156fs RMS at 156.25M (typical)

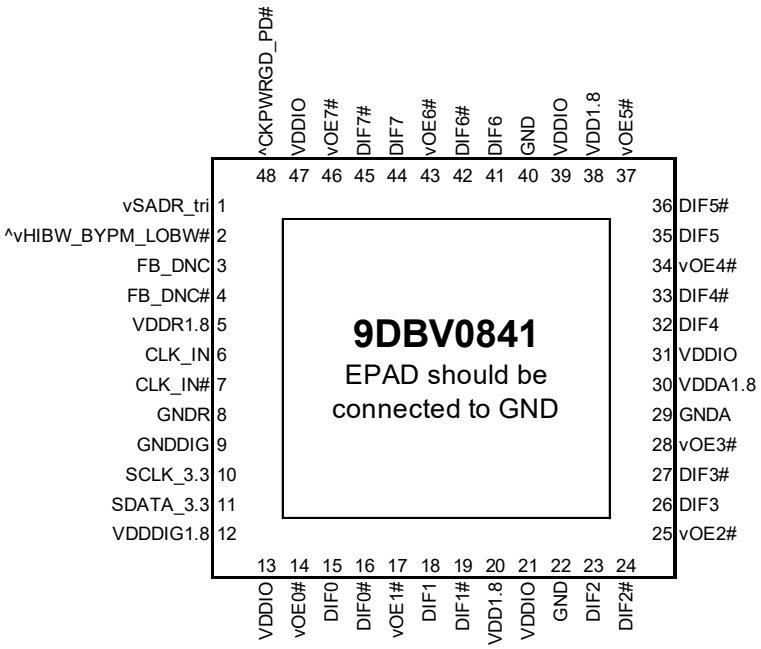
## Features/Benefits

- LP-HCSL outputs save 32 resistors; minimal board space and BOM cost
- 62mW typical power consumption in PLL mode; eliminates thermal concerns
- Spread Spectrum (SS) compatible; allows use of SS for EMI reduction
- OE# pins; support DIF power management
- HCSL compatible differential input; can be driven by common clock sources
- Programmable Slew rate for each output; allows tuning for various line lengths
- Programmable output amplitude; allows tuning for various application environments
- Pin/software selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- Outputs blocked until PLL is locked; clean system start-up
- Software selectable 50MHz or 125MHz PLL operation; useful for Ethernet applications
- Configuration can be accomplished with strapping pins; SMBus interface not required for device control
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 6 × 6 mm 48-VFQFPN; minimal board space
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment

## Block Diagram



# Pin Configuration




**48-pin VFQFPN, 6x6 mm, 0.4mm pitch**

^v prefix indicates internal 120KOhm pull up *AND pull* down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

^ prefix indicates internal 120KOhm pull up resistor

## SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|---|---|---|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

## Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | | PLL |
|---|---|---|---|---|---|---|
| | | | | True O/P | Comp. O/P | |
| 0 | X | X | X | Low | Low | Off |
| 1 | Running | 0 | X | Low | Low | On[1] |
| 1 | Running | 1 | 0 | Running | Running | On[1] |
| 1 | Running | 1 | 1 | Low | Low | On[1] |

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

## Power Connections

| Pin Number | | | Description |
|---|---|---|---|
| VDD | VDDIO | GND | |
| 5 | | 8 | Input receiver analog |
| 12 | | 9 | Digital Power |
| 20, 31, 38 | 13, 21, 31, 39, 47 | 22, 29, 40 | DIF outputs |
| 30 | | 29 | PLL Analog |

## Frequency Select Table

| FSEL Byte3 [4:3] | CLK_IN (MHz) | DIFx (MHz) |
|---|---|---|
| **00 (Default)** | 100.00 | CLK_IN |
| 01 | 50.00 | CLK_IN |
| 10 | 125.00 | CLK_IN |
| 11 | Reserved | Reserved |

## PLL Operating Mode

| HiBW_BypM_LoBW# | MODE | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|---|---|---|---|
| 0 | PLL Lo BW | 00 | 00 |
| M | Bypass | 01 | 01 |
| 1 | PLL Hi BW | 11 | 11 |

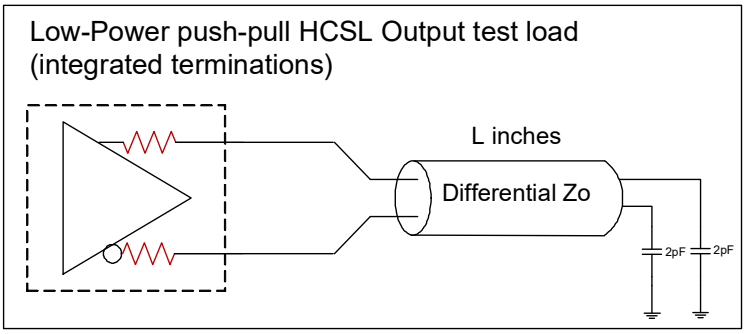
## Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | vSADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. See SMBus Address Selection Table. |
| 2 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 3 | FB_DNC | DNC | True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 4 | FB_DNC# | DNC | Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 5 | VDDR1.8 | PWR | 1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 6 | CLK_IN | IN | True Input for differential reference clock. |
| 7 | CLK_IN# | IN | Complementary Input for differential reference clock. |
| 8 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 9 | GNDDIG | GND | Ground pin for digital circuitry |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | VDDDIG1.8 | PWR | 1.8V digital power (dirty power) |
| 13 | VDDIO | PWR | Power supply for differential outputs |
| 14 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 15 | DIF0 | OUT | Differential true clock output |
| 16 | DIF0# | OUT | Differential Complementary clock output |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | OUT | Differential true clock output |
| 19 | DIF1# | OUT | Differential Complementary clock output |
| 20 | VDD1.8 | PWR | Power supply, nominal 1.8V |
| 21 | VDDIO | PWR | Power supply for differential outputs |
| 22 | GND | GND | Ground pin. |
| 23 | DIF2 | OUT | Differential true clock output |
| 24 | DIF2# | OUT | Differential Complementary clock output |
| 25 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 26 | DIF3 | OUT | Differential true clock output |
| 27 | DIF3# | OUT | Differential Complementary clock output |
| 28 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 29 | GNDA | GND | Ground pin for the PLL core. |
| 30 | VDDA1.8 | PWR | 1.8V power for the PLL core. |
| 31 | VDDIO | PWR | Power supply for differential outputs |
| 32 | DIF4 | OUT | Differential true clock output |
| 33 | DIF4# | OUT | Differential Complementary clock output |
| 34 | vOE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 35 | DIF5 | OUT | Differential true clock output |
| 36 | DIF5# | OUT | Differential Complementary clock output |
| 37 | vOE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 38 | VDD1.8 | PWR | Power supply, nominal 1.8V |

## Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 39 | VDDIO | PWR | Power supply for differential outputs |
| 40 | GND | GND | Ground pin. |
| 41 | DIF6 | OUT | Differential true clock output |
| 42 | DIF6# | OUT | Differential Complementary clock output |
| 43 | vOE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 44 | DIF7 | OUT | Differential true clock output |
| 45 | DIF7# | OUT | Differential Complementary clock output |
| 46 | vOE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs |
| 47 | VDDIO | PWR | Power supply for differential outputs |
| 48 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 49 | epad | GND | Connect epad to ground |

## Test Loads




**L = 5 inches**

## Alternate Terminations

The 9DBV family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with "Universal" Low-Power HCSL Outputs" for details.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV0841. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| 1.8V Supply Voltage | VDDxx | Applies to VDD, VDDA and VDDIO | -0.5 | | 2.5 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$+0.5V | V | 1, 3 |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins | | | 3.6V | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

## Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common Mode Input Voltage | 150 | | 1000 | mV | 1 |
| Input Swing - DIF_IN | $V_{SWING}$ | Differential value | 300 | | | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero.

# Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.7 | 1.8 | 1.9 | V | |
| Output Supply Voltage | VDDIO | Supply voltage for Low Power HCSL Outputs | 0.9975 | 1.05 | 1.9 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commercial range | 0 | 25 | 70 | °C | |
| | | Industrial range | -40 | 25 | 85 | °C | |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus | 0.75 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Single-ended tri-level inputs ('_tri' suffix) | 0.4 $V_{DD}$ | | 0.6 $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus | -0.3 | | 0.25 $V_{DD}$ | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | uA | |
| | $I_{INP}$ | Single-ended inputs<br>$V_{IN}$ = 0 V; Inputs with internal pull-up resistors<br>$V_{IN}$ = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | $F_{ibyp}$ | Bypass mode | 1 | | 200 | MHz | 2 |
| | $F_{ipll}$ | 100MHz PLL mode | 60 | 100.00 | 140 | MHz | 2 |
| | $F_{ipll}$ | 125MHz PLL mode | 75 | 125.00 | 175 | MHz | 2 |
| | $F_{ipll}$ | 50MHz PLL mode | 30 | 50.00 | 65 | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,5 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.6 | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | $f_{MODIN}$ | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of single-ended control inputs | | | | ns | 2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | $V_{DDSMB}$ = 3.3V, see note 4 for $V_{DDSMB}$ < 3.3V | | | 0.6 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | $V_{DDSMB}$ = 3.3V, see note 5 for $V_{DDSMB}$ < 3.3V | 2.1 | | 3.6 | V | 4 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | @ $V_{OL}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | Bus Voltage | 1.7 | | 3.6 | V | |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are > 200 mV.

[4] For $V_{DDSMB}$ < 3.3V, $V_{IHSMB}$ > = 0.8x$V_{DDSMB}$.

[5]DIF_IN input.

[6]The differential input clock must be running for the SMBus to be active.

## Electrical Characteristics–Low Power HCSL Outputs

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | dV/dt | Scope averaging on, fast setting | 1.7 | 2.8 | 4 | V/ns | 1,2,3 |
| | dV/dt | Scope averaging on, slow setting | 1.1 | 2.1 | 3.2 | V/ns | 1,2,3 |
| Slew rate matching | ΔdV/dt | Slew rate matching, Scope averaging on | | 6.2 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 789 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | 38 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 803 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | 15 | | | 7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 417 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 13 | 140 | mV | 1,6 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Electrical Characteristics–Current Consumption

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDA}$ | VDDA+VDDR, PLL Mode, @100MHz | | 10.6 | 15 | mA | 1 |
| | $I_{DD}$ | VDD, All outputs active @100MHz | | 6.1 | 10 | mA | 1 |
| | $I_{DDO}$ | VDDO, All outputs active @100MHz | | 30.7 | 35 | mA | 1 |
| Powerdown Current | $I_{DDAPD}$ | VDDA+VDDR, PLL Mode, @100MHz | | 0.58 | 1 | mA | 1, 2 |
| | $I_{DDPD}$ | VDD, Outputs Low/Low | | 0.81 | 2 | mA | 1, 2 |
| | $I_{DDOPD}$ | VDDO, Outputs Low/Low | | 0.00 | 0.01 | mA | 1, 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = $T_{AMB}$, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 2.7 | 4 | MHz | 1,5 |
| | | -3dB point in Low BW Mode | 1 | 1.4 | 2 | MHz | 1,5 |
| PLL Jitter Peaking | $t_{JPEAK}$ | Peak Pass band Gain | | 1.1 | 2 | dB | 1 |
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode | 45 | 50.1 | 55 | % | 1 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, Bypass Mode @100MHz | -1 | 0.03 | 1 | % | 1,3 |
| Skew, Input to Output | $t_{pdBYP}$ | Bypass Mode, $V_T$ = 50% | 2800 | 3625 | 4500 | ps | 1 |
| | $t_{pdPLL}$ | PLL Mode $V_T$ = 50% | -100 | -4 | 100 | ps | 1,4 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | 39 | 50 | ps | 1,4 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode | | 14 | 50 | ps | 1,2 |
| | | *Additive* Jitter in Bypass Mode | | 0.10 | 25 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

## Electrical Characteristics–Phase Jitter Parameters – 12kHz to 20MHz

$T_{AMB}$ = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| 12k-20M *Additive* Phase Jitter, Fan-out Buffer Mode | $t_{jph12k-20MFOB}$ | Fan-out Buffer Mode, SSC OFF, 156.25MHz | | 156 | | n/a | fs (rms) | 1, 2, 3 |

Notes:

1. Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details.
2. 12kHz to 20MHz brick wall filter.
3. For RMS values additive jitter is calculated by solving for b where [$b = sqrt(c^2 - a^2)$], a is rms input jitter and c is rms total jitter.

## Electrical Characteristics–Additive PCIe Phase Jitter for Fanout Buffer Mode[7]

$T_{AMB}$ = over the specified operating range. Supply Voltages per normal operation conditions. See Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive PCIe Phase Jitter, Fan-out Buffer Mode (Common Clocked Architecture) | $t_{jphPCIeG1-CC}$ | PCIe Gen 1 (2.5 GT/s) | | 1.7 | 3.0 | 86 | ps (p-p) | 1, 2 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen 2 Hi Band (5.0 GT/s) | | 0.033 | 0.049 | 3 | ps (RMS) | 1, 2 |
| | | PCIe Gen 2 Lo Band (5.0 GT/s) | | 0.122 | 0.199 | 3.1 | ps (RMS) | 1, 2 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen 3 (8.0 GT/s) | | 0.059 | 0.098 | 1 | ps (RMS) | 1, 2 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen 4 (16.0 GT/s) | | 0.059 | 0.098 | 0.5 | ps (RMS) | 1, 2, 3, 4 |
| | $t_{jphPCIeG5-CC}$ | PCIe Gen 5 (32.0 GT/s) | | 0.023 | 0.038 | 0.15 | ps (RMS) | 1, 2, 3, 5 |
| Additive PCIe Phase Jitter, Fan-out Buffer Mode (SRIS Architecture) | $t_{jphPCIeG1-SRIS}$ | PCIe Gen 1 (2.5 GT/s) | | 0.175 | 0.038 | n/a | ps (RMS) | 1, 2, 6 |
| | $t_{jphPCIeG2-SRIS}$ | PCIe Gen 2 (5.0 GT/s) | | 0.156 | 0.275 | n/a | ps (RMS) | 1, 2, 6 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen 3 (8.0 GT/s) | | 0.041 | 0.247 | n/a | ps (RMS) | 1, 2, 6 |
| | $t_{jphPCIeG4-SRIS}$ | PCIe Gen 4 (16.0 GT/s) | | 0.043 | 0.064 | n/a | ps (RMS) | 1, 2, 6 |
| | $t_{jphPCIeG5-SRIS}$ | PCIe Gen 5 (32.0 GT/s) | | 0.036 | 0.066 | n/a | ps (RMS) | 1, 2, 6 |

Notes:

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. If oscilloscope data is used, equipment noise is removed from all results.

2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results the RTO result must be used.

3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.

5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.

6. The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. And additional consideration is the value for which to divide by √2. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by √2, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/√2 = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/√2 = 0.5ps RMS if the clock chip is near the clock input.

7. Additive jitter for RMS values is calculated by solving for b where $b = \sqrt{(c^2 - a^2)}$, and a is rms input jitter and c is rms output jitter.

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| Controller (Host) | | | Renesas (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Note**: SMBus Address is Latched on SADR pin.

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| Controller (Host) | | | Renesas |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Output Enable Register** [1]

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | DIF OE7 | Output Enable | RW | Low/Low | OE7# control | 1 |
| **Bit 6** | DIF OE6 | Output Enable | RW | Low/Low | OE6# control | 1 |
| **Bit 5** | DIF OE5 | Output Enable | RW | Low/Low | OE5# control | 1 |
| **Bit 4** | DIF OE4 | Output Enable | RW | Low/Low | OE4# control | 1 |
| **Bit 3** | DIF OE3 | Output Enable | RW | Low/Low | OE3# control | 1 |
| **Bit 2** | DIF OE2 | Output Enable | RW | Low/Low | OE2# control | 1 |
| **Bit 1** | DIF OE1 | Output Enable | RW | Low/Low | OE1# control | 1 |
| **Bit 0** | DIF OE0 | Output Enable | RW | Low/Low | OE0# control | 1 |

1. A low on these bits will override the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | PLLMODERB1 | PLL Mode Readback Bit 1 | **R** | See PLL Operating Mode Table | | Latch |
| **Bit 6** | PLLMODERB0 | PLL Mode Readback Bit 0 | **R** | | | Latch |
| **Bit 5** | PLLMODE_SWCNTRL | Enable SW control of PLL Mode | RW | Values in B1[7:6] set PLL Mode | Values in B1[4:3] set PLL Mode | 0 |
| **Bit 4** | PLLMODE1 | PLL Mode Control Bit 1 | RW[1] | See PLL Operating Mode Table | | 0 |
| **Bit 3** | PLLMODE0 | PLL Mode Control Bit 0 | RW[1] | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.6V | 01 = 0.7V | 1 |
| **Bit 0** | AMPLITUDE 0 | | RW | 10= 0.8V | 11 = 0.9V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW | Slow setting | Fast setting | 1 |
| **Bit 6** | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW | Slow setting | Fast setting | 1 |
| **Bit 5** | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW | Slow setting | Fast setting | 1 |
| **Bit 4** | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow setting | Fast setting | 1 |
| **Bit 3** | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | Slow setting | Fast setting | 1 |
| **Bit 2** | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | Slow setting | Fast setting | 1 |
| **Bit 1** | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow setting | Fast setting | 1 |
| **Bit 0** | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow setting | Fast setting | 1 |

**SMBus Table: Frequency Select Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 1 |
| **Bit 6** | Reserved | | | | | 1 |
| **Bit 5** | FREQ_SEL_EN | Enable SW selection of frequency | RW | SW frequency change disabled | SW frequency change enabled | 0 |
| **Bit 4** | FSEL1 | Freq. Select Bit 1 | RW[1] | See Frequency Select Table | | 0 |
| **Bit 3** | FSEL0 | Freq. Select Bit 0 | RW[1] | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | Reserved | | | | | 1 |
| **Bit 0** | SLEWRATESEL FB | Adjust Slew Rate of FB | RW | Slow setting | Fast setting | 1 |

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

**Byte 4 is Reserved and reads back 'hFF**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | RID3 | Revision ID | **R** | A rev = 0000 | | 0 |
| **Bit 6** | RID2 | | **R** | | | 0 |
| **Bit 5** | RID1 | | **R** | | | 0 |
| **Bit 4** | RID0 | | **R** | | | 0 |
| **Bit 3** | VID3 | VENDOR ID | **R** | 0001 = IDT | | 0 |
| **Bit 2** | VID2 | | **R** | | | 0 |
| **Bit 1** | VID1 | | **R** | | | 0 |
| **Bit 0** | VID0 | | **R** | | | 1 |

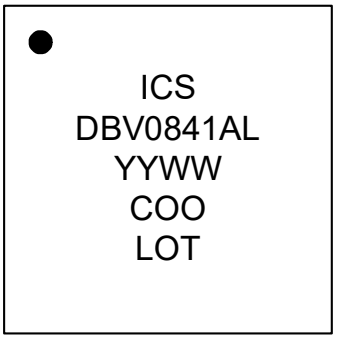
**SMBus Table: Device Type/Device ID**

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Device Type1 | Device Type | **R** | 00 = FGx, 01 = DBx, 10 = DMx, 11= Reserved | | 0 |
| **Bit 6** | Device Type0 | | **R** | | | 1 |
| **Bit 5** | Device ID5 | Device ID | **R** | 001000 binary or 08 hex | | 0 |
| **Bit 4** | Device ID4 | | **R** | | | 0 |
| **Bit 3** | Device ID3 | | **R** | | | 1 |
| **Bit 2** | Device ID2 | | **R** | | | 0 |
| **Bit 1** | Device ID1 | | **R** | | | 0 |
| **Bit 0** | Device ID0 | | **R** | | | 0 |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 0 |
| **Bit 6** | Reserved | | | | | 0 |
| **Bit 5** | Reserved | | | | | 0 |
| **Bit 4** | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| **Bit 3** | BC3 | | RW | | | 1 |
| **Bit 2** | BC2 | | RW | | | 0 |
| **Bit 1** | BC1 | | RW | | | 0 |
| **Bit 0** | BC0 | | RW | | | 0 |

## Marking Diagrams





Notes:
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.

## Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to Case | NDG48 | 33 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to Base | | 2.1 | °C/W | 1 |
| | $\theta_{JA0\theta}$ | Junction to Air, still air | | 37 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow | | 30 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow | | 27 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow | | 26 | °C/W | 1 |

[1]ePad soldered to board

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

48-VFQFPN (NDG48P1)

## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DBV0841AKLF | Trays | 48-pin VFQFPN | 0 to +70° C |
| 9DBV0841AKLFT | Tape and Reel | 48-pin VFQFPN | 0 to +70° C |
| 9DBV0841AKILF | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBV0841AKILFT | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |

**“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

**“A” is the device revision designator (will not correlate with the datasheet revision).**

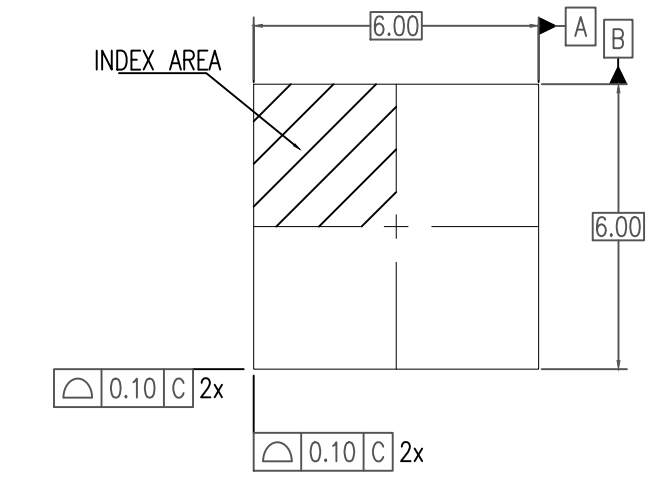
## Revision History

| Revision Date | Description |
|---|---|
| August 13, 2012 | 1. Removed "Differential" from DS title and Recommended Application, corrected typo's in Description. Updated block diagram to show integrated terminations.<br>2. Removed references to 60KOhm pulldown under pinout.<br>3. Updated "Phase Jitter Parameters" table by adding "Industry Limit" column and updated all Electrical Tables with characterization data.<br>4. Updated Byte3[0] to be consistent with Byte 2. Updated Byte6[7:6] definition.<br>5. Updated Mark spec with correct part revision (A) and added thermal data to page 13.<br>6. Added NDG48 to "Package Outline and Package Dimensions" on page 14 and updated Ordering information to correct part revision (A rev).<br>7. Move to final |
| February 18, 2013 | 1. Changed VIH min. from 0.65*VDD to 0.75*VDD<br>2. Changed VIL max. from 0.35*VDD to 0.25*VDD<br>3. Added missing mid-level input voltage spec (VIM) of 0.4*VDD to 0.6*VDD. |
| August 12, 2014 | Changed package designator from "MLF" to "VFQFPN" |
| March 10, 2016 | 1. Numerous typographical and grammatical updates for document consistency with other devices in the family, including updated descriptions for Bytes 0 and 2.<br>2. Fast and slow slew rates were swapped in the "DIF 0.7V Low Power HCSL Outputs" table.<br>3. Changed PCIe clock source from 9FG432 to 9FGV0841/9FGL0841 for PLL mode phase jitter numbers. New phase jitter numbers are lower.<br>4. Added epad to pinout diagram and pin descriptions.<br>5. Updated Clock Input Parameters to be consistent with PCIe Vswing parameter.<br>6. Updated package drawing to latest format. |
| April 28, 2016 | 1. Updated max frequency of 100MHz PLL mode to 140MHz<br>2. Updated max frequency of 125MHz PLL mode to 175MHz<br>3. Updated max frequency of 50MHz PLL mode to 65MHz |
| August 28, 2019 | Updated to PCIe Gen4. |
| July 27, 2021 | 1. Added new Electrical Characteristics–Phase Jitter Parameters tables.<br>2. Updated datasheet title.<br>3. Updated Key Specifications.<br>4. Updated Package Outline Drawings section. |

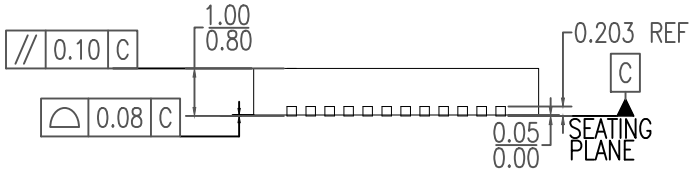
# 48-VFQFPN Package Outline Drawing

6.0 x 6.0 x 0.90 mm Body, Epad 4.1x 4.1 mm, 0.40mm Pitch

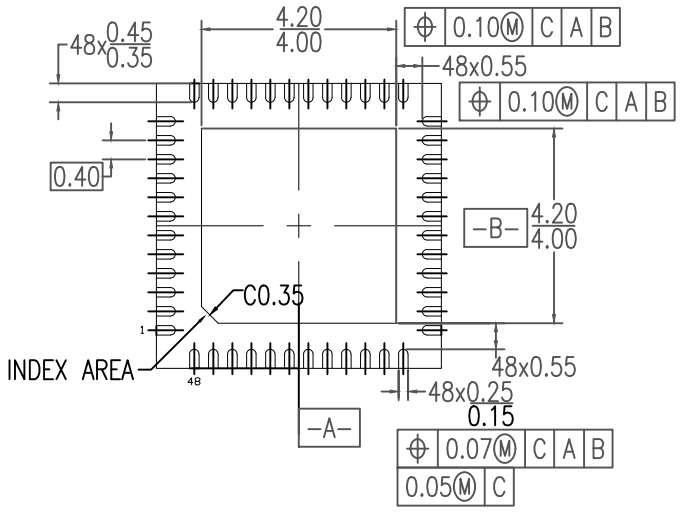
NDG48P1, PSC-4212-01, Rev 01, Page 1




TOP VIEW



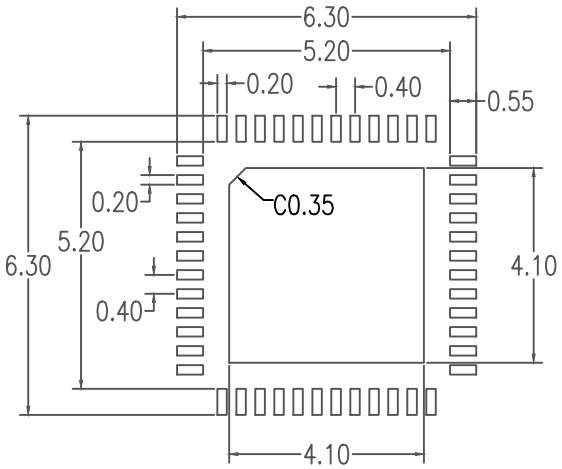

SIDE VIEW




BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.




RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| Aug16, 2018 | Rev 01 | New Format Change QFN to VFQFPN, Recalculate Land Pattern |
| May 6, 2016 | Rev 00 | Add Chamfer |