## Description

The 9DML2855 is a 2-input, 8-output clock multiplexer supporting PCIe Gen5 and DB2000Q applications. It supports today's complex system power sequencing requirements with Power Down Tolerant and Flexible Power Sequencing features. An OE# pin for each output supports PCIe CLKREQ# functionality.

## Typical Applications

- Servers
- Enterprise SSDs
- Networking
- Accelerators

## Key Specifications

- Output-to-output skew: < 50ps
- Additive phase jitter:
  - PCIe Gen5 < 20fs RMS
  - 12kHz to 20MHz at 156.25MHz < 100fs RMS
  - DB2000Q < 30fs RMS
  - IF-UPI < 125fs RMS
- Backwards compatible to PCIe Gen1–4

## Features

- Flexible Power Sequencing (FPS) ensures good behavior when powered up without input clock
- Power-Down Tolerant Input (PDT) inputs: SEL_A_B#, SADR0_tri, OE# pins
- Integrated terminations eliminate 32 resistors, saving 62mm$^2$ of area
- 8 OE# pins; hardware control of each output. SMBus control also available
- 3 selectable SMBus addresses
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- Maximum operating frequency of 400MHz
- 6 × 6 mm 48-VFQFPN package

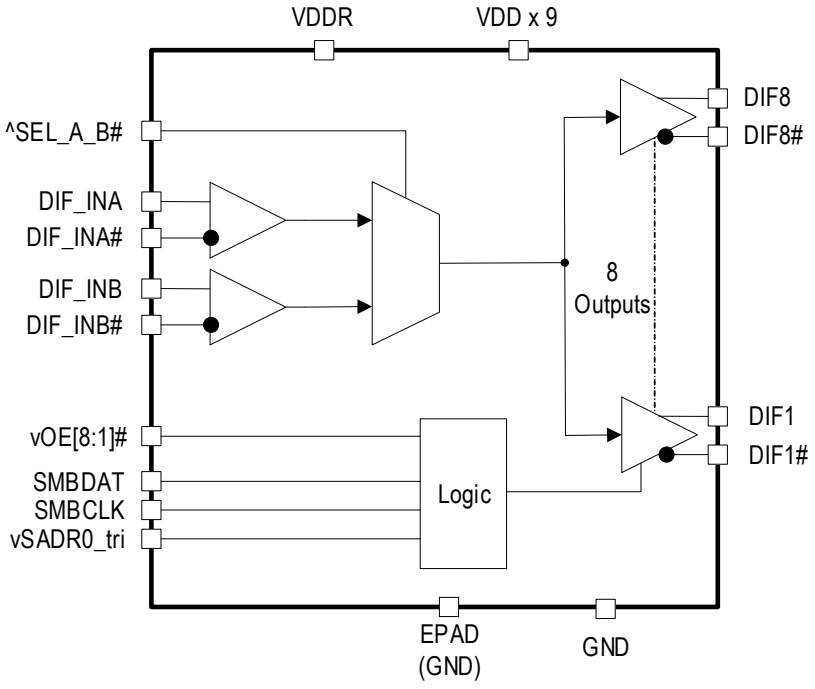
## Output Features

- 8 Low-Power HCSL (LP-HCSL) output pairs with 85Ω Zout

## PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without Spread Spectrum (SRNS, SRIS)

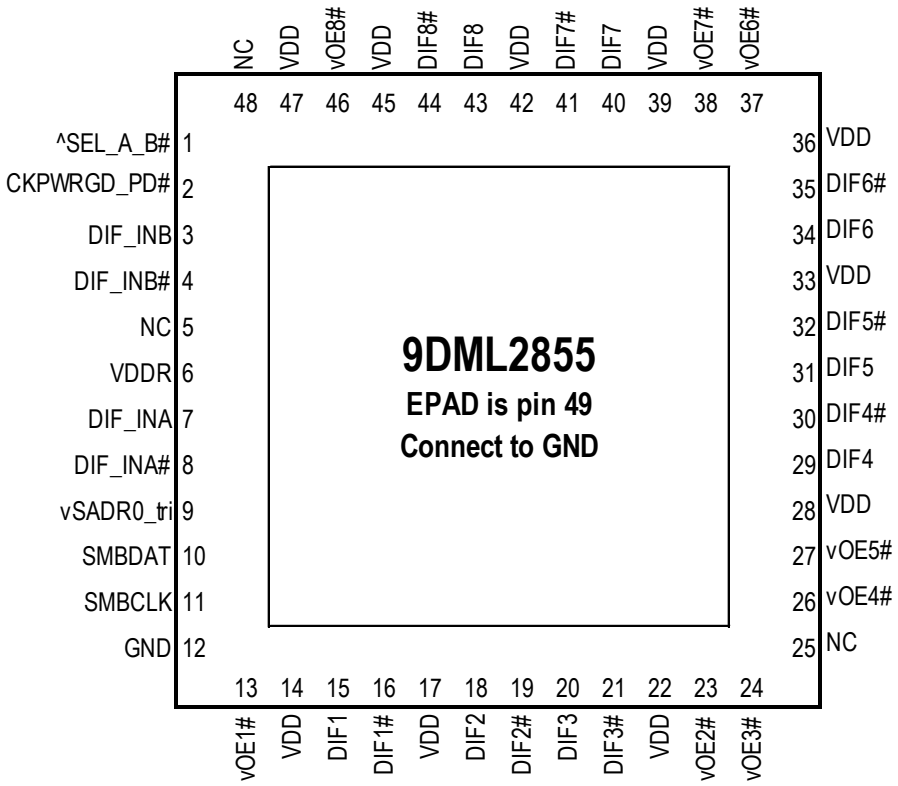
## Block Diagram



# Contents

## Pin Assignments

Figure 1. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View



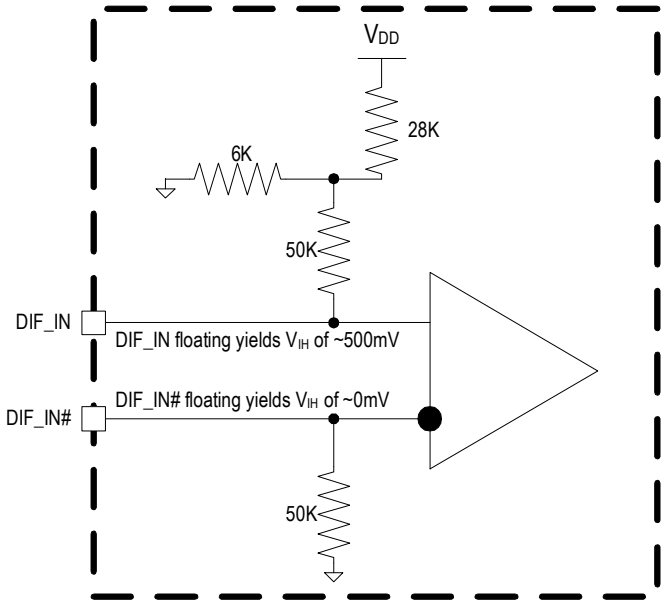

**48-VFQFPN, 6mm x 6mm, 0.4mm pitch**

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

## Input Clock Bias Network

Figure 2. Input Clock Bias Network



# Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | ^SEL_A_B# | Input | Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor.<br>0 = Input B selected, 1 = Input A selected. |
| 2 | CKPWRGD_PD# | Input | 3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 3 | DIF_INB | Input | True input of differential clock |
| 4 | DIF_INB# | Input | Complement input of differential clock. |
| 5 | NC | — | No connection. |
| 6 | VDDR | Power | Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V. |
| 7 | DIF_INA | Input | True input of differential clock |
| 8 | DIF_INA# | Input | Complement input of differential clock |
| 9 | vSADR0_tri | Input | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal pull-down resistor. See the SMBus Addressing table. |
| 10 | SMBDAT | I/O | Data pin of SMBus circuitry. |
| 11 | SMBCLK | Input | Clock pin of SMBus circuitry. |
| 12 | GND | GND | Ground pin. |
| 13 | vOE1# | Input | Active low input for enabling output 1. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 14 | VDD | Power | Power supply, nominally 3.3V. |
| 15 | DIF1 | Output | Differential true clock output. |
| 16 | DIF1# | Output | Differential complementary clock output. |
| 17 | VDD | Power | Power supply, nominally 3.3V. |
| 18 | DIF2 | Output | Differential true clock output. |
| 19 | DIF2# | Output | Differential complementary clock output. |
| 20 | DIF3 | Output | Differential true clock output. |
| 21 | DIF3# | Output | Differential complementary clock output. |
| 22 | VDD | Power | Power supply, nominally 3.3V. |
| 23 | vOE2# | Input | Active low input for enabling output 2. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 24 | vOE3# | Input | Active low input for enabling output 3. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 25 | NC | — | No connection. |
| 26 | vOE4# | Input | Active low input for enabling output 4. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |

Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 27 | vOE5# | Input | Active low input for enabling output 5. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 28 | VDD | Power | Power supply, nominally 3.3V. |
| 29 | DIF4 | Output | Differential true clock output. |
| 30 | DIF4# | Output | Differential complementary clock output. |
| 31 | DIF5 | Output | Differential true clock output. |
| 32 | DIF5# | Output | Differential complementary clock output. |
| 33 | VDD | Power | Power supply, nominally 3.3V. |
| 34 | DIF6 | Output | Differential true clock output. |
| 35 | DIF6# | Output | Differential complementary clock output. |
| 36 | VDD | Power | Power supply, nominally 3.3V. |
| 37 | vOE6# | Input | Active low input for enabling output 6. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 38 | vOE7# | Input | Active low input for enabling output 7. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 39 | VDD | Power | Power supply, nominally 3.3V. |
| 40 | DIF7 | Output | Differential true clock output. |
| 41 | DIF7# | Output | Differential complementary clock output. |
| 42 | VDD | Power | Power supply, nominally 3.3V. |
| 43 | DIF8 | Output | Differential true clock output. |
| 44 | DIF8# | Output | Differential complementary clock output. |
| 45 | VDD | Power | Power supply, nominally 3.3V. |
| 46 | vOE8# | Input | Active low input for enabling output 8. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output. |
| 47 | VDD | Power | Power supply, nominally 3.3V. |
| 48 | NC | — | No connection. |
| 49 | EPAD | Power | Ground. |

# Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DML2855 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Storage Temperature | Ts | | -65 | | 3.9 | V | 1,2 |
| Input Low Voltage | $V_{IL}$ | | GND-0.5 | | | V | 1 |
| Input High Voltage | $V_{IH}$ | Except for SMBus interface. | | | $V_{DD}$+0.5 | V | 1,3 |
| Input High Voltage | $V_{IHSMB}$ | SMBus clock and data pins. | | | 3.9 | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model. | 2000 | | | V | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

# Electrical Characteristics

Over specified temperature and voltage ranges unless otherwise indicated. See Test Loads for loading conditions.

Table 3. SMBus Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.8 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | | 2.1 | | $V_{DDSMB}$ | V | |
| SMBus Output Low Voltage | $V_{OLSMB}$ | At $I_{PULLUP}$. | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | At $V_{OL}$. | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | | 2.7 | | 3.6 | V | 1 |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max $V_{IL}$ - 0.15V) to (Min $V_{IH}$ + 0.15V). | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min $V_{IH}$ + 0.15V) to (Max $V_{IL}$ - 0.15V). | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MaxSMB}$ | Maximum SMBus operating frequency. | | | 400 | kHz | 4 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200 mV.

[4] The selected differential input clock must be running for the SMBus to be active.

Table 4. Input/Supply/Common Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DDx}$ | Supply voltage for core and analog. | 3.135 | 3.3 | 3.465 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Industrial range. | -40 | | 85 | °C | |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus, tri-level inputs. | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus, tri-level inputs. | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | Tri-Level inputs (_tri suffix). | 2.2 | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Tri-Level inputs (_tri suffix). | 1.2 | $V_{DD}/2$ | 1.8 | V | |
| Input Low Voltage | $V_{IL}$ | Tri-Level inputs (_tri suffix). | GND - 0.3 | | 0.8 | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = $V_{DD}$. | -5 | | 5 | µA | |
| | $I_{INP}$ | Single-ended inputs.<br>$V_{IN}$ = 0 V; Inputs with internal pull-up resistors.<br>$V_{IN}$ = VDD; Inputs with internal pull-down resistors. | -100 | | 100 | µA | |
| Input Frequency | $F_{IN}$ | Input Clock Detect not used, Byte 4, bit 6 = 0 (default). | 1 | | 400 | MHz | |
| | $F_{IN}$ | Input Clock Detect used, Byte 4, bit 6 = 1. | 25 | | 400 | MHz | |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN. | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs. | 1.5 | | 2.7 | pF | 1,4 |
| | $C_{OUT}$ | Output pin capacitance. | | | 6 | pF | 1 |
| Clk Stabilization | $t_{STAB}$ | From $V_{DD}$ power-up and after input clock stabilization or de-assertion of PD# to 1st clock. | | 1 | 1.8 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable frequency for PCIe applications. (Triangular Modulation) | 30 | 31.6 | 33 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion.<br>DIF stop after OE# deassertion. | 4 | 5 | 10 | clocks | 1,2,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion. | | 85 | 300 | µs | 1,3 |
| Tfall | $t_F$ | Fall time of control inputs. | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of control inputs. | | | 5 | ns | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV, PLL mode.

[4] DIF_IN input.

Table 5. DIF_IN Clock Input Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input Crossover Voltage | $V_{CROSS}$ | Crossover voltage. | 150 | | 900 | mV | 1 |
| Input Swing – DIF_IN | $V_{SWING}$ | Differential value. | 300 | | | mV | 1 |
| Input Slew Rate – DIF_IN | dv/dt | Measured differentially. | 0.35 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 800mV, $V_{IN}$ = GND. | -200 | | 200 | uA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential waveform. | 45 | | 55 | % | 1 |
| Input Jitter – Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement. | 0 | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 6. DIFn LP-HCSL Outputs

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Slew Rate | dV/dt | Scope averaging on. | 2.3 | 2.8 | 3.5 | 0.6–4 | V/ns | 1,2,3 |
| Slew Rate Matching | ΔdV/dt | Slew rate matching, Scope averaging on. | | 7 | 17 | 20 | % | 1,2,4,7 |
| Maximum Voltage | Vmax | Measurement on single-ended signal using absolute value. (Scope averaging off). | 763 | 825 | 897 | 660–1150 | mV | 7 |
| Minimum Voltage | Vmin | | -90 | -45 | | -300 | | 7 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off. | 344 | 387 | 434 | 250–550 | mV | 1,5,7 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off. | | 15 | 21 | 140 | mV | 1,6,7 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Table 7. Current Consumption

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDx}$ | All other $V_{DD}$ pins, all outputs at 100MHz, $C_L$ = 2pF. | | 50 | 63 | mA | |
| | $I_{DDR}$ | $V_{DDR}$ pins, all outputs at 100MHz, $C_L$ = 2pF. | | 4 | 4 | mA | |
| Powerdown Current | $I_{DDx}$ | All other $V_{DD}$ pins, all outputs Low/Low. | | 4 | 5 | mA | |
| | $I_{DDR}$ | $V_{DDR}$ pins, all outputs at 100MHz, $C_L$ = 2pF. | | 0.8 | 1 | mA | |

Table 8. Skew and Differential Parameters

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| CLK_IN, DIF[x:0] | $t_{PD\_BYP}$ | Input-to-Output Skew, at 100MHz and 156.25MHz, nominal temperature and voltage. | 2.5 | 3.2 | 4.0 | ns | 1,2,3 |
| CLK_IN, DIF[x:0] | $t_{DSPO\_BYP}$ | Input-to-Output Skew Variation, at 100MHz and 156.25MHz, across voltage and temperature, $T_{AMB}$ = 0°C to 70°C, default slew rate. | -250 | 0.0 | 250 | ps | 1,2,3 |
| | | Input-to-Output Skew Variation, at 100MHz and 156.25MHz, across voltage and temperature, $T_{AMB}$ = -40°C to 85°C, default slew rate. | -350 | 0.0 | 350 | ps | 1,2,3,6 |
| DIF[x:0] | $t_{SKEW\_ALL}$ | Output-to-Output Skew across all outputs, at 100MHz and 156.25MHz, default slew rate. | | 19 | 50 | ps | 1,2,3,6 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially at 100MHz and 156.25MHz. | -0.5 | 0.3 | 0.5 | % | 1,7 |

[1] Measured into fixed 2pF load capacitor. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point.

[3] All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] Guaranteed by design and characterization, not 100% tested in production.

[7] Duty cycle distortion is the difference in duty cycle between the output and the input clock in fanout mode.

[8] Measured from differential waveform.

Table 9. Additive PCIe Phase Jitter

$T_{AMB}$ = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive PCIe Phase Jitter (Common Clocked Architecture) | $t_{jphPCIeG1-CC}$ | PCIe Gen1 (2.5 GT/s). | | 1.07 | 1.3 | 86 | ps (p-p) | 1,2 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band (5.0 GT/s). | | 0.02 | 0.022 | 3 | ps (RMS) | 1,2 |
| | | PCIe Gen2 High Band (5.0 GT/s). | | 0.08 | 0.1 | 3.1 | ps (RMS) | 1,2 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen3 (8.0 GT/s). | | 0.04 | 0.05 | 1 | ps (RMS) | 1,2 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen4 (16.0 GT/s). | | 0.04 | 0.05 | 0.5 | ps (RMS) | 1,2,3,4 |
| | $t_{jphPCIeG5-CC}$ | PCIe Gen5 (32.0 GT/s). | | 0.015 | 0.018 | 0.15 | ps (RMS) | 1,2,3,5 |

Table 9. Additive PCIe Phase Jitter (Cont.)

$T_{AMB}$ = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive PCIe Phase Jitter (SRIS Architecture) | $t_{jphPCIeG1-SRIS}$ | PCIe Gen1 (2.5 GT/s). | | 0.58 | 0.82 | N/A | ps (p-p) | 1,2,6 |
| | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 Low Band (5.0 GT/s). | | 0.03 | 0.04 | | ps (RMS) | 1,2,6 |
| | | PCIe Gen2 High Band (5.0 GT/s). | | 0.10 | 0.12 | | ps (RMS) | 1,2,6 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (8.0 GT/s). | | 0.050 | 0.059 | | ps (RMS) | 1,2,6 |
| | $t_{jphPCIeG4-SRIS}$ | PCIe Gen4 (16.0 GT/s). | | 0.050 | 0.059 | | ps (RMS) | 1,2,6 |
| | $t_{jphPCIeG5-SRIS}$ | PCIe Gen5 (32.0 GT/s). | | 0.019 | 0.023 | | ps (RMS) | 1,2,6 |

[1] The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used. Additive jitter for RMS values is calculated by solving for "b" where [ $b = \sqrt{c^2 - a^2}$ ], "a" is rms input jitter and "c" is rms total jitter.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system

[6] While the PCI Express Base specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the N/A in the Limits column.

Table 10. Additive Non-PCIe Phase Jitter

$T_{AMB}$ = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limit | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| Additive DB2000Q Phase Jitter | $t_{jphDB2000Q}$ | DB2000Q filter. | | 23 | 27 | 80 | fs (RMS) | 1,2 |
| Additive 12kHz–20MHz Phase Jitter | $t_{jph12k-20M}$ | 100MHz, includes 1MHz–10MHz IF-UPI | | 108 | 123 | N/A | fs (RMS) | 1,2,3 |
| | | 156.25MHz. | | 89 | 96 | N/A | fs (RMS) | 1,2 |

[1] The REFCLK jitter is measured after applying the filter functions. See the Test Loads section of the data sheet for the exact measurement setup.

[2] Additive jitter for RMS values is calculated by solving for "b" where [ $b = \sqrt{c^2 - a^2}$ ], "a" is rms input jitter and "c" is rms total jitter.

[3] IF-UPI is specified as 1ps RMS maximum over a 1MHz to 10MHz brickwall filter. When the 12kHz to 20MHz value is < 1ps RMS, the IF-UPI specification is also met.

## Power Management

| Inputs | | | Control Bits | | Outputs |
|---|---|---|---|---|---|
| **CKPWRGD_PD#** | **Selected Input Clock (DIF_INx)** | **Output Enable Pin (OEx#)** | **Output Enable Bit (DIFn EN)** | **Input Detect Enable Bit Byte4, bit6** | **DIFn** |
| 0 | X | X | X | X | Low/Low |
| 1 | Running | X | 0 | X | Low/Low |
| | | 1 | X | X | Low/Low |
| | | 0 | 1 | X | Running |
| 1 | Stopped | X | 0 | 0 | Low/Low |
| | | 1 | X | 0 | Low/Low |
| | | 0 | 1 | 0 | DIF_INx |
| 1 | Stopped | X | X | 1 | Low/Low |

x = A or B

n = 1 to 8

## Power Connections

| Pin Number | | Description |
|---|---|---|
| **$V_{DD}$** | **GND** | |
| 6 | 12, 49 (EPAD) | Analog Input |
| 14, 17, 22, 28, 33, 36, 39, 42, 45 | | Output clocks and internal circuits |

# Test Loads

Figure 3. AC/DC Test Load

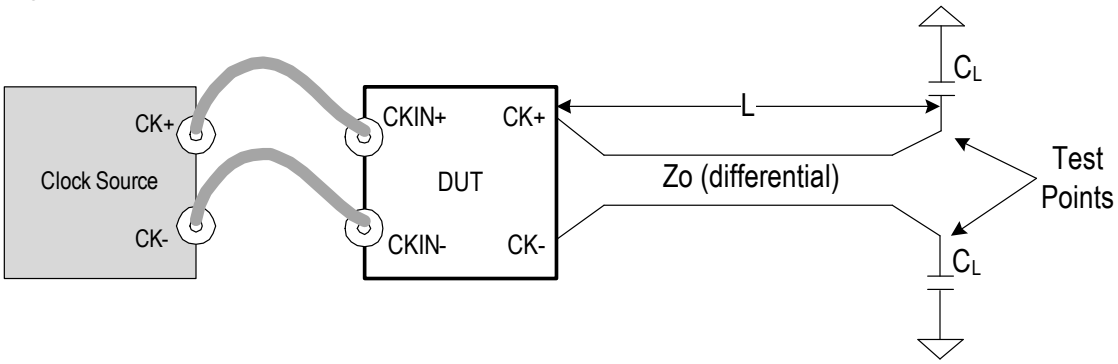



Figure 4. Test Setup for Jitter Measurements

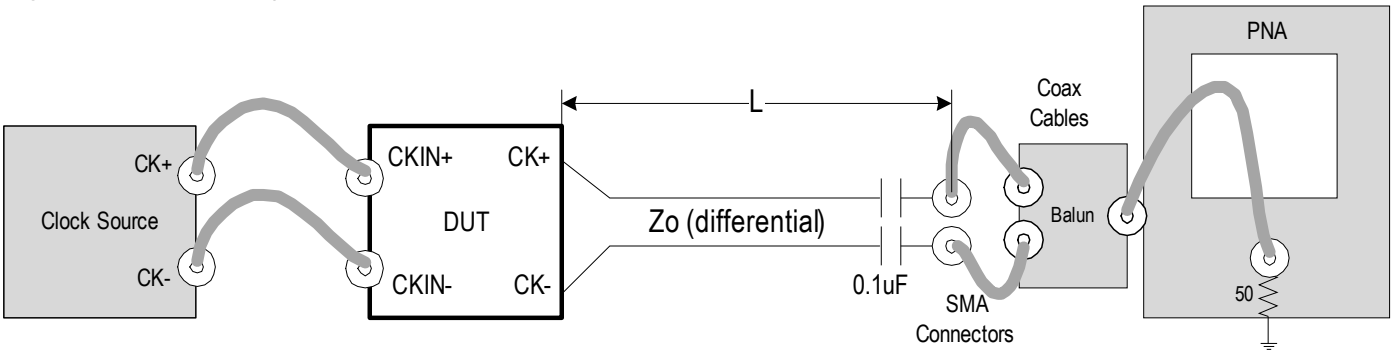



Table 11. Parameters for Output Test Loads

| Clock Source | Rs (Ω) | Zo (Ω) | L (inches) | $C_L$ (pF) | |
|---|---|---|---|---|---|
| SMA100B | Internal | 85 | 5 | 2 | For all measurements except PCIe SRIS. |
| 9FGV1006B | Internal | 85 | 5 | 2 | For PCIe SRIS. |

# Alternate Terminations

The output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for LVPECL, LVDS, CML, and SSTL.

# SMBus Addressing

Table 12. SMBus Addressing

| SMB_A0_tri | SMBus Address (Read/Write bit = 0) |
|---|---|
| 0 | D8 |
| M | DA |
| 1 | DE |

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **Renesas (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0–Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **Renesas (Slave/Receiver)** |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count = X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: PLL Mode and Frequency Select Register**

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved Read Only | | | | | 0 |
| Bit 6 | Reserved Read Only | | | | | 1 |
| Bit 5 | SEL_A_B# | Input Select Readback | R | DIF_INB | DIF_INA | Real Time |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | INP_SEL_SW_EN | Enable S/W control of Input select | RW | Pin Control | SMBus Control | 0 |
| Bit 2 | PLL Mode bit [1] | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 0 |
| Bit 1 | PLL Mode bit [0] | PLL Operating Mode 1 | RW | | | 1 |
| Bit 0 | SEL_A_B# | Input Select control bit | RW | DIF_INB | DIF_INA | 1 |

**SMBus Table: Output Enable Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | DIF6_En | Output Control overrides OE# pin | RW | Low/Low | Pin Control | 1 |
| Bit 5 | DIF5_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | DIF4_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | DIF3_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 2 | DIF2_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 1 | DIF1_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | Reserved | | | | | 0 |

**SMBus Table: Output Enable Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | DIF8_En | Output Control overrides OE# pin | RW | Low/Low | Pin Control | 1 |
| Bit 1 | DIF7_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 0 | Reserved | | | | | 0 |

### SMBus Table: Reserved Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

### SMBus Table: Input_Detect_ReadBack Register

| Byte 4 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Input_Detect_RB | Selected input clock is present | R | Selected Input is not present | Selected input is present | See Notes |
| Bit 6 | Input_Detect_En | Enable or disable Input Detect | RW | Input Detect is Disabled | Input Detect is Enabled | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | Reserved | | | | | 0 |
| Bit 3 | Reserved | | | | | 0 |
| Bit 2 | Reserved | | | | | 0 |
| Bit 1 | Reserved | | | | | 0 |
| Bit 0 | Reserved | | | | | 0 |

Notes on Byte 4:

Clock detect circuit monitors selected input clock (A or B).

Parks the output clocks in a low/low state ~150ns after input clock disappears.

When enabled (Byte 4, bit 6 set to '1'):

- Minimum operating frequency is 25MHz
- Real-time absence or presence of selected input clock may be read back from Byte 4, bit 7

When disabled (Byte 4, bit 6 set to '0' - default):

- Minimum operating frequency is unchanged at 1MHz
- Byte 4, bit 7 reads 0

**SMBus Table: Vendor & Revision ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | RID3 | REVISION ID | R | 1st Revision = 0000 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 0 |
| Bit 3 | VID3 | VENDOR ID | R | IDT/Renesas = 0001 | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

**SMBus Table: Device ID Register**

| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Device ID 7 (MSB) | | R | C5 | | 1 |
| Bit 6 | Device ID 6 | | R | | | 1 |
| Bit 5 | Device ID 5 | | R | | | 0 |
| Bit 4 | Device ID 4 | | R | | | 0 |
| Bit 3 | Device ID 3 | | R | | | 0 |
| Bit 2 | Device ID 2 | | R | | | 1 |
| Bit 1 | Device ID 1 | | R | | | 0 |
| Bit 0 | Device ID 0 | | R | | | 1 |

**SMBus Table: Byte Count Register**

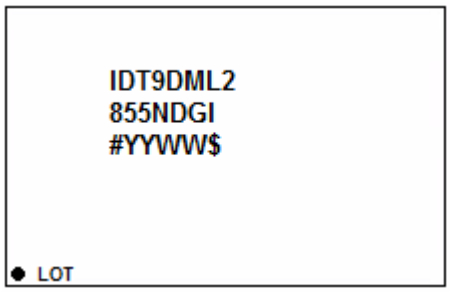
| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| Bit 7 | Reserved | | | | | 0 |
| Bit 6 | Reserved | | | | | 0 |
| Bit 5 | Reserved | | | | | 0 |
| Bit 4 | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 0 |
| Bit 1 | BC1 | | RW | | | 0 |
| Bit 0 | BC0 | | RW | | | 0 |

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

## Marking Diagram




- Lines 1 and 2: part number
- Line 3:
  - "#" denotes the stepping sequence number.
  - "YYWW" denotes the last two digits of the year and work-week the part was assembled.
  - "$" denotes mark code.
- "LOT" denotes lot number.

## Ordering Information

| Orderable Part Number | Differential Output Impedance (Ω) | Package | Carrier Type | Temperature |
|---|---|---|---|---|
| 9DML2855NDGI | 85 | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Trays | -40° to +85°C |
| 9DML2855NDGI8 | 85 | 6 × 6 mm, 0.4mm pitch 48-VFQFPN | Reel | -40° to +85°C |

"G" designates PB-free configuration, RoHS compliant.

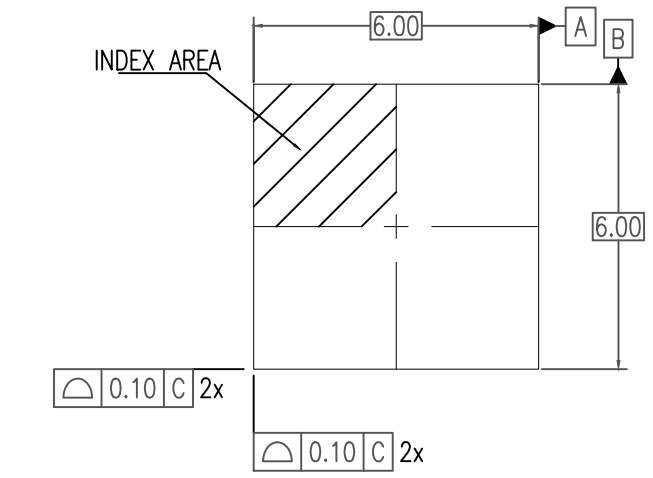
## Revision History

| Revision Date | Description of Change |
|---|---|
| March 16, 2020 | ▪ Updated CLK Stabilization (tSTAB) typical value.<br>▪ Added DIF_IN Clock Input Parameters table.<br>▪ Updated conditions in the Skew and Differential Parameters table. |
| January 14, 2020 | ▪ Updated electrical tables with characterization data.<br>▪ Fill-in TBD in test loads table and Device ID register.<br>▪ Move to final. |
| July 29, 2019 | Initial release. |

# 48-VFQFPN Package Outline Drawing

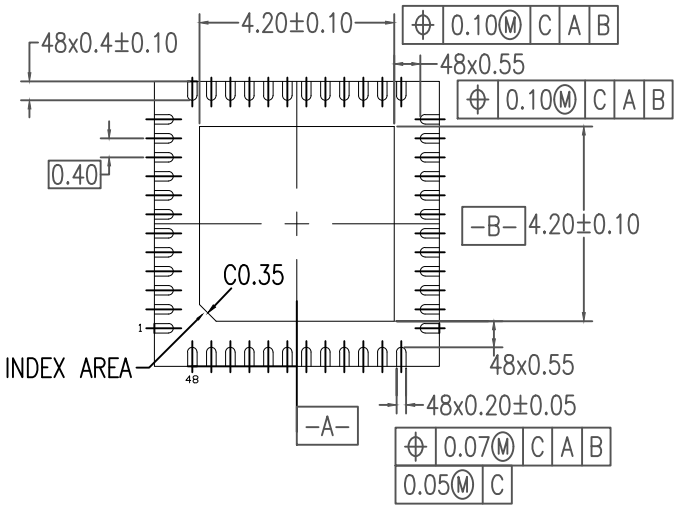
6.0 x 6.0 x 0.90 mm Body, Epad 4.2 x 4.2 mm, 0.40mm Pitch

NDG48P2, PSC-4212-02, Rev 03, Page 1




TOP VIEW

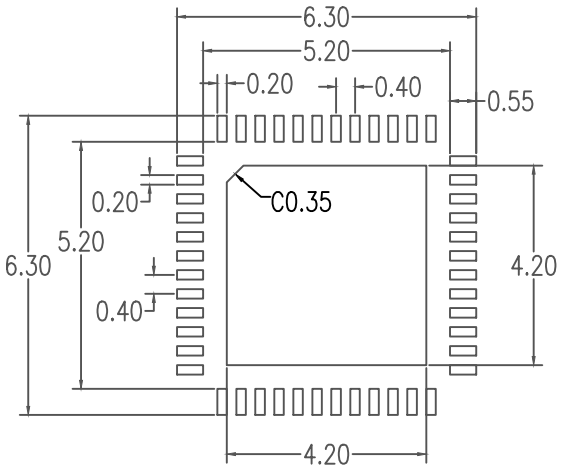

SIDE VIEW




BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.




RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|---|---|---|
| Date Created | Rev No. | Description |
| July 24, 2018 | Rev 02 | New Format Change QFN to VFQFPN, Recalculate Land Pattern |
| Feb 25, 2020 | Rev 03 | Tolerance Format Change |