

9FGL02x1/04x1/06x1/08x1D

3.3V PCIe Gen1-5 Clock Generator Family

The 9FGL02x1/04x1/06x1/08x1D devices comprise a family of 3.3V PCIe Gen1-5 clock generators. There are 2, 4, 6, and 8 outputs versions available and each differential output has a dedicated OE# pin supporting PCIe CLKREQ# functionality.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

Applications

- Servers/High-Performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

Output Features

- 2, 4, 6, or 8 100MHz PCIe output pairs
- One 3.3V LVCMOS REF output with Wake-On-LAN (WOL) support
- See AN-891 for easy AC-coupling to other logic families

Key Specifications

- 90fs RMS typical jitter (PCIe Gen5 CC)
- < 50ps cycle-to-cycle jitter on differential outputs
- < 50ps output-to-output skew on differential outputs
- ±0ppm synthesis error on differential outputs

Features

- Integrated terminations for 100Ω and 85Ω systems save 4 resistors per output
- 112–206 mW typical power consumption (at 3.3V)
- VDDIO rail allows 35% power savings at optional 1.05V (9FGL06 and 9FGL08 only)
- Devices contain default configuration; SMBus not required
- SMBus-selectable features allows optimization to customer requirements:
 - Input polarity and pull-up/pull-downs
 - Output slew rate and amplitude
 - Output impedance (85Ω or 100Ω) for each output
- Contact factory for custom default configurations
- 25MHz input frequency
- OE# pins support PCIe CLKREQ# function
- Pin-selectable SRnS 0%, CC 0% and CC/SRIS - 0.5% spread
- SMBus-selectable CC/SRIS -0.25% spread
- Clean switching between the CC/SRIS spread settings
- DIF outputs blocked until PLL is locked; clean system start-up
- 2 selectable SMBus addresses
- Space saving packages:
 - 4 × 4 mm 24-VFQFPN (9FGL02x1D)
 - 5 × 5 mm 32-VFQFPN (9FGL04x1D)
 - 5 × 5 mm 40-VFQFPN (9FGL06x1D)
 - 6 × 6 mm 48-VFQFPN (9FGL08x1D)

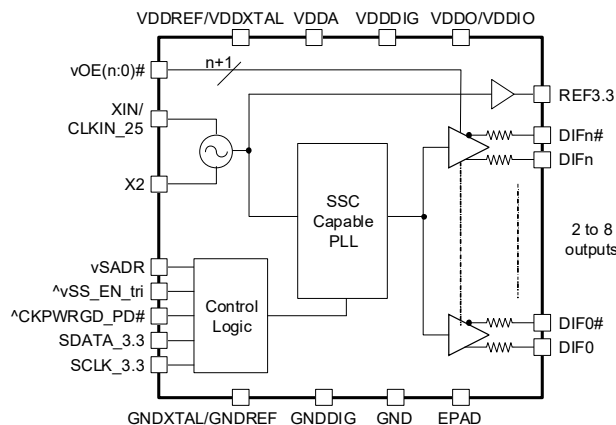
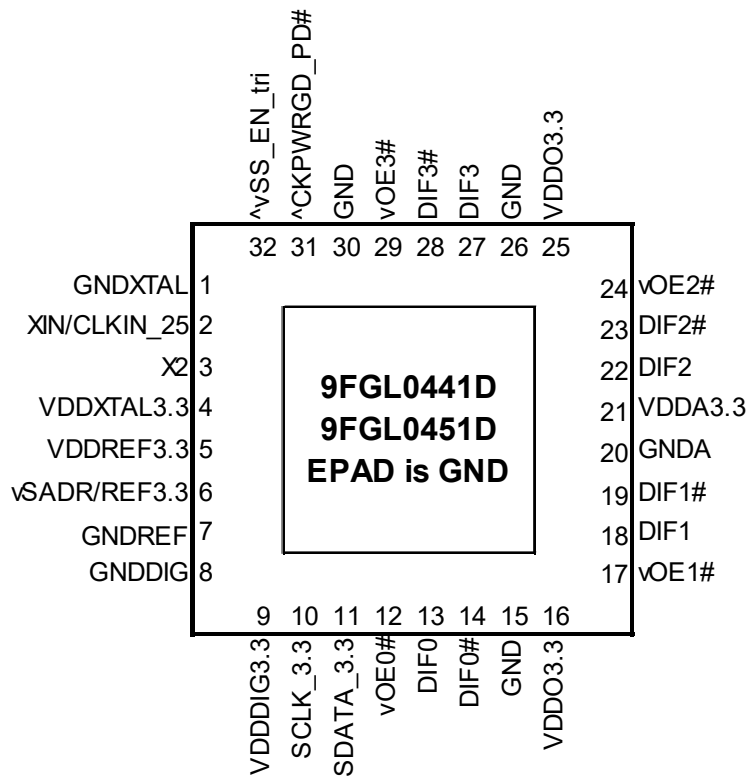


Figure 1. Block Diagram

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1.2 9FGL04x1D Pin Assignments



32-VFQFPN, 5 x 5 mm, 0.5mm pitch

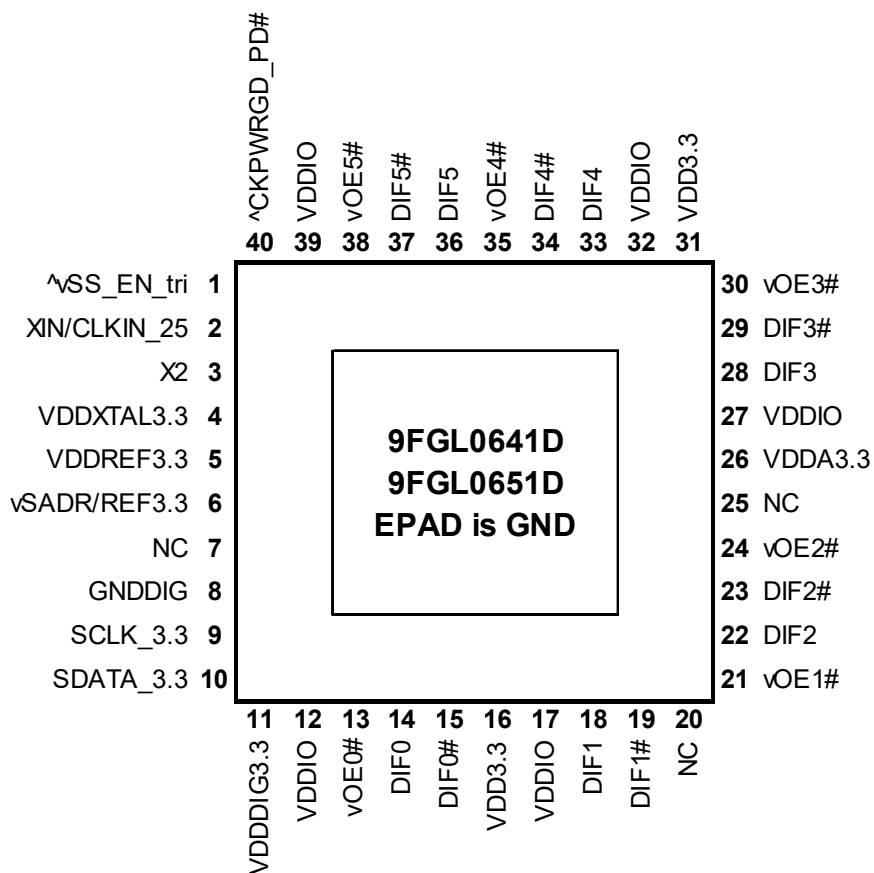
^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistors

Figure 3. 5 x 5 mm 32-VFQFPN Package – Top View

1.3 9FGL06x1D Pin Assignments

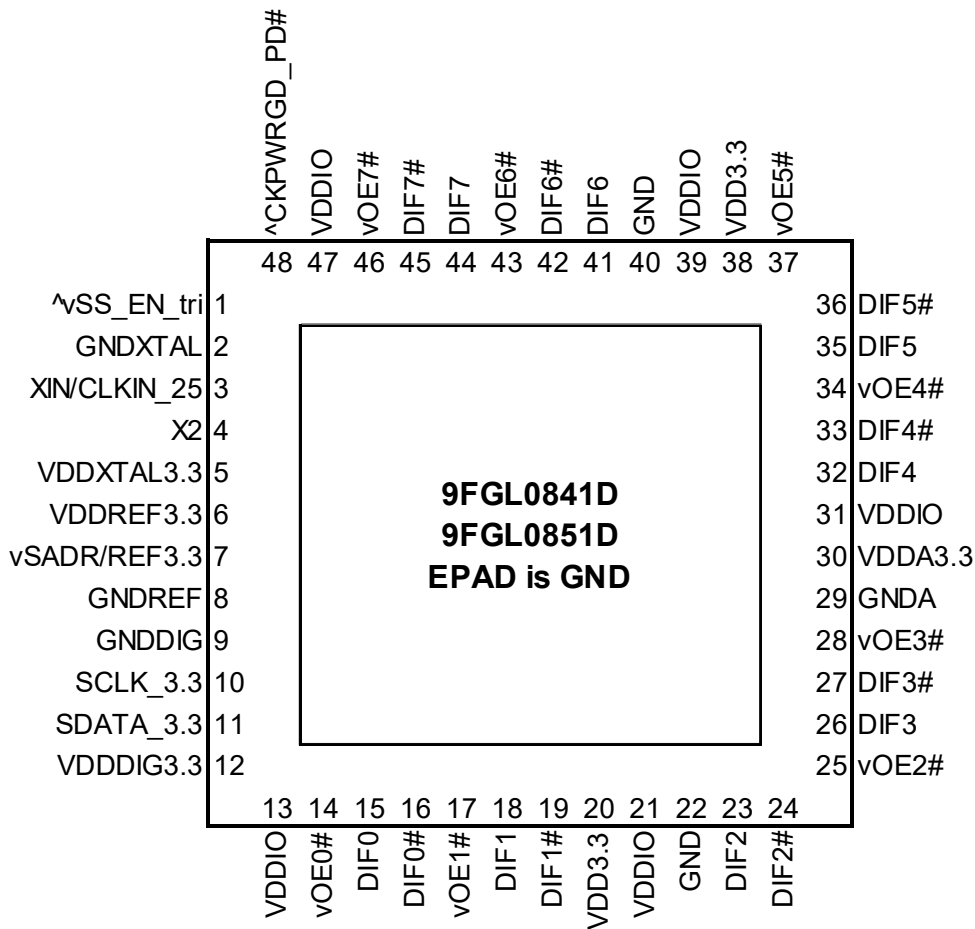


40-VFQFPN, 5 x 5 mm, 0.4mm pitch

- ^ prefix indicates internal 120kOhm pull-up resistor
- v prefix indicates internal 120kOhm pull-down resistor
- ^v prefix indicates internal 120kOhm pull-up and pull-down resistors

Figure 4. 5 x 5 mm 40-VFQFPN Package – Top View

1.4 9FGL08x1D Pin Assignments



48-VFQFPN, 6 x 6 mm, 0.4mm pitch

- ^ prefix indicates internal pull-up resistor
- v prefix indicates internal pull-down resistor
- ^v prefix indicates internal pull-up and pull-down resistors

Figure 5. 6 x 6 mm 48-VFQFPN Package – Top View

1.5 Pin Descriptions

Name	Type	Description	Pin Number			
			9FGL08x1	9FGL06x1	9FGL04x1	9FGL02x1
^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.	48	40	31	22
^vSS_EN_tri	Latched In	Latched select input to select spread spectrum amount at initial power up. See Spread Selection table.	1	1	32	23
DIF0	Output	Differential true clock output.	15	14	13	13

Name	Type	Description	Pin Number			
			9FGL08x1	9FGL06x1	9FGL04x1	9FGL02x1
DIF0#	Output	Differential complementary clock output.	16	15	14	14
DIF1	Output	Differential true clock output.	18	18	18	17
DIF1#	Output	Differential complementary clock output.	19	19	19	18
DIF2	Output	Differential true clock output.	23	22	22	-
DIF2#	Output	Differential complementary clock output.	24	23	23	-
DIF3	Output	Differential true clock output.	26	28	27	-
DIF3#	Output	Differential complementary clock output.	27	29	28	-
DIF4	Output	Differential true clock output.	32	33	-	-
DIF4#	Output	Differential complementary clock output.	33	34	-	-
DIF5	Output	Differential true clock output.	35	36	-	-
DIF5#	Output	Differential complementary clock output.	36	37	-	-
DIF6	Output	Differential true clock output.	41	-	-	-
DIF6#	Output	Differential complementary clock output.	42	-	-	-
DIF7	Output	Differential true clock output.	44	-	-	-
DIF7#	Output	Differential complementary clock output.	45	-	-	-
EPAD	GND	Connect to ground.	49	41	33	25
GND	GND	Ground pin.	22	EPAD	15	10
GND	GND	Ground pin.	40	EPAD	26, 30	21
GND A	GND	Ground pin for the PLL core.	29	EPAD	20	15
GND DIG	GND	Ground pin for digital circuitry.	9	8	8	6
GND REF	GND	Ground pin for the REF outputs.	8	-	7	5
GND XTAL	GND	GND for XTAL.	2	EPAD	1	24
NC	-	No connect.	-	7, 25	-	-
SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.	10	9	10	8
SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.	11	10	11	9
VDD3.3	Power	Power supply, nominally 3.3V.	20	16	16	11
VDD3.3	Power	Power supply, nominally 3.3V.	38	31	25	20
VDDA3.3	Power	3.3V power for the PLL core.	30	26	21	16
VDDDIG3.3	Power	3.3V digital power (dirty power).	12	11	9	7
VDDIO	Power	Power supply for differential outputs.	13	12	-	-
VDDIO	Power	Power supply for differential outputs.	21	17	-	-
VDDIO	Power	Power supply for differential outputs.	31	27	-	-
VDDIO	Power	Power supply for differential outputs.	39	32	-	-
VDDIO	Power	Power supply for differential outputs.	47	39	-	-
VDDREF3.3	Power	Power supply for REF output, nominally 3.3V.	6	5	5	-
VDDXTAL3.3	Power	Power supply for XTAL, nominally 3.3V.	5	4	4	3

Name	Type	Description	Pin Number			
			9FGL08x1	9FGL06x1	9FGL04x1	9FGL02x1
vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	14	13	12	12
vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	17	21	17	19
vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	25	24	24	-
vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	28	30	29	-
vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	34	35	-	-
vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	37	38	-	-
vOE6#	Input	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	43	-	-	-
vOE7#	Input	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	46	-	-	-
vSADR/REF3.3	Latched I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin.	7	6	6	4
X2	Output	Crystal output.	4	3	3	2
XIN/CLKIN_25	Input	Crystal input or Reference Clock input, nominally 25MHz.	3	2	2	1

Table 1. Spread Selection

\wedge vSS_EN_tri Pin	B1[4:3]	Spread%	Note
0	00	0	12kHz to 20MHz mode
-	01	-0.25	PCIe Common Clock or SRIS mode.
M (VDD/2)	10	0	PCIe Common Clock, SRIS or SRNS mode.
1	11	-0.50	PCIe Common Clock or SRIS mode.

If 12kHz to 20MHz mode is desired, power up with \wedge vSS_EN_tri = '0'. Do not attempt to switch to the other modes via SMBus control in Byte 1 or a system reset will be required. If PCIe mode is desired, power up with \wedge vSS_EN_tri at either 'M' or '1'. The desired spread spectrum amount can then be selected via Byte 1 without requiring a system reset. Once 'M' or '1' is latched at power up, do not attempt to enter 12kHz to 20MHz mode or a system reset will be required.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGL02x1/04x1/06x1/08x1D at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage ^[1]	V_{DDx}	With respect to ground	-0.5	4.6	V
Input Voltage ^{[1][2]}	V_{IN}		-0.5	$V_{DD} + 0.5$	V
Input High Voltage, SMBus ^{[1][2]}	V_{IHSMB}	SMBus clock and data pins.	-	$V_{DD} + 0.5$	V
Storage Temperature ^[1]	T_s		-65	150	°C
Junction Temperature ^[1]	T_J		-	125	°C
Input ESD Protection ^[1]	ESD prot	Human Body Model.	2500	-	V

1. Operation under these conditions is neither implied nor guaranteed.

2. Not to exceed 4.6V.

2.2 Thermal Specifications

Table 3. Thermal Characteristics

Parameter	Package	Symbol	Conditions	Typical Values	Unit
9FGL02 Thermal Resistance	NLG24 ^[1]	θ_{JC}	Junction to case.	62	°C/W
		θ_{Jb}	Junction to base.	5.4	°C/W
		θ_{JA0}	Junction to air, still air.	50	°C/W
		θ_{JA1}	Junction to air, 1 m/s air flow.	43	°C/W
		θ_{JA3}	Junction to air, 3 m/s air flow.	39	°C/W
		θ_{JA5}	Junction to air, 5 m/s air flow.	38	°C/W
9FGL04 Thermal Resistance	NLG32 ^[1]	θ_{JC}	Junction to case.	42	°C/W
		θ_{Jb}	Junction to base.	2.4	°C/W
		θ_{JA0}	Junction to air, still air.	39	°C/W
		θ_{JA1}	Junction to air, 1 m/s air flow.	33	°C/W
		θ_{JA3}	Junction to air, 3 m/s air flow.	28	°C/W
		θ_{JA5}	Junction to air, 5 m/s air flow.	27	°C/W
9FGL06 Thermal Resistance	NDG40 ^[1]	θ_{JC}	Junction to case.	42	°C/W
		θ_{Jb}	Junction to base.	2.4	°C/W
		θ_{JA0}	Junction to air, still air.	39	°C/W
		θ_{JA1}	Junction to air, 1 m/s air flow.	33	°C/W
		θ_{JA3}	Junction to air, 3 m/s air flow.	28	°C/W
		θ_{JA5}	Junction to air, 5 m/s air flow.	27	°C/W

Table 3. Thermal Characteristics (Cont.)

Parameter	Package	Symbol	Conditions	Typical Values	Unit
9FGL08 Thermal Resistance	NDG48 [1]	θ_{JC}	Junction to case.	33	°C/W
		θ_{Jb}	Junction to base.	2.1	°C/W
		θ_{JA0}	Junction to air, still air.	37	°C/W
		θ_{JA1}	Junction to air, 1 m/s air flow.	30	°C/W
		θ_{JA3}	Junction to air, 3 m/s air flow.	27	°C/W
		θ_{JA5}	Junction to air, 5 m/s air flow.	26	°C/W

1. EPAD soldered to board.

2.3 Electrical Specifications

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 4. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
SMBus Input Low Voltage	V_{ILSMB}	$V_{DDSMB} = 3.3V$.	-	-	0.8	V
SMBus Input High Voltage	V_{IHSMB}	$V_{DDSMB} = 3.3V$.	2.1	-	3.6	V
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP} .	-	-	0.4	V
SMBus Sink Current	I_{PULLUP}	At V_{OL} .	4	-	-	mA
Nominal Bus Voltage	V_{DDSMB}		2.7	-	3.6	V
SCLK/SDATA Rise Time [1]	t_{RSMB}	(Max. $V_{IL} - 0.15V$) to (Min. $V_{IH} + 0.15V$).	-	-	1000	ns
SCLK/SDATA Fall Time [1]	t_{FSMB}	(Min. $V_{IH} + 0.15V$) to (Max. $V_{IL} - 0.15V$).	-	-	300	ns
SMBus Operating Frequency [2]	f_{SMB}	SMBus operating frequency.	-	-	500	kHz

1. Confirmed by design and characterization, not 100% tested in production.

2. The device must be powered up for the SMBus to function.

Table 5. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DDxxx}	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V
IO Supply Voltage	V_{DDIO}	Supply voltage for differential low power outputs.	0.9975	1.05–3.3	3.465	V
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus.	$0.75 \times V_{DDx}$	-	$V_{DDx} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3	-	$0.25 \times V_{DDx}$	V
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix).	$0.8 \times V_{DDx}$	-	$V_{DDx} + 0.3$	V
Input Mid Voltage	V_{IMtri}		$0.4 \times V_{DDx}$	$0.5 \times V_{DDx}$	$0.6 \times V_{DDx}$	V
Input Low Voltage	V_{ILtri}		-0.3	-	$0.20 \times V_{DDx}$	V

Table 5. Input/Supply/Common Parameters – Normal Operating Conditions (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Current	I_{IN}	Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$.	-5	-	5	μA
	I_{INP}	Single-ended inputs. $V_{IN} = 0V$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors.	-50	-	50	μA
Input Frequency [1]	F_{IN}	XTAL or X1 input.	-	25	-	MHz
Pin Inductance [2]	L_{pin}		-	-	7	nH
Capacitance [2]	C_{IN}	Logic inputs, except DIF_IN.	1.5	-	5	pF
	C_{OUT}	Output pin capacitance.	-	-	6	pF
CLK Stabilization [2][3]	t_{STAB}	From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock.	-	0.3	1.8	ms
SS Modulation Frequency [2]	f_{MOD}	Triangular modulation.	30	31.6	33	kHz
OE# Latency [2]	$t_{LATO\#}$	DIF start after OE# assertion. DIF stop after OE# de-assertion.	3	4	5	clocks
Fall Time [2][3]	t_F	Fall time of single-ended control inputs.	-	-	5	ns
Rise Time [2][3]	t_R	Rise time of single-ended control inputs.	-	-	5	ns

1. Contact the factory for other frequencies.
2. Confirmed by design and characterization, not 100% tested in production.
3. Control input must be monotonic from 20% to 80% of input swing.

Table 6. Differential Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate	T_{rf}	Scope averaging on, fast setting. [1][2]	3	3.8	4.6	V/ns
		Scope averaging, slow setting. [1][2]	2	2.7	3.5	V/ns
Crossing Voltage (abs)	V_{cross_abs}	Scope averaging off. [3][4][5]	250	429	550	mV
Crossing Voltage (var)	$\Delta-V_{cross}$	Scope averaging off. [3][4][6]	-	26	140	mV
Avg. Clock Period Accuracy	T_{PERIOD_AVG}	9FGL0xxx devices have 0 ppm synthesis error. -0.5% SSC. [1][7][8][9]	-	0	+2500	ppm
		-0.25% SSC	-	0	+1250	
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread spectrum modulation. [1][10]	9.95	10	10.0503	ns
Jitter, Cycle to Cycle [1]	$t_{cyc-cyc}$		-	16	50	ps
Voltage High [3]	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	790	850	mV
Voltage Low [3]	V_{LOW}		-150	-4	150	mV
Absolute Maximum Voltage [3][11][12]	V_{MIN}	Measurement on single-ended signal using absolute value (scope averaging off).	-	832	1150	mV
Absolute Minimum Voltage [3][12][13]	V_{MAX}		-300	-61	-	mV
Duty Cycle [1]	t_{DC}		45	48.6	55	%

Table 6. Differential Low-Power HCSL Outputs (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate Matching [3][14]	ΔT_{rf}	Single-ended measurement.	-	9	20	%
Skew, Output to Output [1]	t_{sk3}	Averaging on, $V_T = 50\%$.	-	32	50	ps

1. Measured from differential waveform.
2. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
3. Measured from single-ended waveform.
4. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
6. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.
7. Refer to Section 8.6.2 of the PCI Express Base Specification, Revision 5.0 for information regarding PPM considerations.
8. PCIe Gen1 through Gen4 specify ± 300 ppm frequency tolerances. PCIe Gen5 reduces the allowable tolerance to ± 100 ppm without spread spectrum.
9. "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of $100\text{Hz/ppm} \times 100\text{ppm} = 10\text{kHz}$. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ± 100 ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.
10. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.
11. Defined as the maximum instantaneous voltage including overshoot.
12. At default SMBus amplitude settings.
13. Defined as the minimum instantaneous voltage including undershoot.
14. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ± 75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.
15. System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors C_L . Single-ended probes must be used for measurements requiring single ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load $C_L = 2\text{pF}$.

Table 7. 12kHz–20MHz Phase Jitter of Differential Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Phase Jitter, 12kHz–20MHz	$t_{jph12k20M}$	Differential outputs when device is set to 12kHz to 20MHz mode (SS_EN_tri = 0 or Byte1[4:3] = 00).	-	2	2.1	ps (rms)

Table 8. Current Consumption – 9FGL02

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I _{DDAOP}	V _{DDA} , all outputs active at 100MHz.	-	13	17	mA
	I _{DDOP}	All V _{DD} , except V _{DDA} , all outputs active at 100MHz.	-	18	23	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I _{DDAPD}	V _{DDA} , DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} , DIF outputs off, REF output running. [1]	-	5.7	8	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I _{DDAPD}	V _{DDA} , all outputs off.	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} , all outputs off.	-	1.7	2.5	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 9. Current Consumption – 9FGL04

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I _{DDAOP}	V _{DDA} , all outputs active at 100MHz.	-	13	17	mA
	I _{DDOP}	All other V _{DD} , except V _{DDA} , all outputs active at 100MHz.	-	30	39	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I _{DDAPD}	V _{DDA} , DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I _{DDPD}	All other V _{DD} , except V _{DDA} , DIF outputs off, REF output running. [1]	-	5.9	8.0	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I _{DDAPD}	V _{DDA} , all outputs off.	-	0.9	1.5	mA
	I _{DDPD}	All other V _{DD} , except V _{DDA} , all outputs off.	-	1.5	2.5	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 10. Current Consumption – 9FGL06

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I _{DDAOP}	V _{DDA} , all outputs active at 100MHz.	-	14	17	mA
	I _{DDOP}	All V _{DD} , except V _{DDA} and V _{DDIO} , all outputs active at 100MHz.	-	16	20	mA
	I _{DDIOOP}	V _{DDIO} , all outputs active at 100MHz.	-	27	32	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I _{DDAPD}	V _{DDA} , DIF outputs off, REF output running.	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} and V _{DDIO} , DIF outputs off, REF output running. [1]	-	6	8	mA
	I _{DDIOOP}	V _{DDIO} , DIF outputs off, REF output running. [1]	-	0.04	0.05	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I _{DDAPD}	V _{DDA} , all outputs off.	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} and V _{DDIO} , all outputs off.	-	1.8	2.5	mA
	I _{DDIOOP}	V _{DDIO} , all outputs off.	-	0.04	0.08	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 11. Current Consumption – 9FGL08

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I _{DDAOP}	V _{DDA} , all outputs active at 100MHz.	-	14	19	mA
	I _{DDOP}	All V _{DD} , except V _{DDA} and V _{DDIO} , all outputs active at 100MHz.	-	18	24	mA
	I _{DDIOOP}	V _{DDIO} , all outputs active at 100MHz.	-	30	37	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I _{DDAPD}	V _{DDA} , DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} and V _{DDIO} , DIF outputs off, REF output running. [1]	-	5.2	8	mA
	I _{DDIOOP}	V _{DDIO} , DIF outputs off, REF output running. [1]	-	0.04	0.1	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I _{DDAPD}	V _{DDA} , all outputs off.	-	0.9	1.5	mA
	I _{DDPD}	All V _{DD} , except V _{DDA} and V _{DDIO} , all outputs off.	-	1.7	2.5	mA
	I _{DDIOOP}	V _{DDIO} , all outputs off.	-	0.04	0.1	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 12. PCIe Phase Jitter of Differential Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See [Test Loads](#) for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit	
PCIe Phase Jitter Common Clocked Architecture [1]	t _{jphPCIeG1-CC}	PCIe Gen1 (2.5 GT/s) [2][3]	-	9683	12771	86000	fs pk-pk	
	t _{jphPCIeG2-CC}	PCIe Gen2 Hi Band (5.0 GT/s) [2][3]	-	297	415	3100		
		PCIe Gen2 Lo Band (5.0 GT/s) [2][3]	-	377	531	3000		
	t _{jphPCIeG3-CC}	PCIe Gen3 (8.0 GT/s) [2][3][4]	-	177	228	1000		fs RMS
	t _{jphPCIeG4-CC}	PCIe Gen4 (16.0 GT/s) [2][3][4][5]	-	177	228	500		
t _{jphPCIeG5-CC}	PCIe Gen5 (32.0 GT/s) [2][3][4][6]	-	61	85	150			
PCIe Phase Jitter SRIS Architecture - SSC = -0.5%	t _{jphPCIeG2-SRIS}	PCIe Gen2 (5.0 GT/s) [2]	-	1422	1503	N/A	fs RMS	
	t _{jphPCIeG3-SRIS}	PCIe Gen3 (8.0 GT/s) [2]	-	559	595			
	t _{jphPCIeG4-SRIS}	PCIe Gen4 (16.0 GT/s) [2]	-	411	452			
PCIe Phase Jitter SRIS Architecture - SSC = -0.25%	t _{jphPCIeG5-SRIS}	PCIe Gen5 (32.0 GT/s) [2]	-	126	159			
PCIe Phase Jitter SRNS Architecture - SSC = 0% (Byte1[4:3] = 10, SS_EN_tri = M)	t _{jphPCIeG2-SRNS}	PCIe Gen2 (5.0 GT/s) [2]	-	696	780	N/A	fs RMS	
	t _{jphPCIeG3-SRNS}	PCIe Gen3 (8.0 GT/s) [2]	-	255	318			
	t _{jphPCIeG4-SRNS}	PCIe Gen4 (16.0 GT/s) [2]	-	259	315			
	t _{jphPCIeG5-SRNS}	PCIe Gen5 (32.0 GT/s) [2]	-	111	167			

1. Calculated for Byte1[4:3] spread settings of 01, 10 and 11 (SS_EN_tri = M or 1).
2. The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. If oscilloscope data is used, equipment noise is removed from all results.

- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
- SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

Table 13. REF Output

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Long Accuracy	ppm	See Tperiod min-max values. [1][2]	0			ppm
Clock Period	T _{period}	REF output. [2]	40			ns
High Output Voltage	V _{HIGH}	I _{OH} = -2mA.	0.8 x V _{DDREF}	-	-	V
Low Output Voltage	V _{LOW}	I _{OL} = 2mA.	-	-	0.2 x V _{DDREF}	
Rise/Fall Slew Rate	t _{rf1}	Byte 3 = 1F, V _{OH} = 0.8 x V _{DD} , V _{OL} = 0.2 x V _{DD} . [1]	0.5	0.9	1.5	V/ns
	t _{rf1}	Byte 3 = 5F, V _{OH} = 0.8 x V _{DD} , V _{OL} = 0.2 x V _{DD} . [1][3]	1.0	1.5	2.5	
	t _{rf1}	Byte 3 = 9F, V _{OH} = 0.8 x V _{DD} , V _{OL} = 0.2 x V _{DD} . [1]	1.5	2.1	3.1	
	t _{rf1}	Byte 3 = DF, V _{OH} = 0.8 x V _{DD} , V _{OL} = 0.2 x V _{DD} . [1]	2.0	2.7	3.8	
Duty Cycle	d _{t1X}	V _T = V _{DD} /2 V. [1][4]	45	49.7	55	%
Jitter, Cycle to Cycle	t _{j cyc-cyc}	V _T = V _{DD} /2 V. [1][4]	-	35	125	ps
Noise Floor	t _{jdBc1k}	1kHz offset. [1][4]	-	-132	-115	dBc
	t _{jdBc10k}	10kHz offset to Nyquist. [1][4]	-	-150	-140	
Jitter, Phase	t _{jphREF}	12kHz to 5MHz, DIF SSC off. [1][4]	-	0.13	0.3	ps RMS
		12kHz to 5MHz, DIF SSC on. [1][4][5]	-	1.4	1.5	

- Confirmed by design and characterization, not 100% tested in production.
- All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz
- Default SMBus value.
- When driven by a crystal.
- Does not apply to the 9FGL06x1 devices.

3. Power Management

Table 14. Power Management [1]

CKPWRGD_PD#	SMBus OE bit	OEx# Pin	Differential Output		REF
			True O/P	Comp. O/P	
0	X	X	Low [2]	Low [2]	Hi-Z [3]
1	1	0	Running	Running	Running
1	1	1	Disabled [2]	Disabled [2]	Running
1	0	X	Disabled [2]	Disabled [2]	Disabled [4]

1. Input polarities defined at default values.
2. The output state is set by B11[1:0] (Low/Low default).
3. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5] = 1, in which case REF is running.
4. See SMBus description for Byte 3, bit 4.

Table 15. SMBus Address Selection

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

4. Test Loads

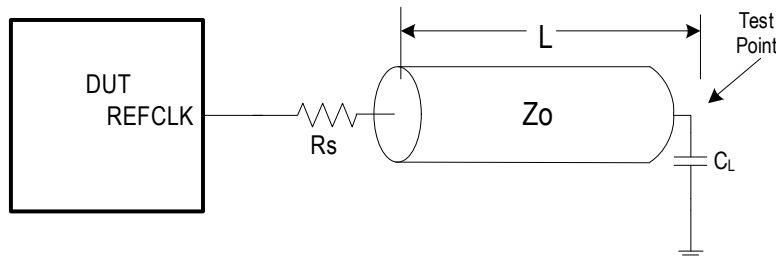


Figure 6. Single-ended Output Test Load

Table 16. Terminations for Single-ended Output

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	CL (pF)
N/A	9FGL0nxx	33	50	12.7	4.7

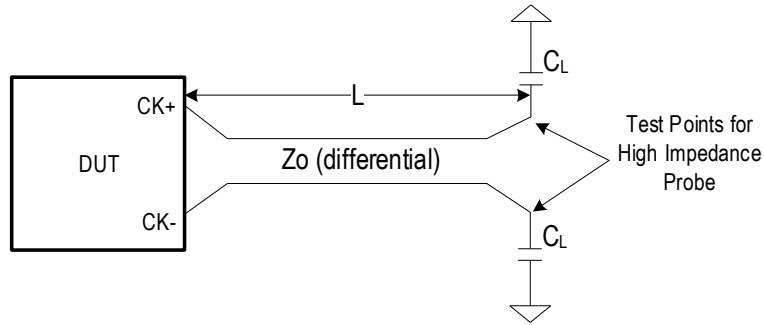


Figure 7. Test Load for AC/DC Measurements

Table 17. Terminations for AC/DC Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	CL (pF)
N/A	9FGL0x41	Internal	100	12.7	2
N/A	9FGL0x51	Internal	85	12.7	2

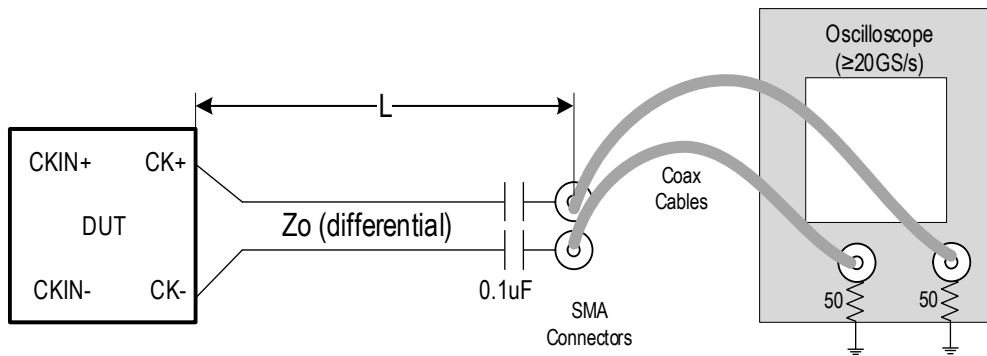


Figure 8. Test Setup for PCIe Clock Phase Jitter Measurements

Table 18. Terminations for PCIe Clock Phase Jitter Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	CL (pF)
N/A	9FGL0x41	Internal	100	12.7	N/A
N/A	9FGL0x51	Internal	85	12.7	N/A

5. Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs”](#) for details.

6. Crystal Characteristics

Table 19. Recommended Crystal Characteristics

Parameter	Value	Unit
Frequency [1]	25	MHz
Resonance Mode	Fundamental	-
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, reference at 25°C over operating temperature range	±20	ppm maximum
Temperature Range (industrial)	-40 to +85	°C
Temperature Range (commercial)	0 to +70	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C _O)	7	pF maximum
Load Capacitance (C _L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

1. When driven by an external oscillator via the XIN/CLKIN_25 pin, X2 should be floating.

7. General SMBus Serial Interface Information

7.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation		
Controller (Host)		Renesas (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Note: Address is latched on SADR pin.

7.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address

- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		Renesas
T	starT bit	
Slave Address		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address		
RD	ReaD	
		ACK
		Data Byte Count=X
ACK		
		Beginning Byte N
ACK		
O		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Table 20. Byte 0: Output Enable Register

Byte 0 [1]	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	See B11[1:0]							
1	OE# Pin Controls Output							
9FGL08 Name	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0

Table 20. Byte 0: Output Enable Register

Byte 0 [1]	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9FGL08 Default	1	1	1	1	1	1	1	1
9FGL06 Name	OE5	OE4	Reserved	OE3	OE2	OE1	Reserved	OE0
9FGL06 Default	1	1	x	1	1	1	x	1
9FGL04 Name	Reserved	Reserved	Reserved	Reserved	OE3	OE2	OE1	OE0
9FGL04 Default	x	x	x	x	1	1	1	1
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	Reserved	OE1	OE0	Reserved
9FGL02 Default	x	x	x	x	x	1	1	x

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

Table 21. Byte 1: Spread Spectrum with V_{HIGH} Control Register

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	SS Enable Readback Bit1	SS Enable Readback Bit0	Enable software control of spread spectrum	SS Software Control Bit1	SS Software Control Bit0	Reserved	Controls Output Amplitude	
Type	R	R	RW	RW [1]	RW [1]		RW	RW
0	See Spread Selection table		SS controlled by latch (B1[7:6])	See Spread Selection table			00 = 0.6V	10 = 0.75V
1			Values in B1[4:3] control SS amount				01 = 0.68V	11 = 0.85V
Name	SSENRB1	SSENRB1	SSEN_SWCNTRL	SSENSW1	SSENSW0		AMPLITUDE 1	AMPLITUDE 0
Default	Latch	Latch	0	0	0	x	1	0

1. See notes on [Spread Selection](#) table. B1[5] must be set to a 1 in order to use B1[4:3].

Table 22. Byte 2: DIF Slew Selection Register [1]

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	Slow Slew Rate							
1	Fast Setting							
9FGL08 Name	DIF7_slew	DIF6_slew	DIF5_slew	DIF4_slew	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew

Table 22. Byte 2: DIF Slew Selection Register [1]

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9FGL08 Default	1	1	1	1	1	1	1	1
9FGL06 Name	DIF5_slew	DIF4_slew	Reserved	DIF3_slew	DIF2_slew	DIF1_slew	Reserved	DIF0_slew
9FGL06 Default	1	1	x	1	1	1	x	1
9FGL04 Name	Reserved	Reserved	Reserved	Reserved	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew
9FGL04 Default	x	x	x	x	1	1	1	1
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	Reserved	DIF1_slew	DIF0_slew	Reserved
9FGL02 Default	x	x	x	x	x	1	1	x

1. See [Differential Low-Power HCSL Outputs](#) table for slew rates.

Table 23. Byte 3: REF Slew Rate Control Register

Byte 3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Slew Rate Control		Wake-on-Lan Enable for REF	REF Output Enable	Reserved	Reserved	Reserved	Reserved
Type	RW	RW	RW	RW				
0	00 = Slowest	10 = Fast	REF disabled in Power Down	Disabled [1]				
1	01 = Slow	11 = Fastest	REF runs in Power Down	Enabled				
Name	REF Slew Rate [1:0]		REF Power Down Function	REF OE				
Default	0	1	0	1	x	x	x	x

1. The disabled state depends on Byte1[1:0]. '00' = Low, '01' = HiZ, '10' = Low, '11' = High.

Byte 4 is Reserved

Table 24. Byte 5: Revision and Vendor ID Register

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				VENDOR ID			
Type	R	R	R	R	R	R	R	R
0	D rev = 0011				0001 = Renesas			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0

Table 25. Byte 6: Device Type/Device ID Register

Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Device Type		Device ID					
Type	R	R	R	R	R	R	R	R
0	00 = FGL		9FGL08 = 0b01000 9FGL06 = 0b00110 9FGL04 = 0b00100 9FGL02 = 0b00010					
1								
Name	Device Type1	Device Type0	Device ID5	Device ID4	Device ID3	Device ID2	Device ID1	Device ID0

Table 26. Byte 7: Byte Count Register

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Byte Count Programming							
Type	Reserved	Reserved	Reserved	RW	RW	RW	RW	RW
0				Writing to this register will configure how many bytes will be read back.				
1				-	-	-	-	-
Name				BC4	BC3	BC2	BC1	BC0
Default				x	x	x	0	1

Bytes 8 and 9 are Reserved

Table 27. Byte 10: PLL MN Enable, PD_Restore Register

Byte 10	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	M/N Programming Enable	Restore Default Config. In PD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Type	RW	RW						
0	M/N Prog. Disabled	Clear Config in PD						
1	M/N Prog. Enabled	Keep Config in PD						
Name	PLL M/N En	Power-Down (PD) Restore						
Default	0	1	x	x	x	x	x	x

Table 28. Byte 11: Stop State Control Register

Byte 11	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Control Function	Reserved							True/Complement DIF Output Disable State	
Type								RW	RW
0								00 = Low/Low	01 = HiZ/HiZ
1								10 = High/Low	11 = Low/High
Name								STP[1]	STP[0]
Default	x	x	x	x	x	x	0	0	

Table 29. Byte 12: Impedance Control Register 1

Byte 12	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = Reserved, 01 = 85ohm DIF Zout							
1	10 = 100ohm DIF Zout, 11 = Reserved							
9FGL08 Name	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	DIF1_imp[1]	DIF1_imp[0]	DIF0_imp[1]	DIF0_imp[0]
9FGL08 Default	9FGL0841 defaults to 0b10101010 9FGL0851 defaults to 0b01010101							
9FGL06 Name	DIF2_imp[1]	DIF2_imp[0]	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved	DIF0_imp[1]	DIF0_imp[0]
9FGL06 Default	9FGL0641 defaults to 0b1010xx10 9FGL0651 defaults to 0b0101xx01							
9FGL04 Name	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved
9FGL04 Default	9FGL0441 defaults to 0b10xx10xx 9FGL0451 defaults to 0b01xx01xx							
9FGL02 Name	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9FGL02 Default	9FGL0241 defaults to 0b10xxxxxx 9FGL0251 defaults to 0b01xxxxxx							

Table 30. Byte 13: Impedance Control Register 2

Byte 13	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = Reserved, 01 = 85ohm DIF Zout							
1	10 = 100ohm DIF Zout, 11 = Reserved							
9FGL08 Name	DIF7_imp[1]	DIF7_imp[0]	DIF6_imp[1]	DIF6_imp[0]	DIF5_imp[1]	DIF5_imp[0]	DIF4_imp[1]	DIF4_imp[0]
9FGL08 Default	9FGL0841 defaults to 0hAA 9FGL0851 defaults to 0h55							
9FGL06 Name	DIF5_imp[1]	DIF5_imp[0]	DIF4_imp[1]	DIF4_imp[0]	Reserved	Reserved	DIF3 Zout	DIF3 Zout
9FGL06 Default	9FGL0641 defaults to 0b1010xx10 9FGL0651 defaults to 0b0101xx01							
9FGL04 Name	Reserved	Reserved	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	Reserved	Reserved
9FGL04 Default	9FGL0441 defaults to 0bxx1010xx 9FGL0451 defaults to 0bxx0101xx							
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved
9FGL02 Default	9FGL0241 defaults to 0bxxxx10xx 9FGL0251 defaults to 0bxxxx01xx							

Table 31. Byte 14: Pull-up Pull-down Control Register 1

Byte 14	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Pull-up(pu)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
1	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
9FGL08 Name	OE3_pu/pd [1]	OE3_pu/pd [0]	OE2_pu/pd [1]	OE2_pu/pd [0]	OE1_pu/pd [1]	OE1_pu/pd [0]	OE0_pu/pd [1]	OE0_pu/pd [0]
9FGL08 Default	0	1	0	1	0	1	0	1
9FGL06 Name	OE2_pu/pd [1]	OE2_pu/pd [0]	OE1_pu/pd [1]	OE1_pu/pd [0]	Reserved	Reserved	OE0_pu/pd [1]	OE0_pu/pd [0]
9FGL06 Default	0	1	0	1	x	x	0	1
9FGL04 Name	OE1_pu/pd [1]	OE1_pu/pd [0]	Reserved	Reserved	OE0_pu/pd [1]	OE0_pu/pd [0]	Reserved	Reserved
9FGL04 Default	0	1	x	x	0	1	x	x

Table 31. Byte 14: Pull-up Pull-down Control Register 1 (Cont.)

Byte 14	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9FGL02 Name	OE0_pu/pd [1]	OE0_pu/pd [0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9FGL02 Default	0	1	x	x	x	x	x	x

Table 32. Byte 15: Pull-up Pull-down Control Register 2

Byte 15	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control		Pull-up(pd)/ Pull-down(pd) control	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
1	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
9FGL08 Name	OE7_pu/pd [1]	OE7_pu/pd [0]	OE6_pu/pd [1]	OE6_pu/pd [0]	OE5_pu/pd [1]	OE5_pu/pd [0]	OE4_pu/pd [1]	OE4_pu/pd [0]
9FGL08 Default	0	1	0	1	0	1	0	1
9FGL06 Name	OE5_pu/pd [1]	OE5_pu/pd [0]	OE4_pu/pd [1]	OE4_pu/pd [0]	Reserved	Reserved	OE3_pu/pd [1]	OE3_pu/pd [0]
9FGL06 Default	0	1	0	1	0	1	0	1
9FGL04 Name	Reserved	Reserved	OE3_pu/pd [1]	OE3_pu/pd [0]	OE2_pu/pd [1]	OE2_pu/pd [0]	Reserved	Reserved
9FGL04 Default	0	1	0	1	0	1	0	1
9FGL02 Name	Reserved	Reserved	Reserved	Reserved	OE1_pu/pd [1]	OE1_pu/pd [0]	Reserved	Reserved
9FGL02 Default	0	1	0	1	0	1	0	1

Table 33. Byte 16: Pull-up Pull-down Control Register 3

Byte 16	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Pull-up(pd)/ Pull-down(pd) control	
Type							RW	RW
0							00 = None	01 = pd
1							10 = pu	11 = pu+pd
Name							CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD_pu/pd[0]
Default	0	0	1	0	0	1	1	0

Byte 17 is Reserved

Table 34. Byte 18: Polarity Control Register 2

Byte 18	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	Output enabled when OE pin is low							
1	Output enabled when OE pin is high							
9FGL08 Name	OE7_polarity	OE6_polarity	OE5_polarity	OE4_polarity	OE3_polarity	OE2_polarity	OE1_polarity	OE0_polarity
9FGL08 Default	0	0	0	0	0	0	0	0
9FGL06 Name	OE5_polarity	OE4_polarity	Reserved	OE3_polarity	OE2_polarity	OE1_polarity	Reserved	OE0_polarity
9FGL06 Default	0	0	0	0	0	0	0	0
9FGL04 Name	Reserved	OE3_polarity	OE2_polarity	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved
9FGL04 Default	0	0	0	0	0	0	0	0
9FGL02 Name	Reserved	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved	Reserved	Reserved
9FGL02 Default	0	0	0	0	0	0	0	0

Table 35. Byte 19: Polarity Control Register 1

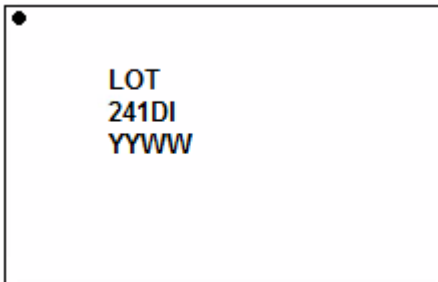
Byte 19	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Sets CKPWRGD_PD polarity
Type								RW
0								Power Down when Low
1								Power Down when High
Name								CKPWRGD_PD polarity
Default	0	0	0	0	0	0	0	0

8. Package Outline Drawings

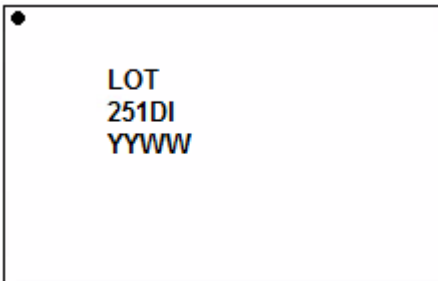
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

9. Marking Diagrams

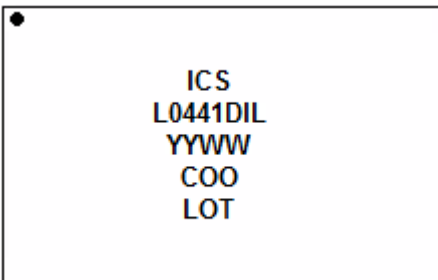
9.1 9FGL02x1D



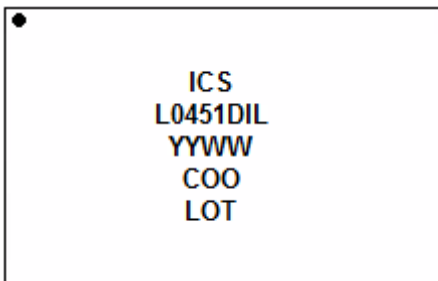
- Line 1: "LOT" denotes the lot number.
- Line 2: truncated part number.
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.



9.2 9FGL04x1D



- Lines 1 and 2: truncated part number
- Line 3: "YYWW" is the last two digits of the year and the work week the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.



9.3 9FGL06x1D

•
ICS
GL0641DI
YYWW
COO
LOT

- Lines 1 and 2: truncated part number
- Line 3: “YYWW” is the last two digits of the year and the work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” denotes the lot number.

•
ICS
GL0651DI
YYWW
COO
LOT

9.4 9FGL08x1D

•
ICS
FGL0841DI
YYWW
COO
LOT

- Lines 1 and 2: truncated part number
- Line 3: “YYWW” is the last two digits of the year and the work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” denotes the lot number.

•
ICS
FGL0851DI
YYWW
CO
LOT

10. Ordering Information

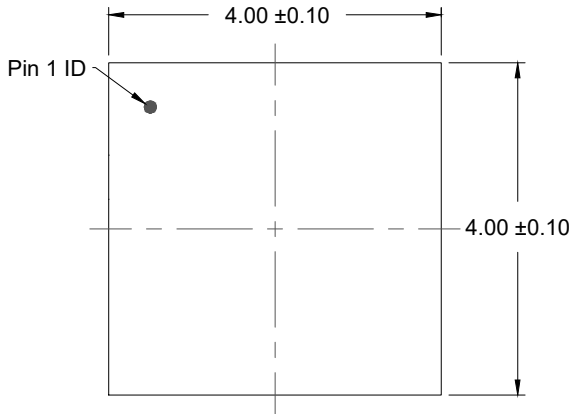
Number of Clock Outputs	Output Impedance	Part Number	Package Description	Temp. Range	Carrier Type
2	100	9FGL0241DKILF	24-VFQFPN, 4 × 4 mm	-40 to +85°C	None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (for more information, see Table 36)
		9FGL0241DKILFT			
	85	9FGL0251DKILF			
		9FGL0251DKILFT			
4	100	9FGL0441DKILF	32-VFQFPN, 5 × 5 mm		
		9FGL0441DKILFT			
	85	9FGL0451DKILF			
		9FGL0451DKILFT			
6	100	9FGL0641DKILF	40-VFQFPN, 5 × 5 mm		
		9FGL0641DKILFT			
	85	9FGL0651DKILF			
		9FGL0651DKILFT			
8	100	9FGL0841DKILF	48-VFQFPN, 6 × 6 mm		
		9FGL0841DKILFT			
	85	9FGL0851DKILF			
		9FGL0851DKILFT			

Table 36. Pin 1 Orientation in Tape and Reel Packaging

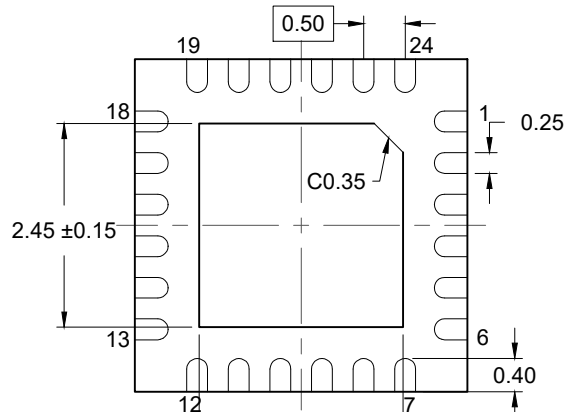
Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	

11. Revision History

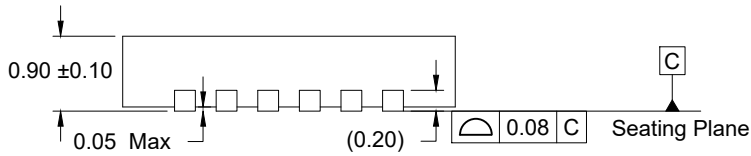
Revision	Date	Description
1.03	Nov 29, 2022	<ul style="list-style-type: none"> Changed the 9FGL08 definition for Device ID in Table 25 to 0b01000 from 0b00100. Updated the package links in Ordering Information
1.02	Aug 19, 2022	Changed the maximum Supply Voltage to 4.6V in Table 2 .
1.01	Jun 14, 2022	Updated Slew Rate values in Table 6 .
1.00	Jun 7, 2022	Initial release.



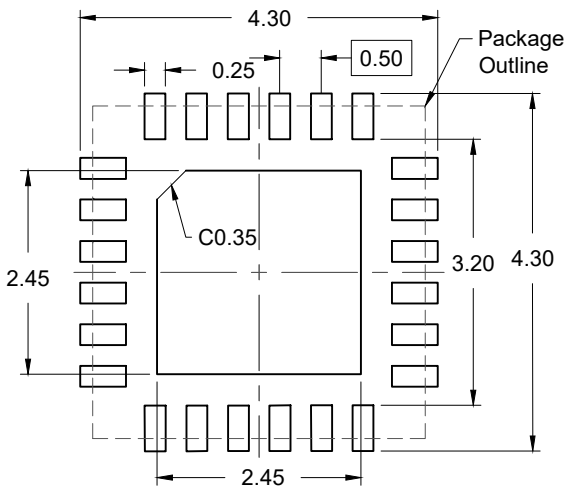
TOP VIEW



BOTTOM VIEW



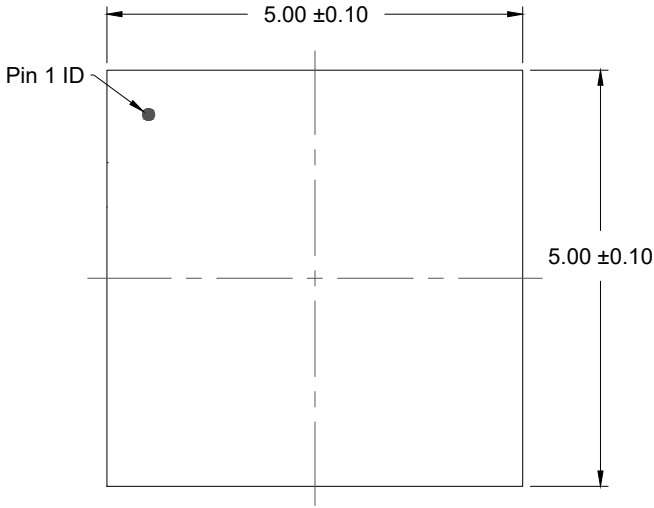
SIDE VIEW



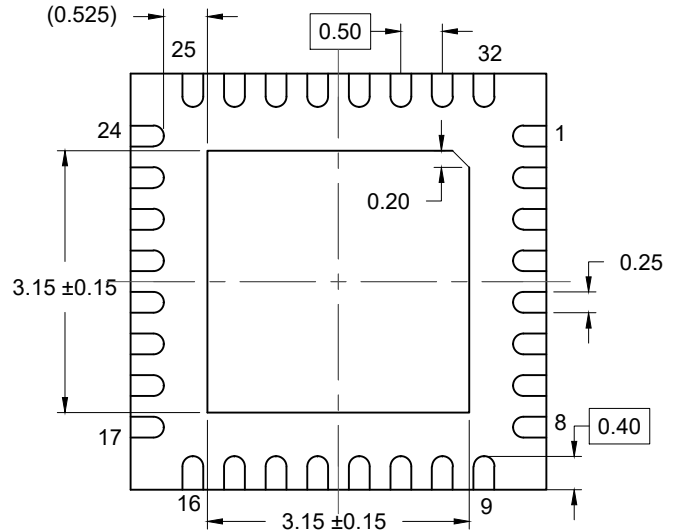
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

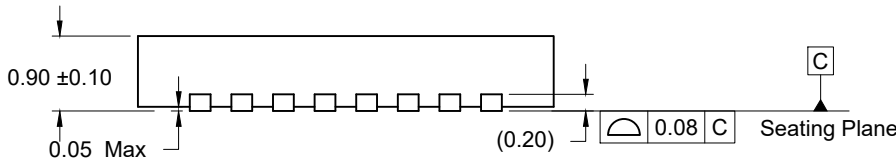
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.



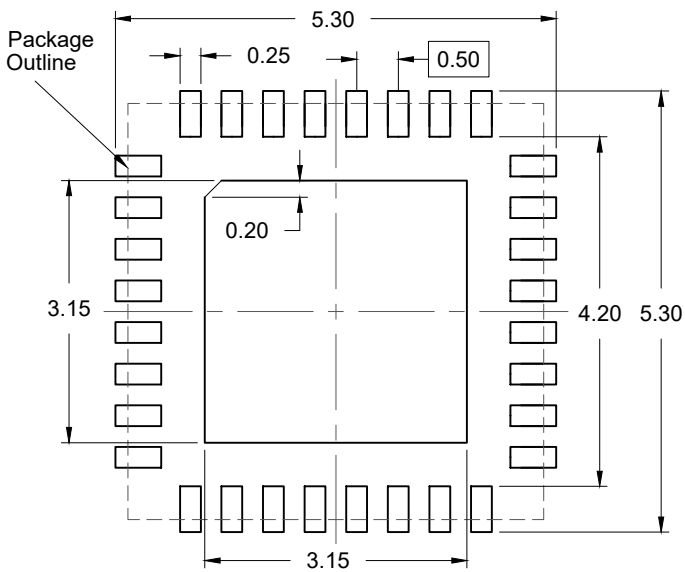
TOP VIEW



BOTTOM VIEW



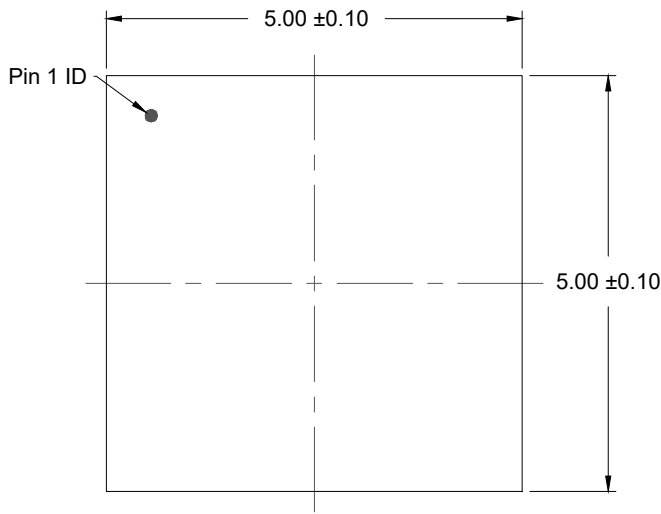
SIDE VIEW



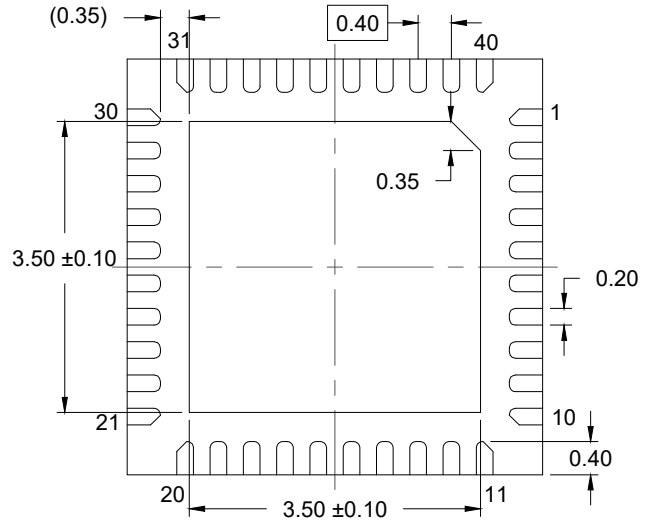
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

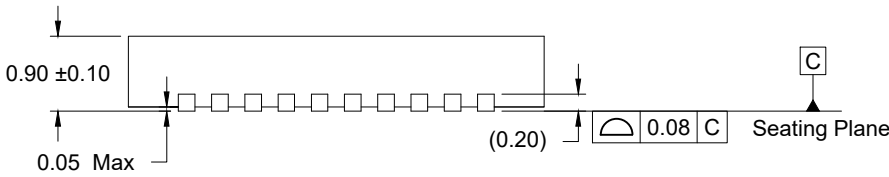
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.



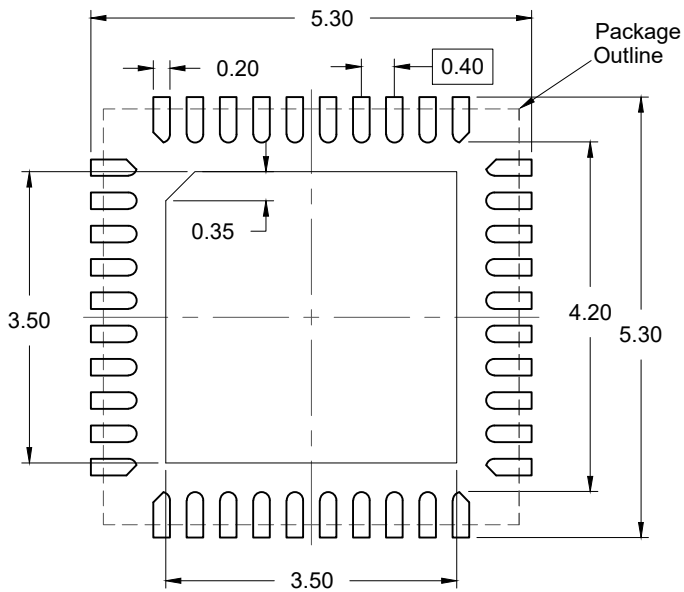
TOP VIEW



BOTTOM VIEW



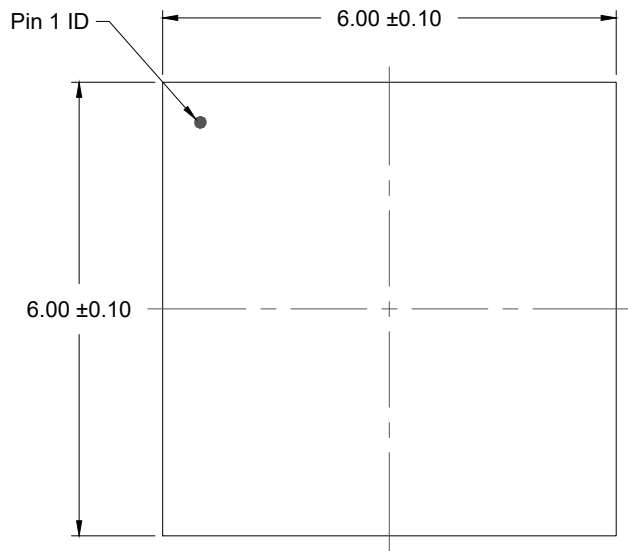
SIDE VIEW



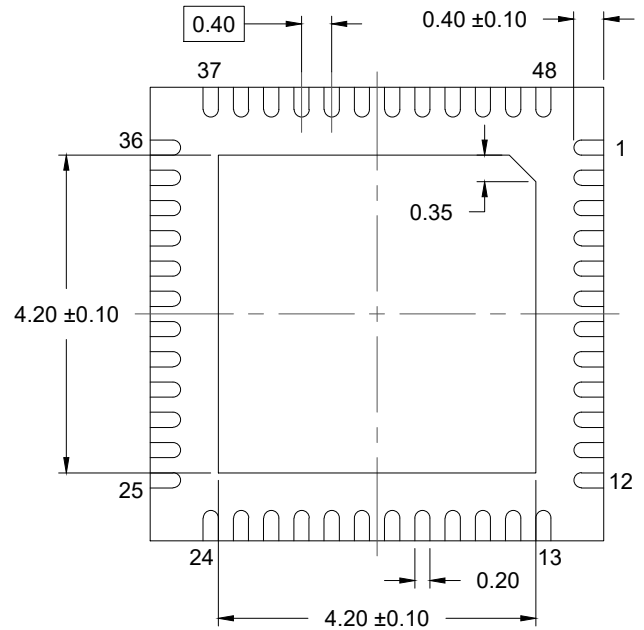
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

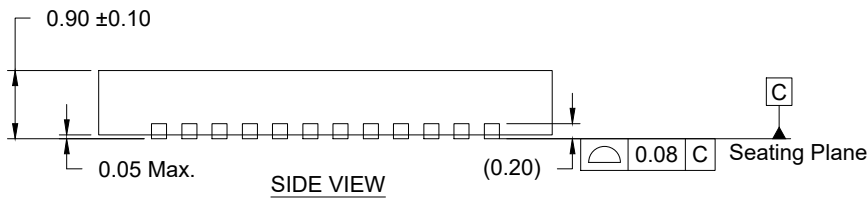
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.



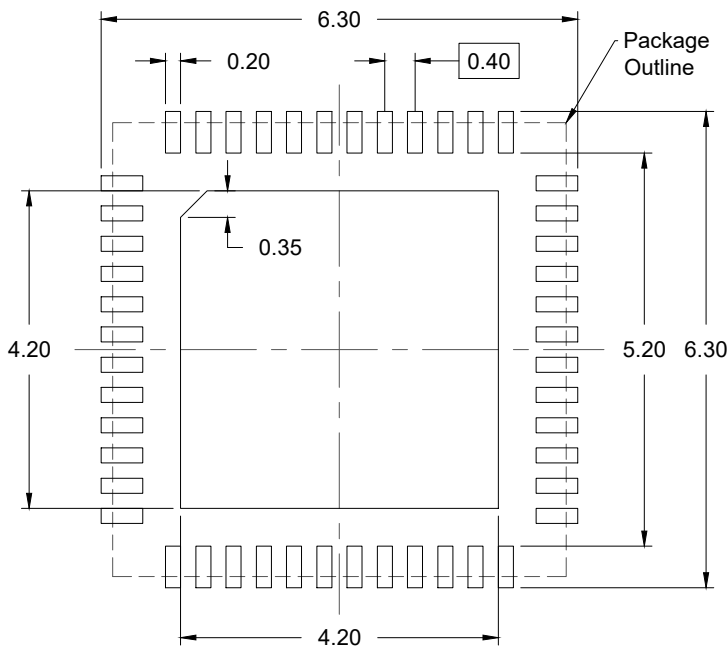
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.