

Description

The 9FGV1001C / 9FGV1005C are members of the Renesas PhiClock™ programmable clock generator family. The devices are optimized for low phase noise in non-spread spectrum applications such as Ethernet or PCI Express. Four user-defined configurations may be selected via two hardware select pins or two I²C bits, allowing easy software selection of the desired configuration.

Typical Applications

- High-performance Computing (HPC)
- Enterprise Storage including eSSDs
- 10G / 25G / 100G Ethernet
- Data Center Accelerators
- Multiple XO replacement

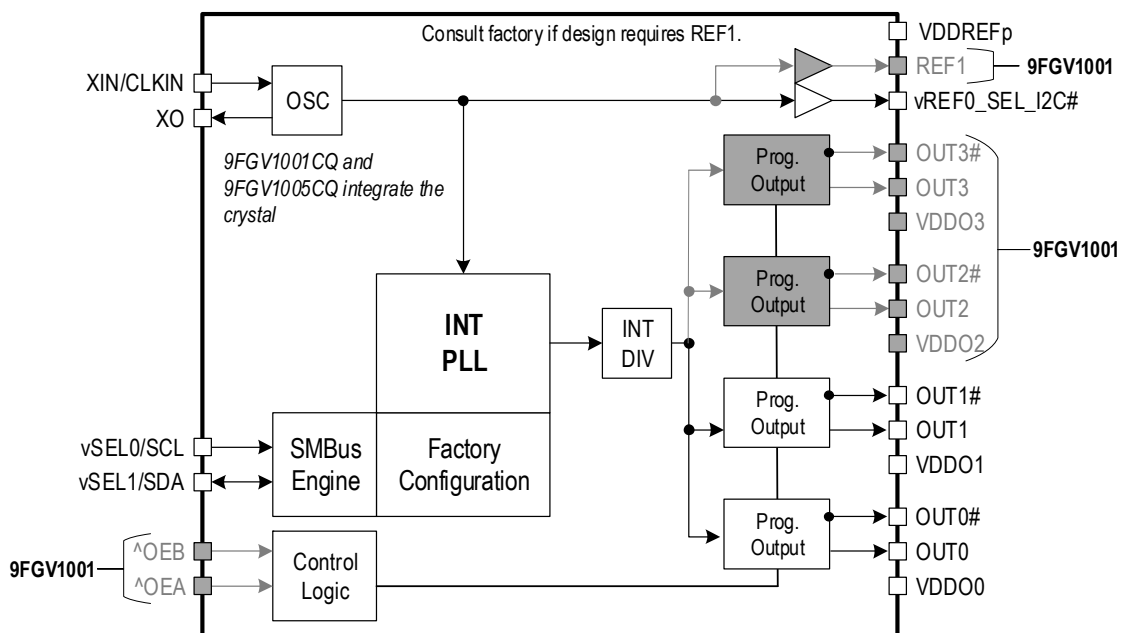
PCIe Cloning Architectures

- Common Clocked (CC)
- Independent Reference without spread spectrum (SRnS)

Output Features

- 9FGV1001: 4 programmable output pairs plus 2 REF outputs
- 9FGV1005: 2 programmable output pairs plus 1 REF output
- 1 integer output frequency per configuration
- 1MHz–325MHz differential outputs
- 1MHz–200MHz single-ended outputs

Block Diagram



Features

- 1.8V to 3.3V power supplies
- Individual 1.8V to 3.3V V_{DDO} for each output pair
- Supports HCSL, LVDS and LVCMOS I/O standards
- HCSL utilizes Renesas' LP-HCSL technology for improved performance, lower power and higher integration:
 - Programmable output impedance of 85Ω or 100Ω
- Supports LVPECL and CML logic with easy AC coupling. See application note [AN-891](#) for alternate terminations
- On-board OTP supports up to 4 complete configurations
- Configuration selected via strapping pins or I²C
- Internal crystal load capacitors
- < 125mW at 1.8V, LP-HCSL outputs at 100MHz (9FGV1001C)
- < 100mW at 1.8V, LP-HCSL outputs at 100MHz (9FGV1005C)
- 4 programmable I²C addresses: D0, D2, D4, D6
- Easily configured with Renesas [Timing Commander™](#) software or Web Configuration tool
- 4 × 4 mm 24-VFQFPN and 24-LGA packages (9FGV1001)
- 3 × 3 mm 16-LGA package (9FGV1005)
- Integrated crystal option available

Key Specifications

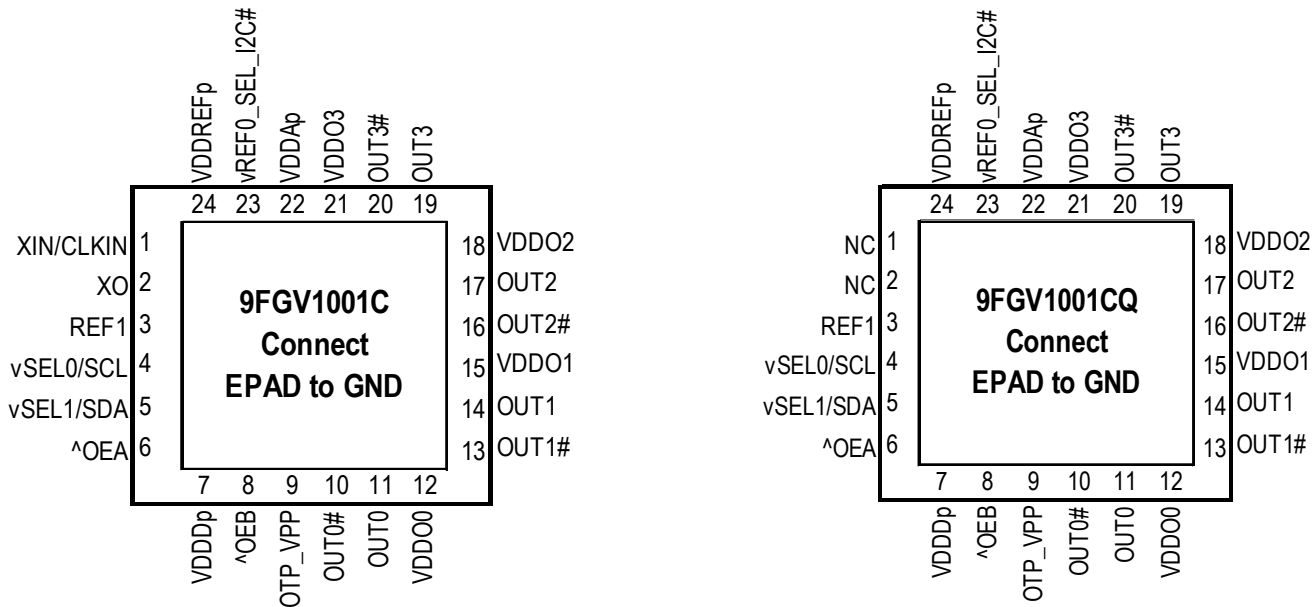
- 261fs RMS 12kHz–20MHz typical phase jitter at 156.25M Hz
- PCIe Gen5 jitter (CC) < 0.08ps RMS
- PCIe Gen5 jitter (SRNS) < 0.07ps RMS

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9FGV1001 Pin Assignments and Descriptions

Figure 1. Pin Assignments for 9FGV1001C 4 x 4 mm 24-VFQFPN and 24-LGA Packages – Top View



4 x 4 mm 24-VFQFPN, 0.5mm pitch

^ prefix indicates internal pull-up resistor
 v prefix indicates internal pull-down resistor

4 x 4 mm 24-LGA, 0.5mm pitch

^ prefix indicates internal pull-up resistor
 v prefix indicates internal pull-down resistor

Table 1. 9FGV1001C Pin Descriptions^[a]

| Number | Name | Type | Description |
|------------------|-----------|--------|---|
| 1 ^[b] | XIN/CLKIN | Input | Crystal input or reference clock input. |
| 2 ^[b] | XO | Output | Crystal output. |
| 3 | REF1 | Output | LVC MOS reference output. |
| 4 | vSEL0/SCL | Input | Select pin for internal frequency configurations/I ² C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down. |
| 5 | vSEL1/SDA | I/O | Select pin for internal frequency configurations/I ² C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down. |
| 6 | ^OEA | Input | Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs. |
| 7 | VDDDp | Power | Digital power. Connect to 1.8V, 2.5V or 3.3V. |
| 8 | ^OEB | Input | Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs. |
| 9 | OTP_VPP | Power | Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V _{DD} . |
| 10 | OUT0# | Output | Complementary output clock 0. |
| 11 | OUT0 | Output | Output clock 0. |
| 12 | VDDO0 | Power | Power supply for output 0. |
| 13 | OUT1# | Output | Complementary output clock 1. |

Table 1. 9FGV1001C Pin Descriptions^[a] (Cont.)

| Number | Name | Type | Description |
|--------|----------------|-------------|--|
| 14 | OUT1 | Output | Output clock 1. |
| 15 | VDDO1 | Power | Power supply for output 1. |
| 16 | OUT2# | Output | Complementary output clock 2. |
| 17 | OUT2 | Output | Output clock 2. |
| 18 | VDDO2 | Power | Power supply for output 2. |
| 19 | OUT3 | Output | Output clock 3. |
| 20 | OUT3# | Output | Complementary output clock 3. |
| 21 | VDDO3 | Power | Power supply for output 3. |
| 22 | VDDAp | Power | Analog power. Connect to same voltage as VDDDp, with proper filtering. |
| 23 | vREF0_SEL_I2C# | Latched I/O | Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I ² C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA. |
| 24 | VDDREFp | Power | Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V. |
| 25 | EPAD | GND | Connect to ground. |

[a] Unused outputs can be programmed off and left floating. Output supplies V_{DDREF} and V_{DDO2} have to be connected. If OUT0 is used, V_{DDO1} must also be connected.

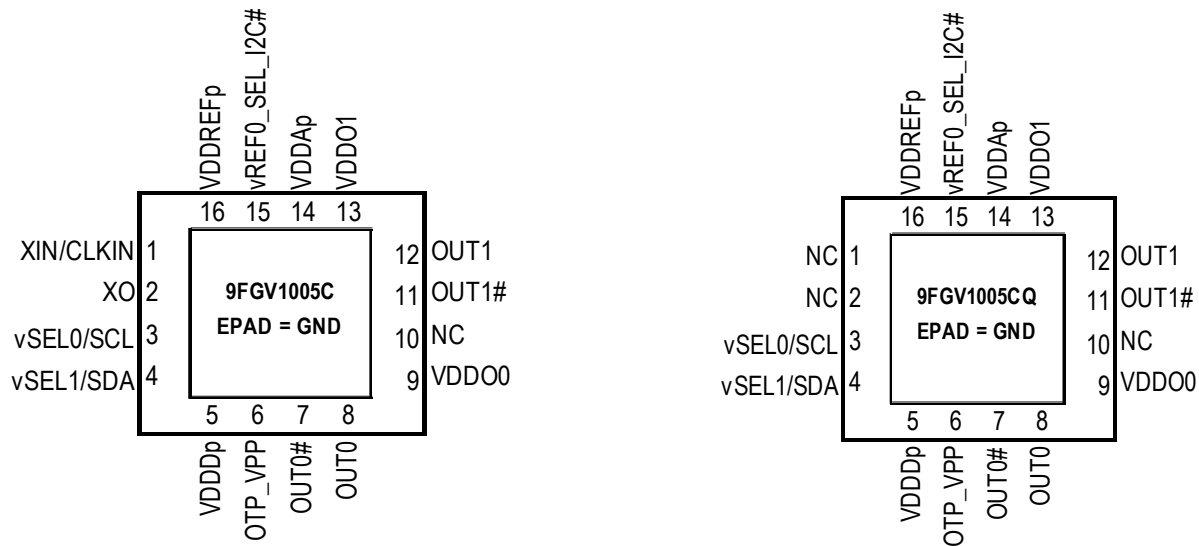
[b] These pins are 'No Connect' on 9FGV1001CQ integrated quartz versions and should have no stubs.

Table 2. 9FGV1001 OE Mapping

| OE[B:A] | OUT0 | OUT1 | OUT2 | OUT3 | REF0 | REF1 |
|---------|---------|---------|---------|---------|---------|---------|
| 00 | Running | Stopped | Stopped | Stopped | Running | Running |
| 01 | Running | Running | Stopped | Stopped | Running | Running |
| 10 | Running | Running | Running | Stopped | Running | Running |
| 11 | Running | Running | Running | Running | Running | Running |

9FGV1005 Pin Assignments and Descriptions

Figure 2. Pin Assignments for 9FGV1005C 3 x 3 mm 16-LGA Package – Top View



16-LGA 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

16-LGA 3 x 3 mm, 0.5mm pitch

^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

Table 3. 9FGV1005C Pin Descriptions^[a]

| Number | Name | Type | Description |
|------------------|-----------|--------|---|
| 1 ^[b] | XIN/CLKIN | Input | Crystal input or reference clock input. |
| 2 ^[b] | XO | Output | Crystal output. |
| 3 | vSEL0/SCL | Input | Select pin for internal frequency configurations/I ² C Clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down. |
| 4 | vSEL1/SDA | I/O | Select pin for internal frequency configurations/I ² C Data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down. |
| 5 | VDDDp | Power | Digital power. Connect to 1.8V, 2.5V or 3.3V. |
| 6 | OTP_VPP | Power | Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V _{DD} . |
| 7 | OUT0# | Output | Complementary output clock 0. |
| 8 | OUT0 | Output | Output clock 0. |
| 9 | VDDO0 | Power | Power supply for output 0. |
| 10 | NC | N/A | No connection. |
| 11 | OUT1# | Output | Complementary output clock 1. |
| 12 | OUT1 | Output | Output clock 1. |
| 13 | VDDO1 | Power | Power supply for output 1. |
| 14 | VDDAp | Power | Analog power. Connect to same voltage as VDDDp, with proper filtering. |

Table 3. 9FGV1005C Pin Descriptions^[a] (Cont.)

| Number | Name | Type | Description |
|--------|----------------|-------------|--|
| 15 | vREF0_SEL_I2C# | Latched I/O | Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I ² C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA. |
| 16 | VDDREFp | Power | Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V. |
| 17 | EPAD | GND | Connect to ground. |

[a] Unused outputs can be programmed off and left floating. Output supplies V_{DDREF} and V_{DDO1} have to be connected. This means that if only one output is to be used, it must be OUT1. If OUT0 is used, pin 10 must be connected. They may share the same power filter.

[b] These pins are 'No Connect' on 9FGV1005CQ integrated quartz version and should have no stubs.

Phase Noise Plots

Figure 3. 9FGV1001C Phase Noise Plot, 3.3V, 25°C

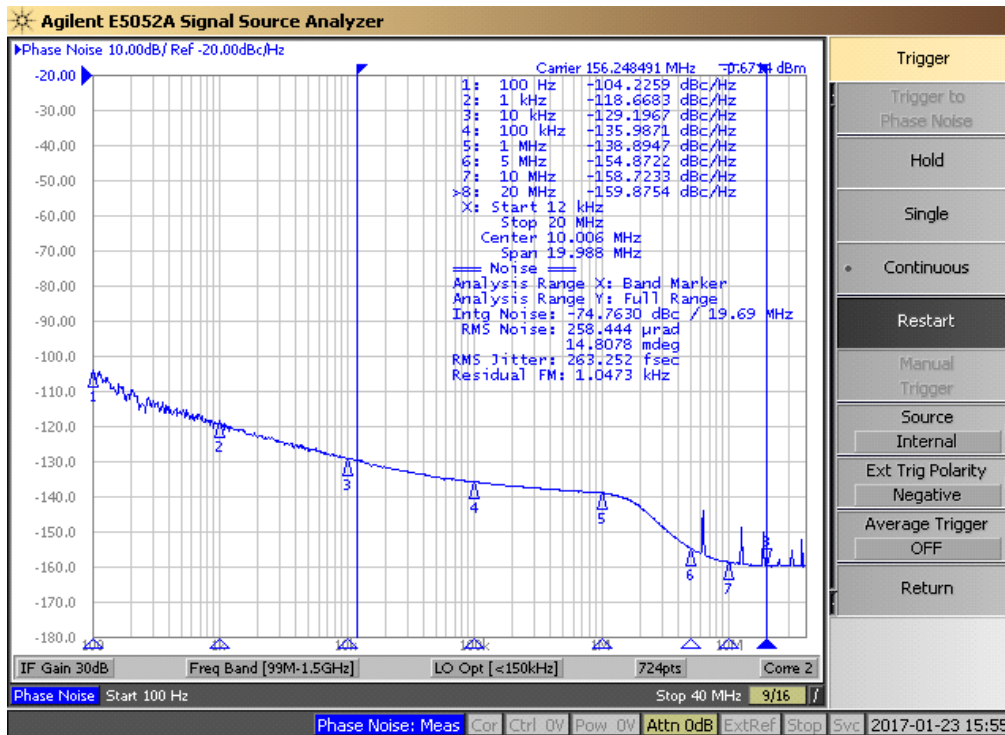
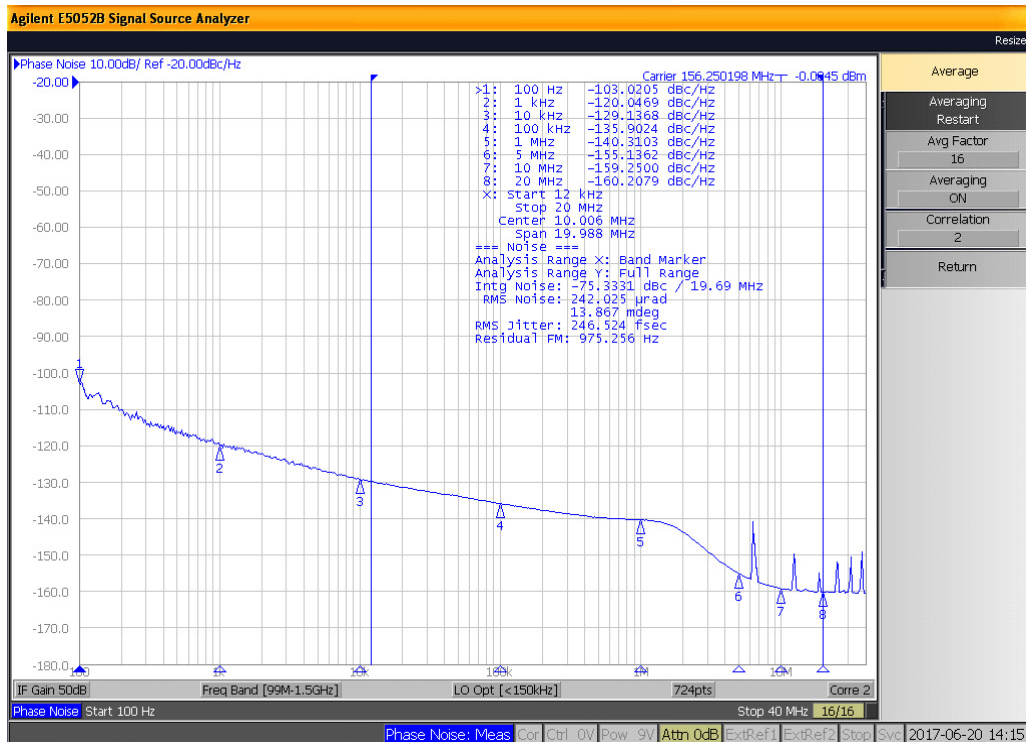


Figure 4. 9FGV1005C Phase Noise Plot, 3.3V, 25°C



Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1001C / 9FGV1005C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 4. Absolute Maximum Ratings

| Parameter | Rating |
|---|---------------------------|
| Supply Voltage, V_{DDA} , V_{DDD} , V_{DDO} | 3.9V |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |
| Inputs | |
| XIN/CLKIN | 0V to 1.2V voltage swing |
| Other Inputs | -0.5V to V_{DDD} |
| Outputs | |
| Outputs, V_{DDO} (LVCMOS) | -0.5V to $V_{DDO} + 0.5V$ |
| Outputs, IO (SDA) | 10mA |

Recommended Operating Conditions

Table 5. Recommended Operating Conditions^[a]

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|------------|---|---------|---------|---------|------|
| V_{DDOx} | Power supply voltage for supporting 1.8V outputs. | 1.71 | 1.8 | 1.89 | V |
| | Power supply voltage for supporting 2.5V outputs. | 2.375 | 2.5 | 2.625 | V |
| | Power supply voltage for supporting 3.3V outputs. | 3.135 | 3.3 | 3.465 | V |
| V_{DDD} | Power supply voltage for core logic functions. | 1.71 | – | 3.465 | V |
| V_{DDA} | Analog power supply voltage. Use filtered analog power supply if available. | 1.71 | – | 3.465 | V |
| T_A | Operating temperature, ambient. | -40 | – | 85 | °C |
| C_L | Maximum load capacitance (3.3V LVCMOS only). | – | – | 15 | pF |
| t_{PU} | Power-up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic). | 0.05 | – | 5 | ms |

[a] All electrical characteristics are specified over these conditions unless noted.

Electrical Characteristics

Table 6. Common Electrical Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--------------------------------|--|---|---------------------------|---------|--------------------------|--------|
| f _{IN} | Input Frequency | Crystal input frequency ^[a] . | 8 | – | 50 | MHz |
| | | CLKIN input frequency ^[b] . | 1 | – | 240 | MHz |
| f _{OUT} | Output Frequency | Differential clock output (LVDS/LP-HCSL). | 1 | – | 325 | MHz |
| | | Single-ended clock output (LVCMOS). | 1 | – | 200 | MHz |
| f _{VCO} | VCO Frequency | VCO operating frequency range. | 2400 | 2500 | 2600 | MHz |
| f _{BW} | Loop Bandwidth | Input frequency = 25MHz. | 0.06 | – | 0.9 | MHz |
| V _{IH} | Input High Voltage | SEL[1:0]. | 0.7 x V _{DDD} | – | V _{DDD} + 0.3 | V |
| V _{IL} | Input Low Voltage | SEL[1:0]. | GND - 0.3 | – | 0.8 | V |
| V _{IH} | Input High Voltage | REF/SEL_I2C#. | 0.65 x V _{DDREF} | – | V _{DDREF} + 0.3 | V |
| V _{IL} | Input Low Voltage | REF/SEL_I2C#. | -0.3 | – | 0.4 | V |
| V _{IH} | Input High Voltage | XIN/CLKIN. | 0.8 | – | 1.2 | V |
| V _{IL} | Input Low Voltage | XIN/CLKIN. | -0.3 | – | 0.4 | V |
| T _R /T _F | Input Rise/Fall Time | OEA, OEB (when present). | – | – | 10 | ns |
| | | SEL1/SDA, SEL0/SCL. | – | – | 300 | |
| C _{IN} | Input Capacitance | SEL[1:0]. | – | 3 | 7 | pF |
| R _{UP} | Internal Pull-up Resistor | | 200 | 237 | 300 | kΩ |
| R _{DOWN} | Internal Pull-down Resistor | | 200 | 237 | 300 | kΩ |
| C _L | Programmable Capacitance at XIN and XO (XIN in parallel with XO) | XIN/CLKIN, XO. | 0 | | 8 | pF |
| t ₂ | Input Duty Cycle | CLKIN, measured at V _{DDREF} /2. | 40 | 50 | 60 | % |
| t ₃ | Output Duty Cycle | LVCMOS, f _{OUT} > 156.25MHz. | 40 | 50 | 60 | % |
| | | LVCMOS, f _{OUT} ≤ 156.25MHz. | 45 | 50 | 55 | % |
| | | LVDS, LP-HCSL outputs. | 45 | 50.2 | 55 | % |
| t ₆ | Clock Jitter (9FGV1001) ^[c] | Cycle-to-cycle jitter (Peak-to-Peak), See Test Frequencies for Jitter Measurements for configurations. | – | 28 | – | ps |
| | | Reference clock RMS phase jitter (12kHz to 20MHz integration range). See Test Frequencies for Jitter Measurements for configurations. | – | 338 | – | fs rms |
| | | OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See Test Frequencies for Jitter Measurements for configurations. | – | 261 | – | fs rms |

Table 6. Common Electrical Characteristics (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|--------|---|---|---------|---------|---------|--------|
| t6 | Clock Jitter (9FGV1005) ^[c] | Cycle-to-cycle jitter (Peak-to-Peak). See Test Frequencies for Jitter Measurements for configurations. | – | 30 | – | ps |
| | | Reference clock RMS phase jitter (12kHz to 5MHz integration range). See Test Frequencies for Jitter Measurements for configurations. | – | 357 | – | fs rms |
| | | OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See Test Frequencies for Jitter Measurements for configurations. | – | 284 | – | fs rms |
| t7 | Output Skew | All outputs using the same driver format and V _{DDO} voltage. (9FGV1001). | – | 105 | 135 | ps |
| | | All outputs using the same driver format and V _{DDO} voltage. (9FGV1005). | – | 37 | 50 | |
| t8a | Lock Time ^[d] ^[e] | PLL outputs valid from V _{DDs} ≥ 1.5V. | – | 5 | 10 | ms |
| t8b | | REF outputs valid from V _{DDs} ≥ 1.5V. | – | 5 | 11 | |

[a] Practical lower frequency is determined by loop filter settings.

[b] Input doubler off. Maximum input frequency with input doubler on is 160MHz.

[c] Actual jitter is configuration dependent. These values are representative of what the device can achieve.

[d] Includes loading the configuration bits from OTP to registers when the configuration number is changed.

[e] Actual PLL output valid time depends on the loop configuration.

Table 7. Test Frequencies for Jitter Measurements

| XIN/CLKIN | OUT0 | OUT1 | OUT2 | OUT3 | Unit |
|-----------|--|------|------|------|------|
| 50 | 156.25 ^[a] ^[b] | | | | MHZ |
| | 100 ^[a] ^[c] ^[d] | | | | MHZ |

[a] Outputs configured as LP-HCSL or LVDS with REF output off unless noted.

[b] This configuration used for 12kHz-20MHz OUT phase jitter measurement. REF off, SSC off.

[c] This configuration used for 12kHz-20MHz REF phase jitter measurement, SSC Off.

[d] This configuration used for PCIe RefClk phase jitter measurements.

Table 8. PCIe Refclk Phase Jitter^{[a] [b] [c]}

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Specification Limits | Unit |
|--------------------|--|--|---------|---------|---------|----------------------|----------|
| $t_{jphPCleG1-CC}$ | PCIe Phase Jitter (Common Clocked Architecture) | PCIe Gen1 (2.5 GT/s) | – | 2.35 | 4.84 | 86 | ps (p-p) |
| $t_{jphPCleG2-CC}$ | | PCIe Gen2 Hi Band (5.0 GT/s) | – | 0.13 | 0.22 | 3 | ps (RMS) |
| | | PCIe Gen2 Lo Band (5.0 GT/s) | – | 0.05 | 0.08 | 3.1 | ps (RMS) |
| $t_{jphPCleG3-CC}$ | | PCIe Gen3 (8.0 GT/s) ^[d] | – | 0.07 | 0.12 | 1 | ps (RMS) |
| $t_{jphPCleG4-CC}$ | | PCIe Gen4 (16.0 GT/s) ^{[d] [e]} | – | 0.07 | 0.12 | 0.5 | ps (RMS) |
| $t_{jphPCleG5-CC}$ | | PCIe Gen5 (32.0 GT/s) ^{[d] [f]} | – | 0.03 | 0.05 | 0.15 | ps (RMS) |
| $t_{jphPCleG1-IR}$ | PCIe Phase Jitter (IR Architecture) ^[g] | PCIe Gen1 (2.5 GT/s) | – | 0.24 | 0.34 | N/A | ps (RMS) |
| $t_{jphPCleG2-IR}$ | | PCIe Gen2 (5.0 GT/s) | – | 0.18 | 0.28 | N/A | ps (RMS) |
| $t_{jphPCleG3-IR}$ | | PCIe Gen3 (8.0 GT/s) | – | 0.05 | 0.08 | N/A | ps (RMS) |
| $t_{jphPCleG4-IR}$ | | PCIe Gen4 (16.0 GT/s) | – | 0.05 | 0.08 | N/A | ps (RMS) |
| $t_{jphPCleG5-IR}$ | | PCIe Gen5 (32.0 GT/s) | – | 0.04 | 0.07 | N/A | ps (RMS) |

[a] See [Test Loads](#) for details.

[b] The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

[c] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83.

[d] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[e] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[f] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[g] The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate IR jitter values, however, it does not provide specification limits, hence the “N/A” in the Limit column. IR values are informative only. In general, a clock operating in an IR system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. And additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the CC ref clock jitter limits, and the case can be made for dividing the CC channel simulation values by $\sqrt{2}$, if the ref clock is close to the clock input. An example for Gen4 is as follows: A rule-of-thumb IR limit would be either $0.5ps\ RMS/\sqrt{2} = 0.35ps\ RMS$, or $0.7ps\ RMS/\sqrt{2} = 0.5ps\ RMS$, depending on the distance between the clock generator and the Tx or Rx clock input.

Table 9. Low-Power (LP) HCSL Differential Output Electrical Characteristics^[a]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------------|------------------------|---|---------|---------|---------|------|
| $T_{R/F}$ | Slew Rate | Scope averaging on. ^{[b] [c]} | 1.25 | 2.5 | 4 | V/ns |
| $\Delta T_{R/F}$ | Slew Rate Matching | ^{[d] [e]} | – | 9 | 20 | % |
| V_{CROSS} | Crossing Voltage (abs) | Scope averaging off. ^{[d] [e] [f]} | 250 | 424 | 550 | mV |

Table 9. Low-Power (LP) HCSL Differential Output Electrical Characteristics^[a] (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------------------|-------------------------------|--|---------|---------|---------|------|
| ΔV_{CROSS} | Crossing Voltage (var) | Scope averaging off. ^{[d] [e] [g]} | – | 16 | 140 | mV |
| $T_{\text{PERIOD_AVG}}$ | Average Clock Period Accuracy | Outputs set to 100MHz for PCIe applications. SSC off. ^{[b] [h] [i] [j]} | -100 | 0 | +100 | |
| V_{MAX} | Absolute Maximum Voltage | Includes 300mV of overshoot (Vovs). ^{[d] [k] [l]} | 660 | 808 | 1150 | mV |
| V_{MIN} | Absolute Minimum Voltage | Includes -300mV of undershoot (Vuds). ^{[d] [l] [m]} | -300 | -54 | 150 | mV |

[a] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. See [Test Loads](#) for details.

[b] Measured from differential waveform.

[c] Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[d] Measured from single-ended waveform.

[e] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a $\pm 75\text{mV}$ window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[f] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[g] Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[h] Refer to Section 8.6 of the PCI Express Base Specification, Revision 5.0 for information regarding PPM considerations.

[i] PCIe Gen1 through Gen4 specify $\pm 300\text{ppm}$ frequency tolerances. PCIe Gen5 specifies $\pm 100\text{ppm}$ frequency tolerances and the 9FGV100x devices already meet this.

[j] “ppm” refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of $100\text{Hz/ppm} \times 100\text{ppm} = 10\text{kHz}$. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The $\pm 100\text{ppm}$ applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

[k] Defined as the maximum instantaneous voltage including overshoot.

[l] At default amplitude settings.

[m] Defined as the minimum instantaneous voltage including undershoot.

Table 10. 9FGV1001C Current Consumption^[a]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------------|--|--|---------|---------|---------|------|
| I _{DDREF} | VDDREF Supply Current | 50MHz REFCLK. | – | 4 | 6 | mA |
| I _{DDCORE} | Core Supply Current ^[b] | 2500MHz VCO, 50MHz REFCLK. | – | 23 | 29 | |
| I _{DDOx} | Output Buffer Supply Current V _{DDO2} (includes output divider) | LVDS, 325MHz. | – | 19 | 24 | |
| | | LP-HCSL, 100MHz. | – | 16 | 20 | |
| | | LVC MOS, 50MHz ^[c] . | – | 15 | 19 | |
| | | LVC MOS, 200MHz ^[c] . | – | 24 | 37 | |
| | Output Buffer Supply Current (V _{DDO0} , V _{DDO1} , V _{DDO3} – per output) | LVDS, 325MHz. | – | 7 | 10 | |
| | | LP-HCSL, 100MHz. | – | 6 | 8 | |
| | | LVC MOS, 50MHz ^[c] . | – | 4 | 7 | |
| | | LVC MOS, 200MHz ^[c] . | – | 13 | 24 | |
| I _{DDPD} | Total Power Down Current ^[b] | Programmable outputs, HCSL mode, B37[0] = 0. | – | 9 | 12 | |
| | | Programmable outputs in LVDS mode, B37[0] = 0. | – | 24 | 30 | |
| | | Programmable outputs in LVC MOS1 mode, B37[0] = 0. | – | 4 | 7 | |

[a] See [Test Loads](#) for details.

[b] I_{DDCORE} = I_{DDA} + I_{DDDIG}.

[c] Single CMOS driver active for each output pair.

Table 11. 9FGV1005C Current Consumption [a]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------------|---|--|---------|---------|---------|------|
| I _{DDREF} | VDDREF Supply Current | 50MHz REFCLK. | – | 5 | 8 | mA |
| I _{DDCORE} | Core Supply Current [b] | 2500MHz VCO, 50MHz REFCLK. | – | 24 | 30 | |
| I _{DDOx} | Output Buffer Supply Current V _{DDO1} (includes output divider) | LVDS, 325MHz. | – | 22 | 27 | |
| | | LP-HCSL, 100MHz. | – | 17 | 23 | |
| | | LVC MOS, 50MHz [c]. | – | 15 | 19 | |
| | | LVC MOS, 200MHz [c]. | – | 25 | 39 | |
| | Output Buffer Supply Current – V _{DDO0} | LVDS, 325MHz. | – | 8 | 11 | |
| | | LP-HCSL. | – | 6 | 9 | |
| | | LVC MOS, 50MHz [c]. | – | 4 | 7 | |
| I _{DDPD} | Total Power Down Current [b] | Programmable outputs in HCSL mode, B37[0] = 0. | – | 7 | 10 | |
| | | Programmable outputs in LVDS mode, B37[0] = 0. | – | 16 | 20 | |
| | | Programmable outputs in LVC MOS1 mode, B37[0] = 0. | – | 5 | 7 | |

[a] See [Test Loads](#) for details.

[b] I_{DDCORE} = I_{DDA} + I_{DDD} + I_{DDAO}.

[c] Single CMOS driver active for each output pair.

Table 12. LVC MOS Output Electrical Characteristics [a]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-------------------|------------------------------|--|------------------------|---------|------------------|------|
| S _R | Slew Rate | 3.3V ±5%, 20% to 80% of V _{DDO} (output load = 4.7pF). | 2.6 | 3.7 | 4.7 | V/ns |
| | | 2.5V ±5%, 20% to 80% of V _{DDO} (output load = 4.7pF). | 1.5 | 2.4 | 4.7 | |
| | | 1.8V ±5%, 20% to 80% of V _{DDO} (output load = 4.7pF). | 1.0 | 1.7 | 3.2 | |
| V _{OH} | Output High Voltage | I _{OH} = -15mA at 3.3V. | 0.8 x V _{DDO} | – | V _{DDO} | V |
| | | I _{OH} = -12mA at 2.5V. | | | | |
| | | I _{OH} = -8mA at 1.8V. | | | | |
| V _{OL} | Output Low Voltage | I _{OL} = 15mA at 3.3V. | – | 0.22 | 0.4 | V |
| | | I _{OL} = 12mA at 2.5V. | – | | | |
| | | I _{OL} = 8mA at 1.8V. | – | | | |
| I _{OZDD} | Output Leakage Current | Outputs, tri-stated, V _{DDO} , V _{DDREF} = 3.465V. | – | 0 | 5 | µA |
| R _{OUT} | CMOS Output Driver Impedance | T _A = 25°C. | – | 17 | – | Ω |

[a] See [Test Loads](#) for details.

Table 13. LVDS Output Electrical Characteristics^[a]

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---------------------|---|---------|---------|---------|------|
| V _{OT} (+) | Differential Output Voltage for the TRUE Binary State | 247 | 328 | 454 | mV |
| V _{OT} (-) | Differential Output Voltage for the FALSE Binary State | -454 | -332 | -247 | mV |
| ΔV _{OT} | Change in V _{OT} between Complementary Output States | – | – | 50 | mV |
| V _{OS} | Output Common Mode Voltage (Offset Voltage) at 3.3V +5% and 2.5V +5% | 1.125 | 1.19 | 1.55 | V |
| V _{OS} | Output Common Mode Voltage (Offset Voltage) at 1.8V +5% | 0.8 | 0.86 | 0.95 | V |
| ΔV _{OS} | Change in V _{OS} between Complementary Output States | – | 0 | 50 | mV |
| I _{OS} | Outputs Short Circuit Current, V _{OUT+} or V _{OUT-} = 0V or V _{DD} | – | 6 | 12 | mA |
| I _{OSD} | Differential Outputs Short Circuit Current, V _{OUT+} = V _{OUT-} | – | 3 | 12 | mA |
| T _R | Rise Times Tested at 20%–80% | – | 257 | 375 | ps |
| T _F | Fall Times Tested at 80%–20% | – | 287 | 375 | ps |

[a] See [Test Loads](#) for details.

I²C Bus Characteristics

Table 14. I²C Bus DC Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------------|-----------------------|------------------------|-------------------------|---------|------------------------|------|
| V _{IH} | Input High Level | – | 0.7 × V _{DDD} | – | – | V |
| V _{IL} | Input Low Level | – | – | – | 0.3 × V _{DDD} | V |
| V _{HYS} | Hysteresis of Inputs | – | 0.05 × V _{DDD} | – | – | V |
| I _{IN} | Input Leakage Current | – | -1 | – | 30 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 3mA. | – | – | 0.4 | V |

Table 15. I²C Bus AC Characteristics^[a]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-----------------------|--------------------------------------|------------|---------------------------|---------|---------|------|
| F _{SCLK} | Serial Clock Frequency (SCL) | – | 10 | – | 400 | kHz |
| t _{BUF} | Bus Free Time between STOP and START | – | 1.3 | – | – | μs |
| t _{SU:START} | Setup Time, START | – | 0.6 | – | – | μs |
| t _{HD:START} | Hold Time, START | – | 0.6 | – | – | μs |
| t _{SU:DATA} | Setup Time, Data Input (SDA) | – | 0.1 | – | – | μs |
| t _{HD:DATA} | Hold Time, Data Input (SDA) | – | 0 | – | – | μs |
| t _{OVD} | Output Data Valid from Clock | – | – | – | 0.9 | μs |
| C _B | Capacitive Load for Each Bus Line | – | – | – | 400 | pF |
| t _R | Rise Time, Data and Clock (SDA, SCL) | – | 20 + 0.1 × C _B | – | 300 | ns |
| t _F | Fall Time, Data and Clock (SDA, SCL) | – | 20 + 0.1 × C _B | – | 300 | ns |

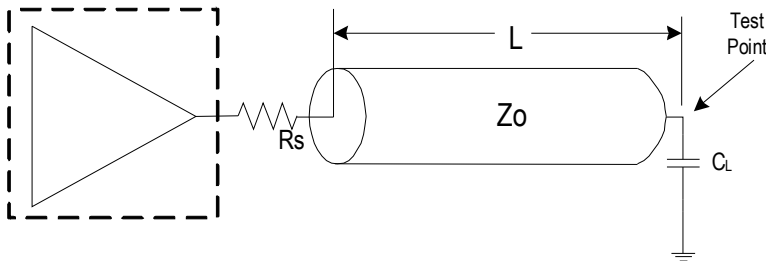
Table 15. I²C Bus AC Characteristics^[a] (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------------|------------------------|------------|---------|---------|---------|------|
| t _{HIGH} | HIGH Time, Clock (SCL) | – | 0.6 | – | – | μs |
| t _{LOW} | LOW Time, Clock (SCL) | – | 1.3 | – | – | μs |
| t _{SU:STOP} | Setup Time, STOP | – | 0.6 | – | – | μs |

[a] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IH(MIN)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Test Loads

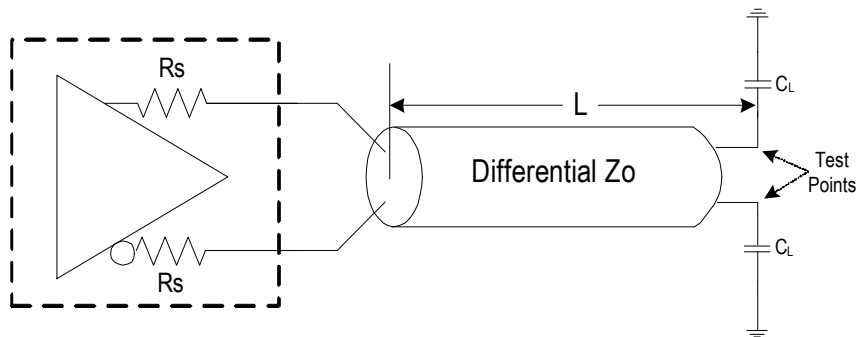
Figure 5. LVCMOS AC/DC Test Load



| Rs | Zo | L | CL |
|-----|-----|----------|-------|
| 33Ω | 50Ω | 5 inches | 4.7pF |

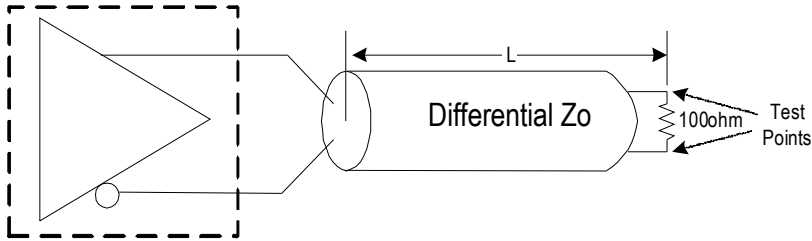
Figure 6. LP-HCSL AC/DC Test Load

(Standard PCIe source-terminated test load)



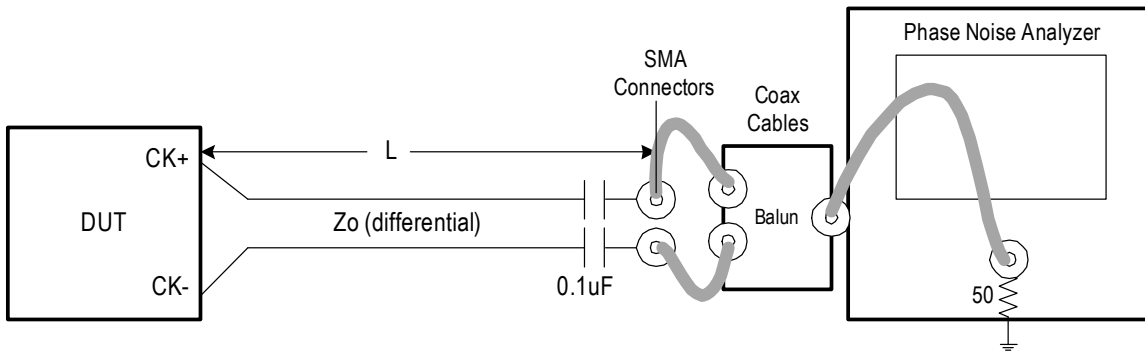
| Rs | Zo | L | CL |
|----------|------|----------|-----|
| Internal | 100Ω | 5 inches | 2pF |
| Internal | 85Ω | 5 inches | 2pF |

Figure 7. LVDS AC/DC Test Load



| R_s | Z_o | L | C_L |
|-------|-------|----------|-------|
| N/A | 100Ω | 5 inches | N/A |

Figure 8. Test Setup for PCIe Measurement Using a Phase Noise Analyzer



| R_s | Z_o | L | C_L |
|----------|-------|----------|-------|
| Internal | 100Ω | 5 inches | N/A |

Crystal Characteristics

Table 16. Recommended Crystal Characteristics

| Parameter | Value | Unit |
|---|-------------|-------------|
| Frequency | 8–50 | MHz |
| Resonance Mode | Fundamental | – |
| Frequency Tolerance at 25°C | ±20 | ppm maximum |
| Frequency Stability, REF at 25°C Over Operating Temperature Range | ±20 | ppm maximum |
| Temperature Range (commercial) | 0–70 | °C |
| Temperature Range (industrial) | -40 to 85 | °C |
| Equivalent Series Resistance (ESR) | 50 | Ω maximum |
| Shunt Capacitance (C _O) | 7 | pF maximum |
| Load Capacitance (C _L) | 8 | pF maximum |
| Drive Level | 0.1 | mW maximum |
| Aging Per Year | ±5 | ppm maximum |

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

Thermal Characteristics

Table 17. Thermal Resistance [a]

| Parameter | Symbol | Conditions | Package | Typical Values | Unit |
|--|----------------------------------|----------------------------------|---------|----------------|------|
| Thermal Resistance (devices with external crystal) | θ_{JC} | Junction to case. | NBG24 | 52 | °C/W |
| | θ_{Jb} | Junction to base. | | 2.3 | |
| | θ_{JA0} | Junction to air, still air. | | 44 | |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 37 | |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 33 | |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 32 | |
| | θ_{JC} | Junction to case. | LTG16 | 66 | |
| | θ_{Jb} | Junction to base. | | 5.1 | |
| | θ_{JA0} | Junction to air, still air. | | 63 | |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 56 | |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 51 | |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 49 | |
| Thermal Resistance Q-series (devices with internal crystal) | θ_{JC} | Junction to case. | LTG24 | 57.3 | |
| | θ_{Jb} | Junction to base. | | 24.3 | |
| | θ_{JA0} | Junction to air, still air. | | 79.8 | |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 73.9 | |
| | θ_{JA3} | Junction to air, 3 m/s air flow. | | 69.9 | |
| | θ_{JA5} | Junction to air, 5 m/s air flow. | | 67.3 | |
| | θ_{JC} | Junction to case. | LTG16 | 82.1 | |
| | θ_{Jb} | Junction to base. | | 42.3 | |
| | θ_{JA0} | Junction to air, still air. | | 93.6 | |
| | θ_{JA1} | Junction to air, 1 m/s air flow. | | 87.1 | |
| θ_{JA3} | Junction to air, 3 m/s air flow. | 83.3 | | | |

[a] EPAD soldered to board.

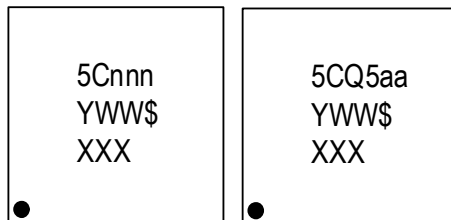
Marking Diagrams

Figure 9. 9FGV1001C Marking Diagrams



- Lines 1 and 2: truncated part number:
 - “nnn” denotes the decimal digits indicating a specific configuration.
 - “aa” denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 3:
 - “#” denotes the stepping number.
 - “YWW” denotes the last digits of the year and week the part was assembled.
 - “**” denotes the lot sequence; “\$” denotes the mark code.

Figure 10. 9FGV1005C Marking Diagrams



- Line 1: truncated part number
 - “nnn” denotes the decimal digits indicating a specific configuration.
 - “aa” denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 2: “YWW” denotes the last digits of the year and week the part was assembled; “\$” denotes mark code.
- Line 3: “XXX” denotes the last three characters of the lot number.

Standard Configurations

Table 18. 9FGV1001C / 9FGV1005C Standard Configurations

| Supply Voltage—all pins (V) | Output Impedance (ohms) | Number of PCIe Clock Outputs | XTAL Frequency (MHz) | Orderable Part Number (Bulk) | Orderable Part Number (Tape and Reel) |
|-----------------------------|-------------------------|------------------------------|----------------------|------------------------------|---------------------------------------|
| 3.3 | 100 | 4 | 25 – external | 9FGV1001C001NBGI | 9FGV1001C001NBGI8 |
| | | | 50 – internal | 9FGV1001CQ505LTGI | 9FGV1001CQ505LTGI8 |
| | | 2 | 25 – external | 9FGV1005C001LTGI | 9FGV1005C001LTGI8 |
| | | | 50 – internal | 9FGV1005CQ505LTGI | 9FGV1005CQ505LTGI8 |
| 1.8 | 100 | 4 | 25 – external | 9FGV1001C002NBGI | 9FGV1001C002NBGI8 |
| | | | 50 – internal | 9FGV1001CQ506LTGI | 9FGV1001CQ506LTGI8 |
| | | 2 | 25 – external | 9FGV1005C002LTGI | 9FGV1005C002LTGI8 |
| | | | 50 – internal | 9FGV1005CQ506LTGI | 9FGV1005CQ506LTGI8 |

Table 19. Common Features of 9FGV1001C / 9FGV1005C Standard Configurations

These common features are collaborative with [Table 18](#).

| Configuration | Output Frequency (MHz) | Output Type | Ref Outputs |
|---------------|------------------------|-------------|-------------|
| 0 | 50 | LP-HCSL | OFF |
| 1 | 100 | | |
| 2 | 125 | | |
| 3 | 156.25 | | |

Table 20. 9FGV1001C / 9FGV1005C Standard Configurations (with 39.0625MHz crystal frequency)

| Supply Voltage—all pins (V) | Output Impedance (ohms) | Number of PCIe Clock Outputs | XTAL Frequency (MHz) | Orderable Part Number (Bulk) | Orderable Part Number (Tape and Reel) |
|-----------------------------|-------------------------|------------------------------|----------------------|------------------------------|---------------------------------------|
| 3.3 | 100 | 4 | 39.0625 – external | 9FGV1001C011NBGI | 9FGV1001C011NBGI8 |
| | | 2 | 39.0625 – external | 9FGV1005C011LTGI | 9FGV1005C011LTGI8 |
| 1.8 | 100 | 4 | 39.0625 – external | 9FGV1001C012NBGI | 9FGV1001C012NBGI8 |
| | | 2 | 39.0625 – external | 9FGV1005C012LTGI | 9FGV1005C012LTGI8 |

Table 21. Common Features of 9FGV1001C / 9FGV1005C Standard Configurations (with 39.0625MHz crystal frequency)

These common features are collaborative with [Table 20](#).

| Configuration | Output Frequency (MHz) | Output Type | Ref Outputs |
|---------------|------------------------|-------------|-------------|
| 0 | 156.25 | LP-HCSL | OFF |
| 1 | 161.1328125 | | |
| 2 | 312.5 | | |
| 3 | 322.265625 | | |

Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature | Crystal |
|-----------------------|---|---------------|--------------|----------------|
| 9FGV1001CnnnNBGI | 4 × 4 mm, 0.5mm pitch 24-VFQFPN | Tray | -40 to +85°C | External |
| 9FGV1001CnnnNBGI8 | | Tape and Reel | | |
| 9FGV1001CQ5aaLTGI | 4 × 4 mm, 0.5mm pitch 24-LGA | Tray | | 50MHz Internal |
| 9FGV1001CQ5aaLTGI8 | | Tape and Reel | | |
| 9FGV1005CnnnLTGI | 3 × 3 mm, 0.5mm pitch 16-LGA | Tray | | External |
| 9FGV1005CnnnLTGI8 | | Tape and Reel | | |
| 9FGV1005CQ5aaLTGI | | Tray | | 50MHz Internal |
| 9FGV1005CQ5aaLTGI8 | | Tape and Reel | | |

“G” indicates RoHS 6.6 compliance.

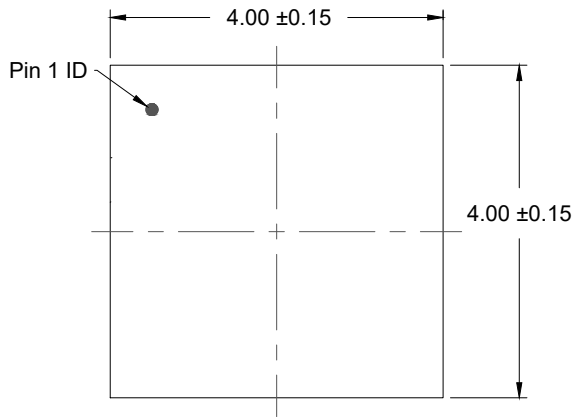
“nnn” are decimal digits indicating a specific configuration.

“aa” are alphanumeric digits indicating a specific configuration.

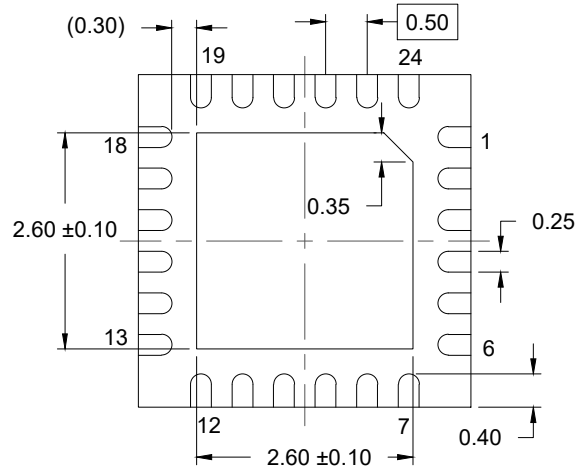
“Q5” indicates internal 50MHz crystal.

Revision History

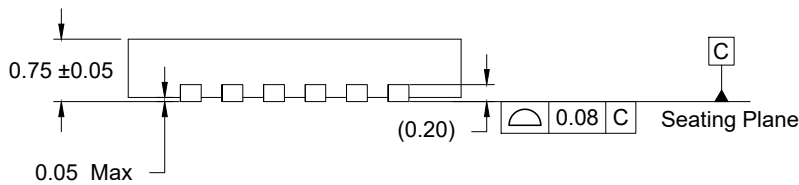
| Revision Date | Description of Change |
|--------------------|---|
| March 29, 2023 | Updated footnote "d" in Table 6 . |
| October 29, 2020 | Updated pin descriptions for VDDAp and VDDDp. |
| September 28, 2020 | Added Standard Configurations section and tables. |
| September 18, 2020 | Corrected typo in Features section from 3 x 3 mm 16-LGA (9FGV1006) to 3 x 3 mm 16-LGA (9FGV1005). |
| August 18, 2020 | Updated 9FGV1005CQ marking diagram. |
| August 14, 2020 | Updated Slew Rate 1.8V minimum value from 0.8 to 1.0V/ns. |
| August 13, 2020 | Updated Carrier Type in Ordering Information table from "Cut-Tape" to "Tray". |
| July 21, 2020 | <ul style="list-style-type: none"> ▪ Merge 9FGV1001 and 9FGV1005 into single data sheet. ▪ Update to device Rev C, SEL0 and SEL1 lines now have internal pull-down resistors. ▪ Add PCIe Gen5 performance specifications. ▪ Updated electrical tables to latest format. |



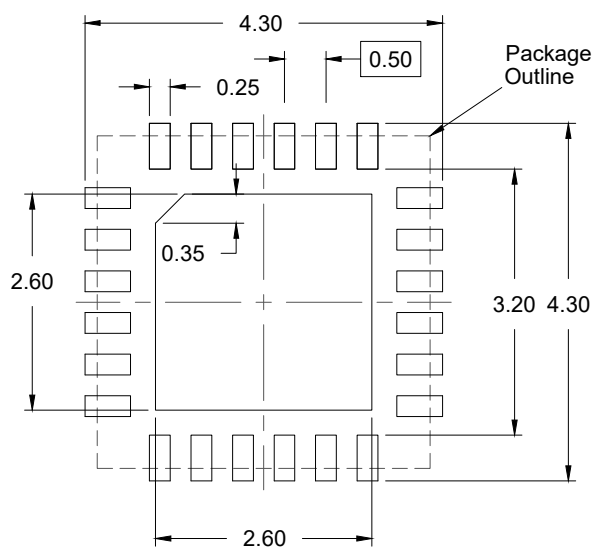
TOP VIEW



BOTTOM VIEW



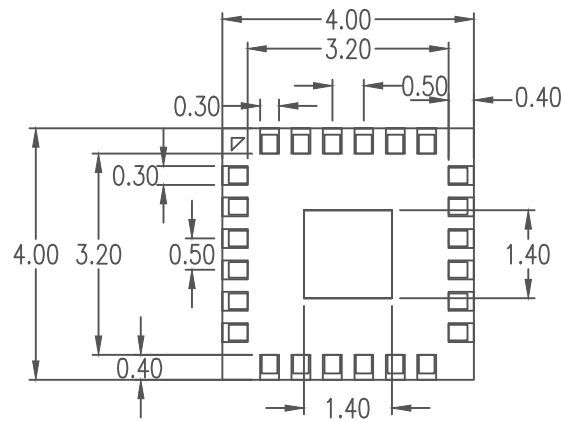
SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.

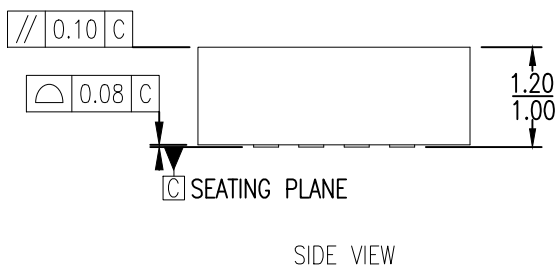
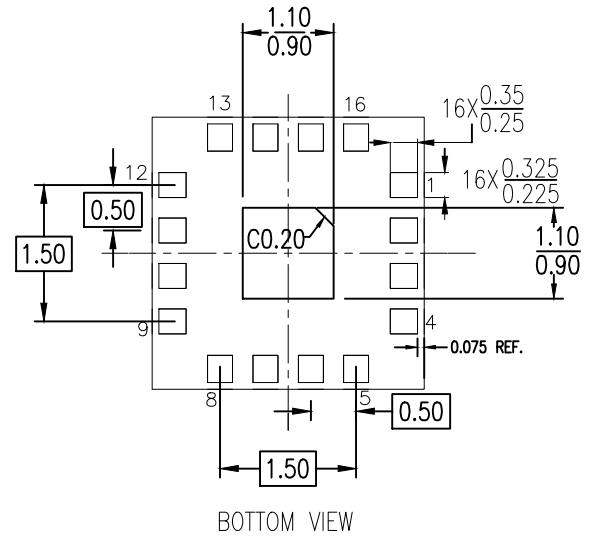
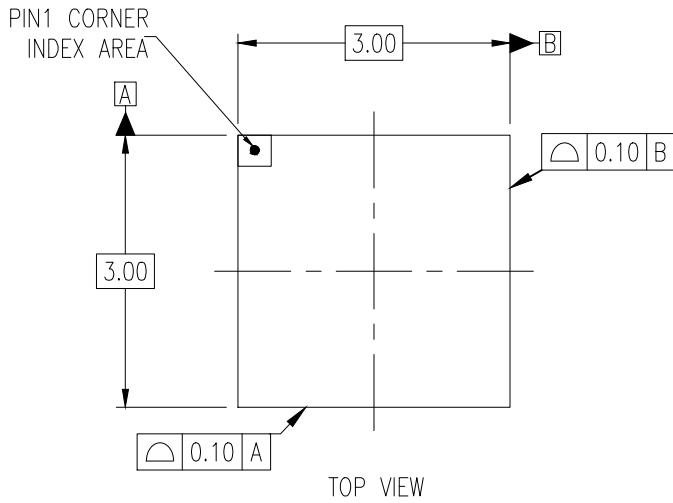


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

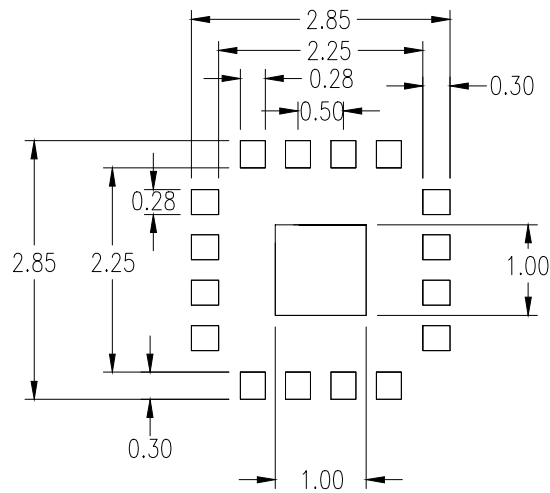
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|--------------------------|---------|-----------------|
| Date Created | Rev No. | Description |
| Sept 15, 2017 | Rev 00 | Initial Release |



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.