Description

The 9ZML1245/9ZML1255/9ZML1256 devices are third generation enhanced performance 2-input, 12-output clock multiplexers. Each input clock has software adjustable input-to-output delay when operating in Zero-Delay (ZDB) mode. The devices also implement an extensive set of features ensuring that clocks are well behaved with today's ever more complex power-up sequencing. The 9ZML1256 has an SMBus Write Lockout pin for increased device and system security.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Key Specifications

- Fanout Buffer Mode additive phase jitter:
  - PCIe Gen5 CC < 15fs RMS
  - DB2000Q additive jitter < 25fs RMS
  - QPI/UPI 11.4GB/s < 40fs RMS
  - IF-UPI additive jitter < 70fs RMS
- ZDB Mode phase jitter:
  - PCIe Gen5 CC < 24fs RMS
  - QPI/UPI 11.4GB/s < 110fs RMS
  - IF-UPI additive jitter < 130fs RMS
- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps

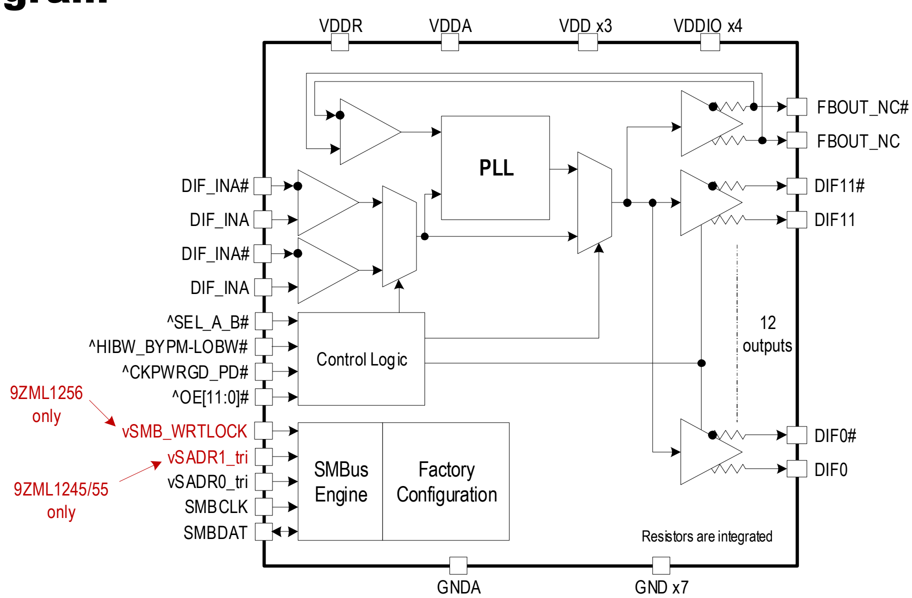
Features

- 12 Low-power HCSL (LP-HCSL) outputs
- Integrated terminations for 85Ω (9ZXL1255/56) and 100Ω (9ZXL1245) systems eliminate up to 4 resistors per output pair
- Flexible Power Sequencing (FPS) configuration via SMBus
- Power Down Tolerant input (PDT); inputs: SEL_A_B#, SADR[1:0]_tri, OE# pins
- Input-to-output delay: 0ps default. Programmable through 360°
- 2 software-configurable input-to-output delay lines
- Dedicated OE# pins support PCIe CLKREQ# function
- Up to 9 selectable SMBus addresses (9ZXL1245/55)
- SMBus Write Protect Pin (9ZXL1256)
- Selectable ZDB bandwidths minimizes jitter peaking in cascaded ZDB topologies
- Hardware/SMBus control of ZDB and FOB modes
- Spread-spectrum compatible
- Up to 400MHz FOB operation
- 100MHz ZDB mode operation
- -40°C to +85°C operating temperature range
- 10 × 10 mm 72-VFQFPN package

Typical Applications

- Servers/High-performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

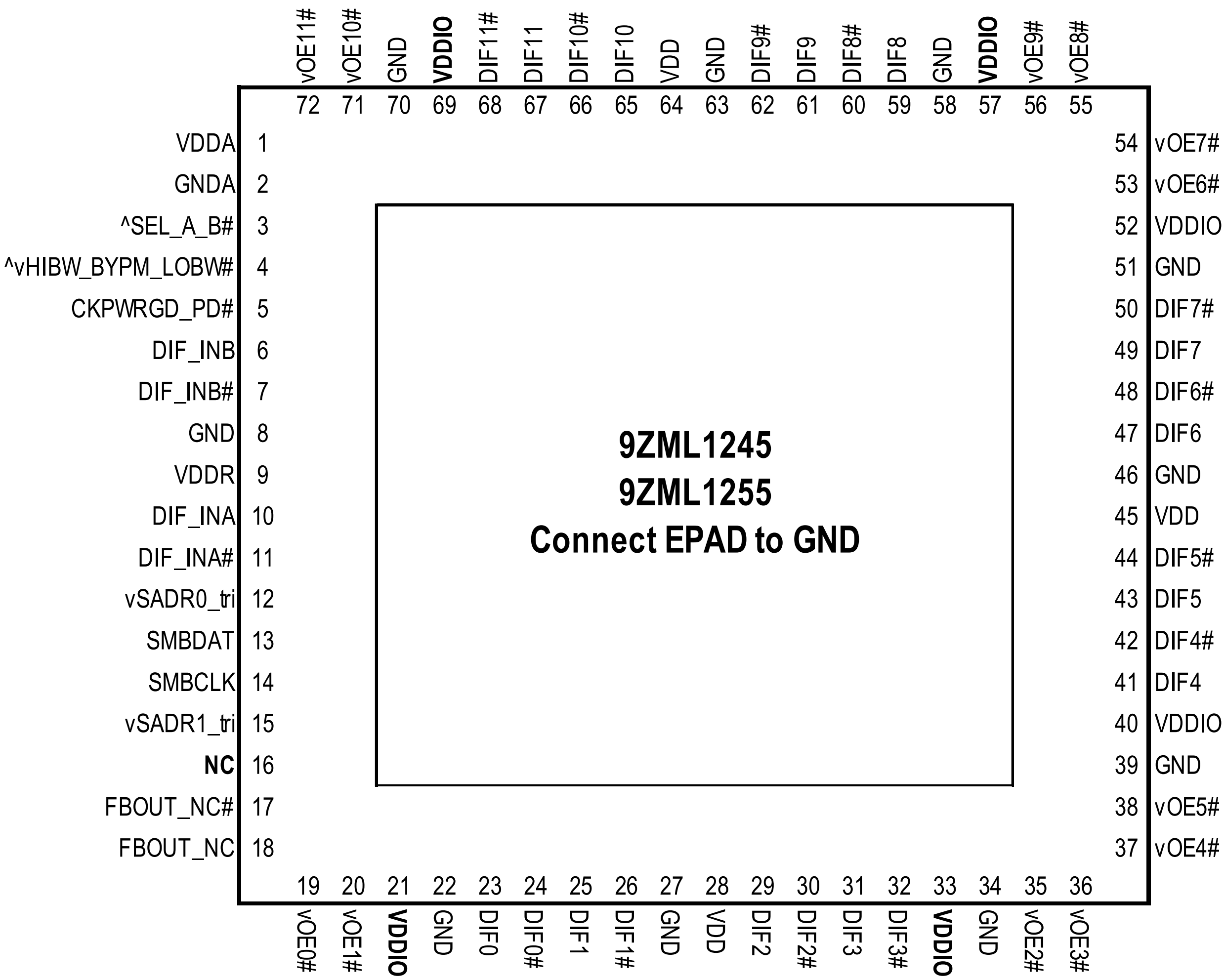
Block Diagram



Contents

Pin Assignments

9ZML1245/9ZML1255



10 × 10 mm, 0.5mm pitch 72-VFQFPN

^ prefix indicates internal 120kOhm pull-up

v prefix indicates internal 120kOhm pull-down

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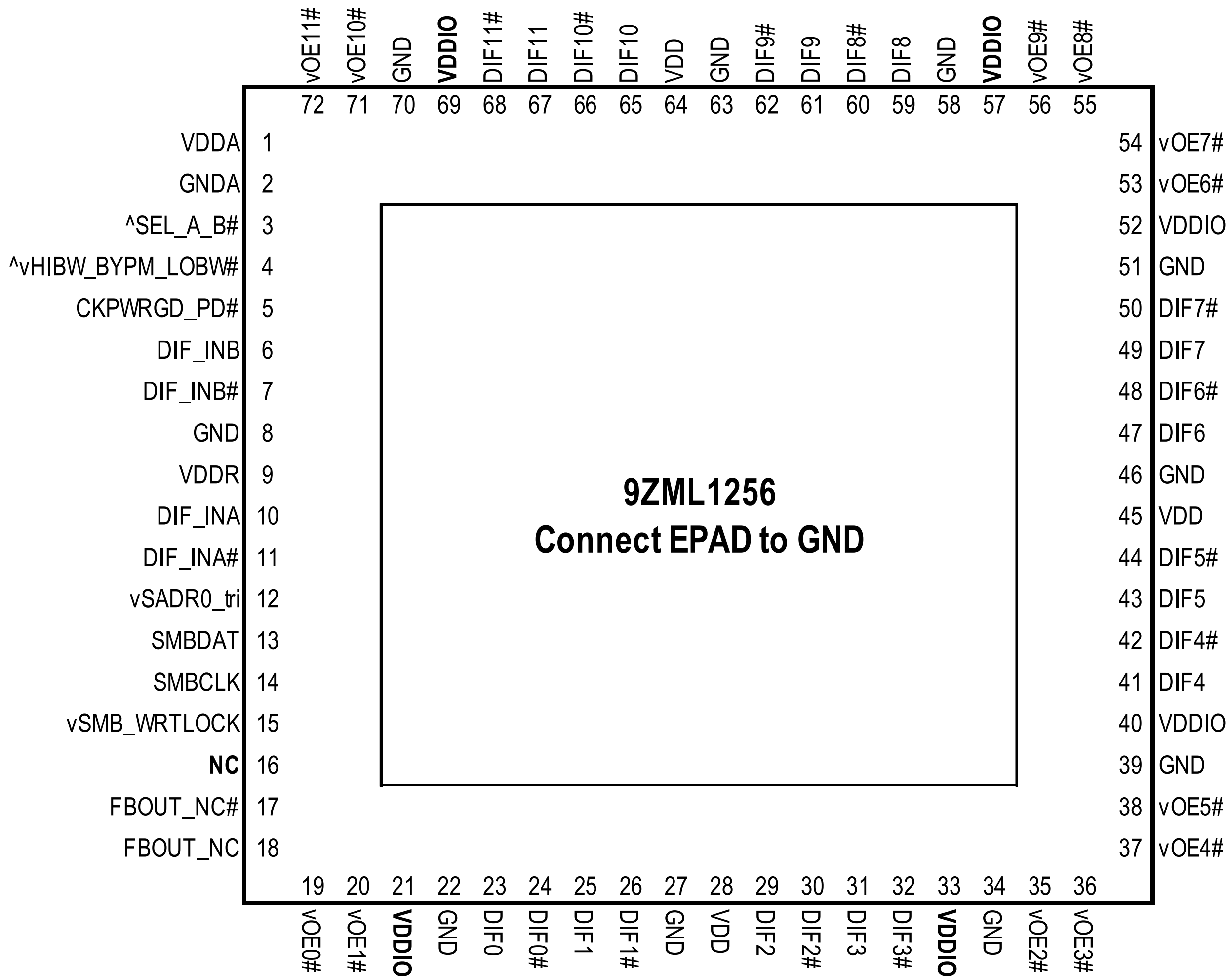
9ZML1256



10 × 10 mm, 0.5mm pitch 72-VFQFPN

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Pin Descriptions

Table 1. Pin Descriptions

Name	Type	Description	9ZML1245/ 9ZML1255 Pin No.	9ZML1256 Pin No.
^SEL_A_B#	Input	Input to select differential input clock A or differential input clock B. This input has an internal pull-up resistor. 0 = Input B selected, 1 = Input A selected.	3	3
^vHIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode table for Details.	4	4
CKPWRGD_PD#	Input	3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.	5	5
DIF_INA	Input	True input of differential clock.	10	10
DIF_INA#	Input	Complement input of differential clock.	11	11
DIF_INB	Input	True input of differential clock.	6	6
DIF_INB#	Input	Complement input of differential clock.	7	7
DIF0	Output	Differential true clock output.	23	23
DIF0#	Output	Differential complementary clock output.	24	24
DIF1	Output	Differential true clock output.	25	25
DIF1#	Output	Differential complementary clock output.	26	26
DIF10	Output	Differential true clock output.	65	65
DIF10#	Output	Differential complementary clock output.	66	66
DIF11	Output	Differential true clock output.	67	67
DIF11#	Output	Differential complementary clock output.	68	68
DIF2	Output	Differential true clock output.	29	29
DIF2#	Output	Differential complementary clock output.	30	30
DIF3	Output	Differential true clock output.	31	31
DIF3#	Output	Differential complementary clock output.	32	32
DIF4	Output	Differential true clock output.	41	41
DIF4#	Output	Differential complementary clock output.	42	42
DIF5	Output	Differential true clock output.	43	43
DIF5#	Output	Differential complementary clock output.	44	44
DIF6	Output	Differential true clock output.	47	47
DIF6#	Output	Differential complementary clock output.	48	48
DIF7	Output	Differential true clock output.	49	49
DIF7#	Output	Differential complementary clock output.	50	50
DIF8	Output	Differential true clock output.	59	59
DIF8#	Output	Differential complementary clock output.	60	60

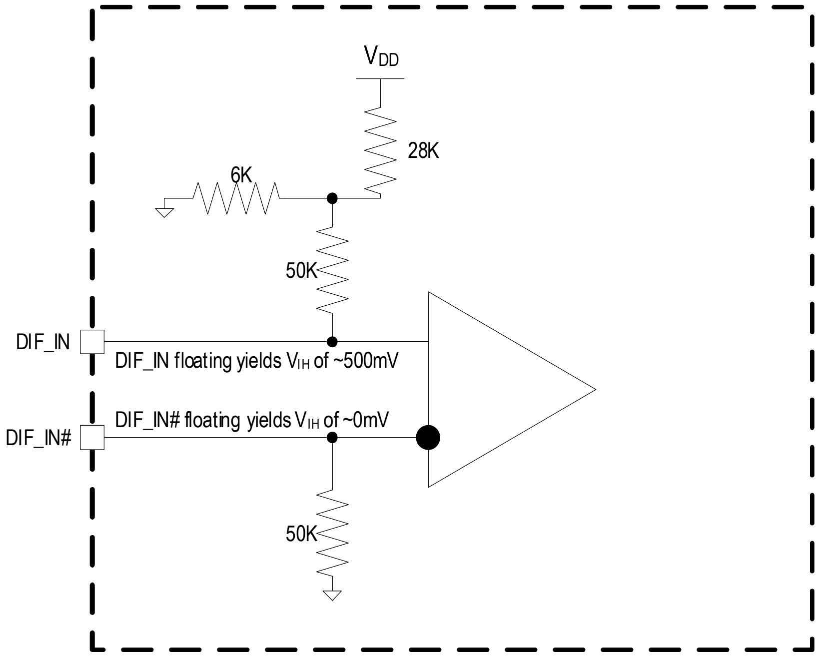
Table 1. Pin Descriptions (Cont.)

Name	Type	Description	9ZML1245/ 9ZML1255 Pin No.	9ZML1256 Pin No.
DIF9	Output	Differential true clock output.	61	61
DIF9#	Output	Differential complementary clock output.	62	62
EPAD	GND	Connect to ground.	73	73
FBOUT_NC	Output	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.	18	18
FBOUT_NC#	Output	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.	17	17
GND	GND	Ground pin.	8	8
GND	GND	Ground pin.	22	22
GND	GND	Ground pin.	27	27
GND	GND	Ground pin.	34	34
GND	GND	Ground pin.	39	39
GND	GND	Ground pin.	46	46
GND	GND	Ground pin.	51	51
GND	GND	Ground pin.	58	58
GND	GND	Ground pin.	63	63
GND	GND	Ground pin.	70	70
GNDA	GND	Ground pin for the PLL core.	2	2
NC	—	No connection.	16	16
SMBCLK	Input	Clock pin of SMBUS circuitry.	14	14
SMBDAT	I/O	Data pin of SMBUS circuitry.	13	13
VDD	Power	Power supply, nominally 3.3V.	28	28
VDD	Power	Power supply, nominally 3.3V.	45	45
VDD	Power	Power supply, nominally 3.3V.	64	64
VDDA	Power	Power supply for PLL core. See Power Connections table for additional information.	1	1
VDDIO	Power	Power supply for differential outputs.	21	21
VDDIO	Power	Power supply for differential outputs.	33	33
VDDIO	Power	Power supply for differential outputs.	40	40
VDDIO	Power	Power supply for differential outputs.	52	52
VDDIO	Power	Power supply for differential outputs.	57	57
VDDIO	Power	Power supply for differential outputs.	69	69
VDDR	Power	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.	9	9

Table 1. Pin Descriptions (Cont.)

Name	Type	Description	9ZML1245/ 9ZML1255 Pin No.	9ZML1256 Pin No.
vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	19	19
vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	20	20
vOE10#	Input	Active low input for enabling output 10. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	71	71
vOE11#	Input	Active low input for enabling output 11. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	72	72
vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	35	35
vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	36	36
vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	37	37
vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	38	38
vOE6#	Input	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	53	53
vOE7#	Input	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	54	54
vOE8#	Input	Active low input for enabling output 8. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	55	55
vOE9#	Input	Active low input for enabling output 9. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	56	56
vSADR0_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addresses table.	12	12
vSADR1_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. It has an internal pull-down resistor. See the SMBus Addresses table.	15	—
vSMB_WRTLOCK	Input	This pin prevents SMBus writes when asserted. SMBus reads are not affected. This pin has an internal pull-down. 0 = SMBus writes allows, 1 = SMBus writes blocked.	—	15

Figure 1. Clock Input Bias Network



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZML1245/9ZML1255/9ZML1256. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDX}				3.9	V_{DD}	1,2
Input Low Voltage	V_{IL}		GND - 0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface.			V_{DD} + 0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins.			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Thermal Characteristics

Table 3. Thermal Characteristics

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
9ZML12xx Thermal Resistance	θ_{JC}	Junction to case.	NLG72	19	°C/W	1
	θ_{Jb}	Junction to base.		0.5	°C/W	1
	θ_{JA0}	Junction to air, still air.		30	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		23	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		20	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		19	°C/W	1

Electrical Characteristics

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 4. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency.			400	kHz	5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Table 5. DIF_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Crossover voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.35		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	μA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 6. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDX}	Supply voltage for core and analog.	3.135	3.3	3.465	V	
Output Supply Voltage	V_{DDIO}	Supply voltage for DIF outputs, if present.	0.95	1.05	3.465	V	5
Ambient Operating Temperature	T_{AMB}	Industrial range (T_{IND}).	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs.	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs.	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-level inputs.	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Tri-level inputs.	1.2	VDD/2	1.8	V	
Input Low Voltage	V_{IL}	Tri-level inputs.	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, $V_{IN} = V_{DD.}$	-5		5	μA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors.	-50		50	μA	
Input Frequency	F_{ibyp}	Bypass/FOB Mode, Ck Detect Disabled (B4b6=0).	1		400	MHz	5
	$F_{ibypCkDet}$	Bypass/FOB Mode, Ck Detect Enabled (B4b6=1).	15		400	MHz	
	F_{iZDB}	100MHz ZDB Mode.	98.5	100.00	102.5	MHz	
ppm Error Contribution	ppm	ppm error contributed to input clock.		0		ppm	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.		1	1.8	ms	1, 2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular modulation).	30		33	kHz	

Table 6. Input/Supply/Common Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	4	5	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# deassertion.		57	300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	2
Trise	t_R	Rise time of control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV, PLL mode.

[4] DIF_IN input.

[5] This is the default value.

Table 7. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDA}	V_{DDA}, PLL Mode at 100MHz.		55	66	mA	1
		V_{DDA}, Fan-out Buffer Mode at 100MHz.		10	13	mA	1
	I_{DD}	All other V_{DD} pins.		16	20	mA	
	I_{DDIO}	V_{DDIO} for LP-HCSL outputs, if applicable.		78	97	mA	
Power Down Current	I_{DDAPD}	V_{DDA}, CKPWRGD_PD# = 0.		4	5	mA	1
	I_{DDPD}	All other V_{DD} pins, CKPWRGD_PD# = 0.		0.5	1	mA	
	I_{DDO}	V_{DDIO} pins, CKPWRGD_PD# = 0.		0.04	0.1	mA	

[1] Includes V_{DDR}.

Table 8. Skew and Differential Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
CLK_IN, DIF[x:0]	t_{SKEW_PLL}	Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage.	-100	9	100	ps	1,2,4,5, 6,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage.	2.3	3	3.8	ns	1,2,3,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature.	-50	0	50	ps	1,2,3,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = 0 to 70°C, default slew rate.	-250	0	250	ps	1,2,3,8
		Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = -40 to +85°C, default slew rate.	-350	0	350	ps	1,2,3,8
CLK_IN, DIF[x:0]	t_{DTE}	Random differential tracking error between two 9ZX devices in Hi BW Mode.		3	5	ps (RMS)	1,2,3,5, 8
CLK_IN, DIF[x:0]	t_{DTSSE}	Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode.		23	50	ps	1,2,3,5, 8
DIF[x:0]	t_{SKEW_ALL}	Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz, default slew rate.		33	50	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1.		1.3	2	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0.		1.2	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1.	2	2.8	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0.	0.7	1.1	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode.	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz.	-0.5	-0.1	0.5	%	1,10
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	PLL Mode.		17	50	ps	1,11

[1] Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
[3] All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
[4] This parameter is deterministic for a given device.
[5] Measured with scope averaging ON to find mean value.
[6] This value is programmable. See I2O programming table.
[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
[8] Guaranteed by design and characterization, not 100% tested in production.
[9] Measured at 3db down or half power point.
[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.
[11] Measured from differential waveform. The device in bypass mode does not add cycle to cycle jitter.

Table 9. LP-HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	2	2.8	4	1 – 4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Slew rate matching. Scope averaging on.		5.3	20	20	%	1,4,7
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	700	808	850	660 – 1150	mV	7,8
Minimum Voltage	Vmin		-150	-35	150	-300		7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	328	395	465.3	250 – 550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		20	50	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes previously separate values of +300mV overshoot and -300mV of undershoot.

Table 10. PCIe Phase Jitter Parameters for ZDB Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limits	Units	Notes
PCIe Phase Jitter, Low Bandwidth ZDB Mode (Common Clocked Architecture)	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1 (2.5 GT/s)		3	7	86	ps (p-p)	1,2
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)		0.09	0.2	3	ps (RMS)	1,2
		PCIe Gen 2 Lo Band (5.0 GT/s)		0.08	0.12	3.1	ps (RMS)	1,2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (8.0 GT/s)		0.05	0.07	1	ps (RMS)	1,2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (16.0 GT/s)		0.05	0.07	0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen 5 (32.0 GT/s)		0.018	0.022	0.15	ps (RMS)	1,2,3,5
PCIe Phase Jitter, Low Bandwidth ZDB Mode (SRIS Architecture)	$t_{jphPCIeG1\text{-}SRIS}$	PCIe Gen 1 (2.5 GT/s)		8.71	8.73	n/a	ps (RMS)	1,2,6
	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (5.0 GT/s)		0.81	0.83	n/a	ps (RMS)	1,2,6
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (8.0 GT/s)		0.329	0.335	n/a	ps (RMS)	1,2,6
	$t_{jphPCIeG4\text{-}SRIS}$	PCIe Gen 4 (16.0 GT/s)		0.222	0.235	n/a	ps (RMS)	1,2,6
	$t_{jphPCIeG5\text{-}SRIS}$	PCIe Gen 5 (32.0 GT/s)		0.084	0.091	n/a	ps (RMS)	1,2,6

Table 10. PCIe Phase Jitter Parameters for ZDB Mode (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limits	Units	Notes
PCIe Phase Jitter, High Bandwidth ZDB Mode (Common Clocked Architecture)	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1 (2.5 GT/s)		5	7	86	ps (p-p)	1,2
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)		0.19	0.25	3	ps (RMS)	1,2
		PCIe Gen 2 Lo Band (5.0 GT/s)		0.09	0.13	3.1	ps (RMS)	1,2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (8.0 GT/s)		0.10	0.13	1	ps (RMS)	1,2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (16.0 GT/s)		0.10	0.13	0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen 5 (32.0 GT/s)		0.032	0.042	0.15	ps (RMS)	1,2,3,5
PCIe Phase Jitter, High Bandwidth ZDB Mode (SRIS Architecture)	$t_{jphPCIeG1\text{-}SRIS}$	PCIe Gen 1 (2.5 GT/s)		8.61	8.63	N/A	ps (RMS)	1,2,6
	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (5.0 GT/s)		0.88	0.96		ps (RMS)	1,2,6
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (8.0 GT/s)		0.354	0.375		ps (RMS)	1,2,6
	$t_{jphPCIeG4\text{-}SRIS}$	PCIe Gen 4 (16.0 GT/s)		0.271	0.305		ps (RMS)	1,2,6
	$t_{jphPCIeG5\text{-}SRIS}$	PCIe Gen 5 (32.0 GT/s)		0.097	0.109		ps (RMS)	1,2,6

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. An additional consideration is the value for which to divide by √2. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by √2, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/√2 = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/√2 = 0.5ps RMS if the clock chip is near the clock input.

Table 11. Additive PCIe Phase Jitter for Fanout Buffer Mode

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limits	Units	Notes
Additive PCIe Phase Jitter, Fanout Buffer Mode[7] (Common Clocked Architecture)	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1 (2.5 GT/s)		1.3	1.9	86	ps (p-p)	1,2
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Hi Band (5.0 GT/s)		0.089	0.126	3	ps (RMS)	1,2
		PCIe Gen 2 Lo Band (5.0 GT/s)		0.023	0.034	3.1	ps (RMS)	1,2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (8.0 GT/s)		0.044	0.062	1	ps (RMS)	1,2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (16.0 GT/s)		0.044	0.062	0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5\text{-}CC}$	PCIe Gen 5 (32.0 GT/s)		0.017	0.024	0.15	ps (RMS)	1,2,3,5
Additive PCIe Phase Jitter, Fanout Buffer Mode[7] (SRIS Architecture)	$t_{jphPCIeG1\text{-}SRIS}$	PCIe Gen 1 (2.5 GT/s)		0.127	0.181	N/A	ps (RMS)	1,2,6
	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (5.0 GT/s)		0.112	0.159		ps (RMS)	1,2,6
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (8.0 GT/s)		0.029	0.042		ps (RMS)	1,2,6
	$t_{jphPCIeG4\text{-}SRIS}$	PCIe Gen 4 (16.0 GT/s)		0.031	0.043		ps (RMS)	1,2,6
	$t_{jphPCIeG5\text{-}SRIS}$	PCIe Gen 5 (32.0 GT/s)		0.027	0.038		ps (RMS)	1,2,6

[1] The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. The total Ref Clk jitter limits for each data rate are listed for convenience. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all results.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.

[4] Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

[5] Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

[6] The PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by $\sqrt{2}$. An additional consideration is the value for which to divide by $\sqrt{2}$. The conservative approach is to divide the ref clock jitter limit, and the case can be made for dividing the channel simulation values by $\sqrt{2}$, if the ref clock is close to the Tx clock input. An example for Gen4 is as follows. A "rule-of-thumb" SRIS limit would be either 0.5ps RMS/$\sqrt{2}$ = 0.35ps RMS if the clock chip is far from the clock input, or 0.7ps RMS/$\sqrt{2}$ = 0.5ps RMS if the clock chip is near the clock input.

[7] Additive jitter for RMS values is calculated by solving for "b" where $b = \sqrt{(c^2 - a^2)}$ and "a" is rms input jitter and "c" is rms output jitter.

Table 12. Filtered Phase Jitter Parameters – QPI/UPI, IF-UPI and DB2000Q

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
Phase Jitter, ZDB Mode	t_{jphQPI_UPI}	QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.19	0.39	0.5	ps (RMS)	1,2
		QPI and UPI (100MHz, 8.0Gb/s, 12UI)		0.10	0.15	0.3	ps (RMS)	1,2
		QPI and UPI (100MHz, ≤11.4Gb/s, 12UI)		0.08	0.12	0.2	ps (RMS)	1,2
Additive Phase Jitter, Fanout Mode	t_{jphQPI_UPI}	QPI and UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.08	0.22	N/A	ps (RMS)	1,2,3
		QPI and UPI (100MHz, 8.0Gb/s, 12UI)		0.04	0.08		ps (RMS)	1,2,3
		QPI and UPI (100MHz, ≤11.4Gb/s, 12UI)		0.03	0.06		ps (RMS)	1,2,3
	$t_{jphIF\text{-}UPI}$	IF-UPI, Lo-BW ZDB Mode		0.10	0.13	1	ps (RMS)	1,4,5
		IF-UPI, Hi-BW ZDB Mode		0.17	0.20	1	ps (RMS)	1,4,5
		IF-UPI, Fanout Mode		0.06	0.07	1	ps (RMS)	1,4
	$t_{jphDB2000Q}$	DB2000Q, Fanout Mode		28	39	80	fs (RMS)	1,4,5

[1] Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details.

[2] Calculated from Intel™-supplied clock jitter tool.

[3] For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{(c^2 - a^2)}$, “a” is rms input jitter and “c” is rms total jitter.

[4] Calculated from phase noise analyzer with Intel-specified brick-wall filter applied. This is an additive jitter specification regardless of buffer operating mode.

[5] The IF-UPI specification is an additive specification, regardless of the buffer operating mode. The enhanced 9ZML devices meet this specification in all operating modes.

Table 13. Phase Jitter Parameters – 12kHz to 20MHz

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Units	Notes
12kHz–20MHz Additive Phase Jitter, Fanout Buffer Mode	$t_{jph12k\text{-}20MFOB}$	Fanout Buffer Mode, SSC OFF, 100MHz		130		N/A	fs (RMS)	1,2,3

[1] Applies to all differential outputs, guaranteed by design and characterization. See Test Loads for measurement setup details.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values, additive jitter is calculated by solving for “b” where $b = \sqrt{(c^2 - a^2)}$, “a” is rms input jitter and “c” is rms total jitter.

Power Management

Table 14. Power Management

Inputs		Control Bits	Outputs		PLL State
CKPWRGD_PD#	DIF_IN	SMBus EN bit	DIF_x	FBOUT_NC	
0	X	X	Low/Low	Low/Low	Off
1	Running	0	Low/Low	Running	On
		1	Running	Running	On

Table 15. Power Connections

Pin Number			Description
V_{DD}	V_{DDIO}	GND	
1		2	Analog PLL
9		8	Analog input
28, 45, 64	**21**, **33**, 40, 52, **57**, **69**	**16**, 22, 27, 34, 39, 46, 51, 58, 63, 70	DIF clocks

Table 16. PLL Operating Mode

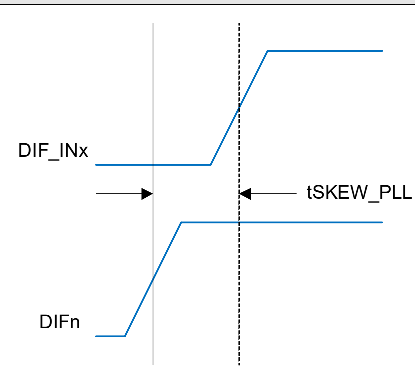
HIBW_BYPM_LOBW#	Byte0[7:6]
Low (PLL Low BW)	00
Mid (Bypass)	01
High (PLL High BW)	11

Note: PLL is OFF in Bypass Mode.

Skew Programming

Table 17. Skew Programming

Skew[2:0]	Skew Steps	Skew (ps)
000	0	0.00
001	1	-416.67
010	2	-833.33
011	3	-1250.00
100	4	-1666.67
101	5	-2083.33
110	6	-2500.00
111	7	-2916.67



Test Loads

Figure 2. Test Load for AC/DC Measurements

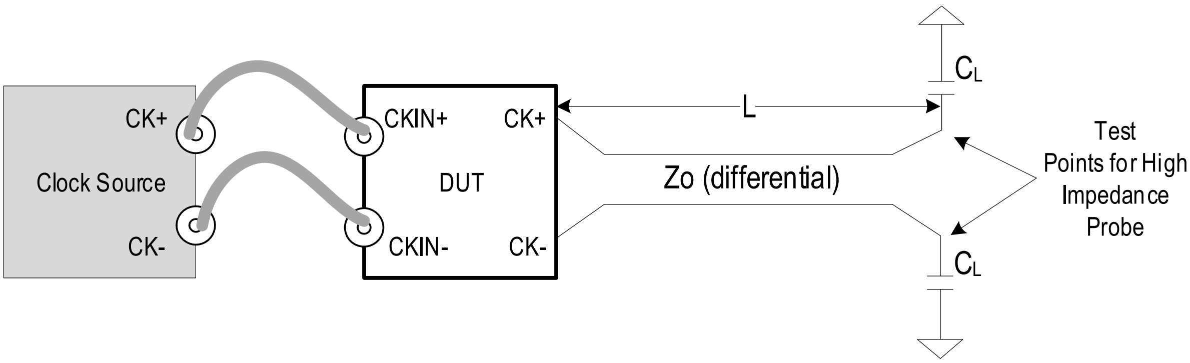


Table 18. Parameters for AC/DC Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Parameters Measured
SMA100B	9ZML124x	Internal	100	25.4	2	AC/DC parameters
SMA100B	9ZML125x	Internal	85	25.4	2	

Figure 3. Test Load for Phase Jitter Measurements using Phase Noise Analyzer

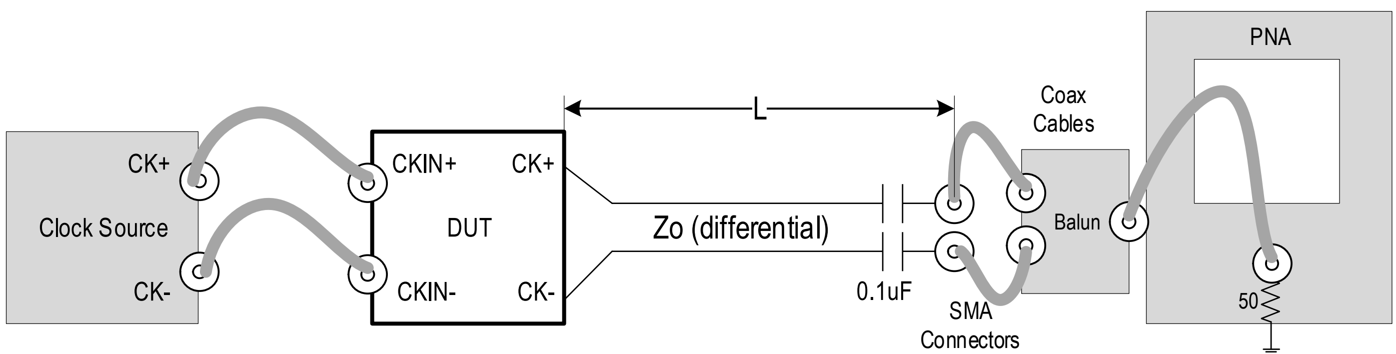


Table 19. Parameters for Phase Jitter Measurements using Phase Noise Analyzer

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Notes	Parameters Measured
SMA100B	9ZML124x	Internal	100	25.4	N/A	Fanout Mode	PCIe, IF-UPI, DB2000Q
9FGV1006	9ZML124x	Internal	100	25.4		ZDB Mode	
SMA100B	9ZML125x	Internal	85	25.4		Fanout Mode	
9FGV1006	9ZML125x	Internal	85	25.4		ZDB Mode	

Figure 4. Test Load for Phase Jitter Measurements using Oscilloscope

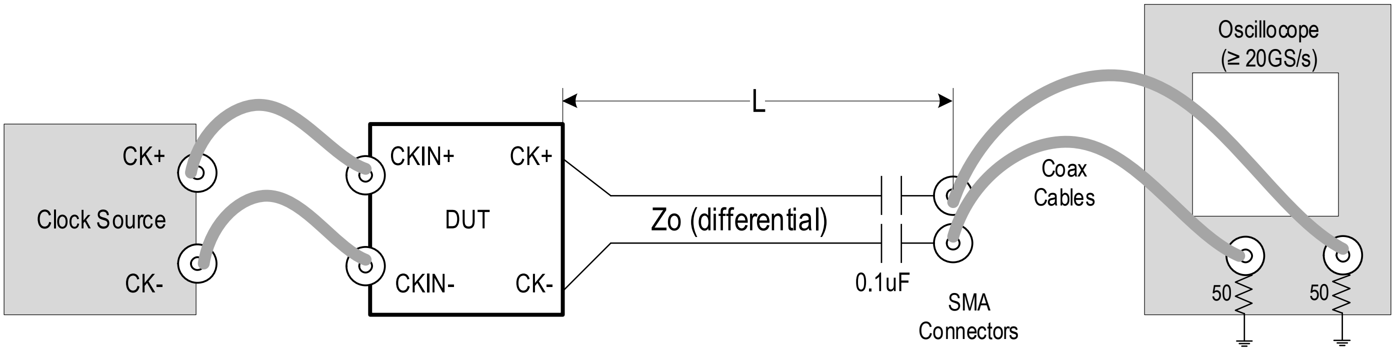


Table 20. Parameters for Phase Jitter Measurements using Oscilloscope

Clock Source	Device Under Test (DUT)	Rs (Ω)	Differential Zo (Ω)	L (cm)	C_L (pF)	Notes	Parameters Measured
SMA100B	9ZML124x	Internal	100	25.4	N/A	Fanout Mode	QPI/UPI
9FGV1006	9ZML124x	Internal	100	25.4		ZDB Mode	
SMA100B	9ZML125x	Internal	85	25.4		Fanout Mode	
9FGV1006	9ZML125x	Internal	85	25.4		ZDB Mode	

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See “AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs” for termination schemes for LVPECL, LVDS, CML and SSTL.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			Renesas
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 21. SMBus Addresses

Pin		SMBus Address	
SADR1_tri	SADR0_tri	9ZML1245/9ZML1255	9ZML1256
0	0	D8	D8
0	M	DA	DA
0	1	DE	DE
M	0	C2	—
M	M	C4	—
M	1	C6	—
1	0	CA	—
1	M	CC	—
1	1	CE	—

Table 22. Byte 0: PLL Mode and Frequency Select Register

Byte 0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	PLL Operating Mode Readback 1	PLL Operating Mode Readback 0	Input Select Readback	SMB_WRTLOCK_ Readback (9ZML1256 only)	Enable S/W control of PLL BW and Input select	PLL Operating Mode 1	PLL Operating Mode 0	Input Select control bit
Type	R	R	R	R	RW	RW	RW	RW
0	00 = Low BW ZDB Mode	01 = Bypass (Fanout Buffer)	DIF_INB is selected	Pin is Low	HW Latch	00 = Low BW ZDB Mode	01 = Bypass (Fanout Buffer)	DIF_INB is selected
1	10 = Reserved	11 = High BW ZDB Mode	DIF_INA is selected	Pin is High	SMBus Control	10 = Reserved	11 = High BW ZDB Mode	DIF_INA is selected
Name	PLL Mode bit [1]	PLL Mode bit [0]	SEL_A_B#	SMB_ WRTLOCK_RB	PLL_SEL_SW_EN	PLL Mode bit [1]	PLL Mode bit [0]	SEL_A_B#
Default	Latch	Latch	Pin	0	0	1	1	1

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 5 via use of bits 2 and 1. The system may require a warm system reset if the user changes these bits. The clock itself does not require a reset. Setting bit 3 to a '1' also allows the user to use bit 0 to control the input select.

Table 23. Byte 1: Output Control Register 1

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output Enable							
Type	RW							
0	Low/Low							
1	OE# Pin Control							
Name	DIF7_en	DIF6_en	DIF5_en	DIF4_en	DIF3_en	DIF2_en	DIF1_en	DIF0_en
Default	1	1	1	1	1	1	1	1

Table 24. Byte 2: Output Control Register 2

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Output _enable			
Type					RW			
0					Low/Low			
1					OE# Pin Control			
Name					DIF11_en	DIF10_en	DIF9_en	DIF8_en
Default	0	0	0	0	1	1	1	1

Bytes 3 is Reserved

Table 25. Byte 4: Input Detect Readback Register

Byte 4	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Input clock presence detect	Enable or disable Input Detect	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Type	R	RW						
0	Selected Input is not present	Input Detect is Disabled						
1	Selected input is present	Input Detect is Enabled						
Name	Input_Detect_RB	Input_Detect_En						
Default	See Note	0	0	0	0	0	0	0

Notes on Byte 4:

Clock detect circuit monitors selected input clock (A or B)

Parks the output clocks in a low/low state ~150ns after input clock disappears.

When enabled (Byte 4, bit 6 set to '1'):

- Bypass Mode minimum operating frequency is 25MHz

- ZDB mode frequency range is unchanged
- Realtime absence or presence of selected input clock may be read back from Byte 4, bit 7

When disabled (Byte 4, bit 6 set to ‘0’ - default):

- Bypass Mode minimum operating frequency is unchanged
- ZDB mode frequency range is unchanged
- Byte 4, bit 7 reads 0
- Part behaves like existing devices

Table 26. Byte 5: Revision and Vendor ID Register

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				Vendor ID			
Type	R	R	R	R	R	R	R	R
0	A rev = 0010				IDT/Renesas = 0001			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0
Default	0	1	0	0	0	0	0	1

Table 27. Byte 6: Device ID Register

Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Device ID							
Type	R	R	R	R	R	R	R	R
0	See table below							
1								
Name	DevID 7	DevID 6	DevID 5	DevID 4	DevID 3	DevID 2	DevID 1	DevID 0
9ZML1245 9ZML1255	0hC5							
9ZML1256	0hC5							

Table 28. Byte 7: Byte Count Register

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Writing to this register configures how many bytes will be read back on a block read.				
Type				RW	RW	RW	RW	RW
0				Default value is 8.				
1								
Name				BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	1	0	0	0

Table 29. Byte 8: Output Skew Register A (when Input Clock A is selected)

Byte 8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Channel A Output delay programming (early)		
Type						RW	RW	RW
0						Binary value of number of VCO periods that outputs will be pulled earlier than input.		
1								
Name						I2O_FB_A Skew2	I2O_FB_A Skew1	I2O_FB_A Skew0
Default	0	0	0	0	0	0	0	0

Note: For example, at 2.4GHz, each VCO period is 416.7ps and there are 24 VCO periods in a 100MHz output. B10[6] determines the accumulative mode of the delay steps. By default, accumulation is disabled and the part operates in absolute mode. This means that the maximum number of skew tuning steps is '111' or 7. In absolute mode, each skew tuning value must be higher than the value previously written. For example, writing '010' pulls the output a total 2 VCO periods earlier. Writing '000' or '001' is not allowed. Writing '011' will pull the output one additional cycle earlier for a total of 3. In accumulative mode, each write to bits [2:0] will pull the output a early by that number of VCO periods. Writing '110' 4 times would pull the output back in phase with the input (360 degrees). Writing '001' twice will accomplish the same result as writing '010' once - pulling the output 2 VCO periods earlier.

Table 30. Byte 9: Output Skew Register B (when Input Clock B is selected)

Byte 9	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Channel A Output delay programming (early)		
Type						RW	RW	RW
0						Binary value of number of VCO periods that outputs will be pulled earlier than input.		
1								
Name						I2O_FB_A Skew2	I2O_FB_A Skew1	I2O_FB_A Skew0
Default	0	0	0	0	0	0	0	0

The note for Byte 8 also applies to Byte 9.

Table 31. Byte 10: Global Amplitude and Delay Step Control Register

Byte 10	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Bypass the skew tuning circuit	Enable accumulative step delay	Reserved	Reserved	Reserved	Global Differential Amplitude Control		
Type	RW	RW				RW	RW	RW
0	Skew Circuit Enabled	Disable				0xx = Reserved, 100 = 750mV 101 = 850mV, 110 = 950mV, 111 = Reserved		
1	Skew Circuit Bypassed	Enable						
Name	Skew Bypass	Accumulate Mode				AMP[2]	AMP[1]	AMP[0]
Default	1	0	0	0	0	1	0	1

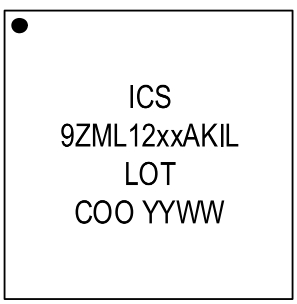
Table 32. Byte 11: Output Configuration Register

Byte 11	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SR_OUT	SR_FB	ZO_OUT[1]	ZO_OUT[0]	ZO_FB[1]	ZO_FB[0]	STP[1]	STP[0]
Control Function	Output slew rate control	Feedback slew rate control	Output differential impedance		Feedback differential impedance		Differential Stop State	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	Slow	Slow	00 = 33ohm 01 = 85ohm (9ZML125x) 10 = 100ohm (9ZML124x) 11 = Reserved		00 = 33ohm 01 = 85ohm (9ZML125x) 10 = 100ohm (9ZML124x) 11 = Reserved		00 = Low/Low	01 = HiZ/HiZ
1	Fast	Fast					10 = High/Low	11 = Low/High
Default	1	1	X	X	X	X	0	0

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



- Lines 1 and 2: truncated part number
  - "xx" denotes 45, 55, or 56
- Line 3: "LOT" denotes the lot number.
- Line 4:
  - "COO" denotes country of origin.
  - "YYWW" denotes the last two digits of the year and work week that the part was assembled.

Ordering Information

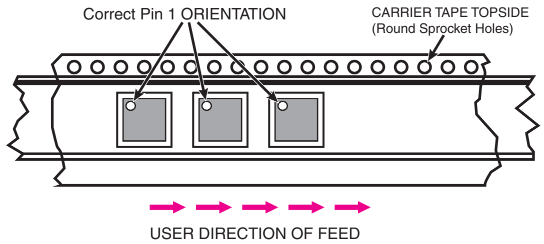
Table 33. Ordering Information

Orderable Part Number	Output Impedance	Description	Number of Clock Outputs	Package	Temperature Range	Part Number Suffix and Shipping Method
9ZML1245AKILF	100	2:12 ZDB/FOB	12	10 × 10 × 0.9 mm 72-VFQFPN	-40°C to +85°C	None = Trays "T" = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 34 for more details)
9ZML1245AKILFT						
9ZML1255AKILF	85	2:12 ZDB/FOB				
9ZML1255AKILFT						
9ZML1256AKILF	85	2:12 ZDB/FOB with SMBus Write Protection				
9ZML1256AKILFT						

"A" is the device revision designator (will not correlate with the datasheet revision).

"LF" denotes Pb-free configuration, RoHS compliant; "T" is the orderable suffix for Tape and Reel packaging.

Table 34. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	

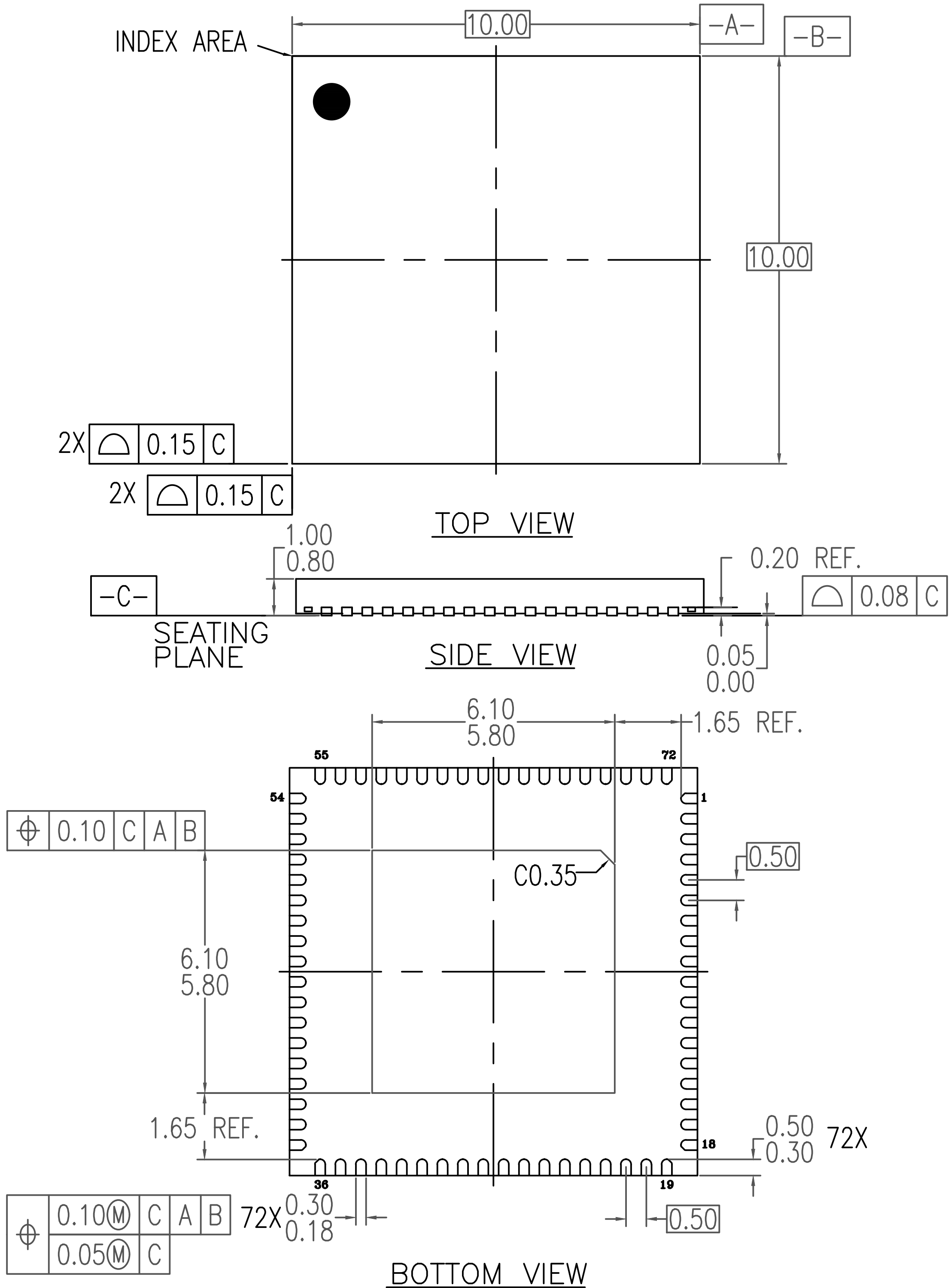
Revision History

Revision Date	Description of Change
May 12, 2021	Updates to Byte 0, bit 0 and bit 5 defaults.
April 29, 2021	Corrected typo in Byte 0, bit 0. Removed reference to 9ZXL devices from footnote for Byte 0.
March 17, 2021	Added Byte 11.
October 9, 2020	Updated Byte 0, bit Control Function. Updated the footnote for this register table.
May 19, 2020	Rebranded document.
November 14, 2019	Combined 9ZML1245, 9ZML1255, and 9ZML1256 datasheets into one single document.

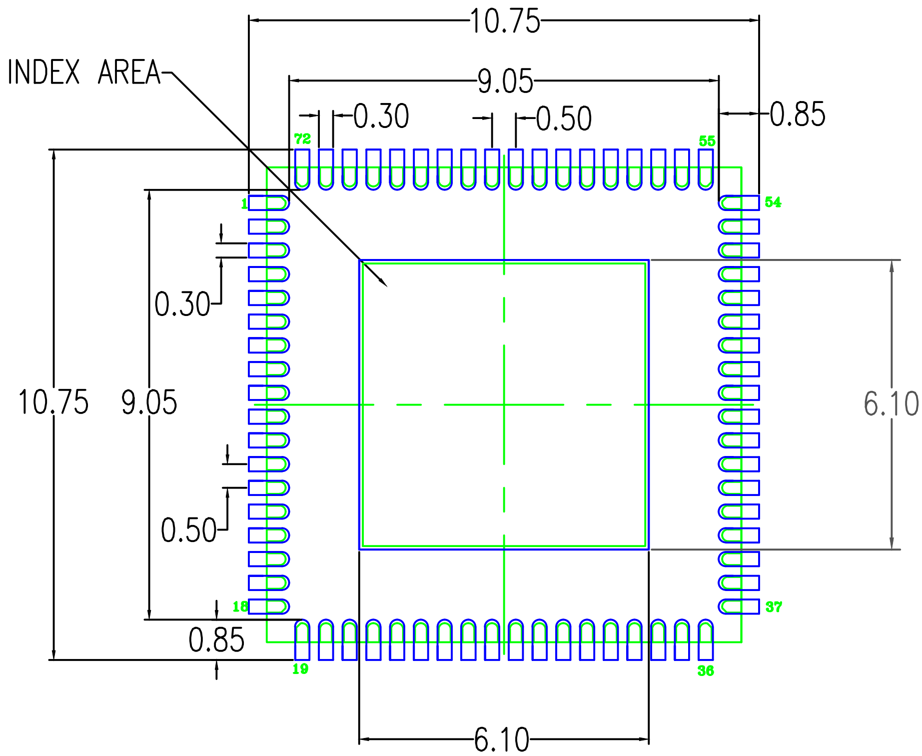
72-VFQFPN, Package Outline Drawing

10.0 x 10.0 x 0.90 mm Body, Epad 5.95 x 5.95 mm 0.50mm Pitch

NLG72P1, PSC-4208-01, Rev 03, Page 1



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 3, 2019	Rev 03	Update P1 Dimension from 5. 8 to 5.95 mm SQ
May 8, 2017	Rev 02	Change Package Code QFN to VFQFPN